6080A

SYNTHESIZED RF SIGNAL GENERATOR

Service Manual

PN 868914
February 1991
©1991 John Fluke Mfg. Co., Inc. All rights reserved. Litho in U.S.A.

FLUKE ®

WARRANTY

Notwithstanding any provision of any agreement the following warranty is exclusive:

The JOHN FLUKE MFG. CO., INC., warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries (rechargeable type batteries are warranted for 90-days), or any product or parts which have been subject to misuse, neglect, accident, or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within 1 year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

> THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. JOHN FLUKE MFG. CO., INC., SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify the JOHN FLUKE MFG. CO., INC., or nearest Service facility, giving full details of the difficulty, and include the model number, type number, and serial number. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of JOHN FLUKE MFG. CO., INC., instruments should be made via United Parcel Service or "Best Way"* prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The JOHN FLUKE MFG. CO., INC, will be happy to answer all applications or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX C9090, EVERETT, WASHINGTON 98206, ATTN: Sales Dept. For European Customers: Fluke (Holland) B.V., P.O. Box 2269, 5600 CG, Eindhoven, The Netherlands.

*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

Rev. 7/88

SAFETY SUMMARY

SAFETY TERMS IN THIS MANUAL

This instrument has been designed and tested in accordance with IEC Publication 348, Safety Requirements for Electronic Measuring Apparatus. This Service Manual contains information, warnings, and cautions that must be followed to ensure safe maintenance and to keep the Signal Generator in a safe condition.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to equipment.

SYMBOLS MARKED ON EQUIPMENT

⚡ DANGER — High voltage.

⏚ Ground (earth) terminal.

⚠ Attention — refer to the manual. This symbol indicates that information about the use of a feature is contained in the manual.

POWER SOURCE

The Signal Generator is intended to operate from a power source that will not apply more than 264V ac rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse identical in type, voltage rating, and current rating to that specified on the rear panel fuse rating label.

GROUNDING THE INSTRUMENT

The Signal Generator is a Safety Class I (grounded enclosure) instrument as defined in IEC 348. The enclosure is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired earth grounded receptacle before connecting anything to any of the Signal Generator connectors. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector appropriate for the voltage and plug configuration in your country.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate the Signal Generator in an atmosphere of explosive gas.

DO NOT ATTEMPT TO OPERATE IF ELECTRIC SHOCK PROTECTION MAY BE IMPAIRED

If the Signal Generator appears damaged or operates abnormally, protection from electric shock may be impaired. Do not attempt to operate it. When in doubt, have the instrument serviced.

DO NOT REMOVE COVER UNLESS QUALIFIED TO DO SO

To avoid electric shock, do not remove the Signal Generator cover unless you are qualified to do so. Service procedures are for qualified service personnel only.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless a person cap-able of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points inside this product. To avoid personal injury, do not touch exposed connections and components while the power is on.

UNPLUG POWER CORD TO REMOVE INSTRUMENT POWER

This product remains energized when the POWER switch is in the STBY position. Disconnect incoming ac power by unplugging the power cord before removing protective panels, soldering, or replacing components.

Table of Contents

SECTION TITLE PAGE

1 **Introduction and Specifications** **1-1**

1-1. INTRODUCTION 1-1
1-2. OPTIONS 1-1
1-3. OBTAINING FACTORY SERVICE 1-2
1-4. SPECIFICATIONS 1-2

2 **Theory of Operation** **2-1**

2-1. INTRODUCTION 2-1
2-2. GENERAL DESCRIPTION 2-1
2-3. FUNCTIONAL DESCRIPTION 2-2
2-4. Frequency 2-2
2-5. Frequency Modulation 2-4
2-6. Internal Modulation Oscillator 2-6
2-7. Phase Modulation 2-6
2-8. Output/Level Control 2-7
2-9. Amplitude Modulation 2-7
2-10. Pulse Modulation 2-7
2-11. Power Supply 2-8
2-12. DIGITAL CONTROLLER SOFTWARE DESCRIPTION 2-8
2-13. User Interface 2-8
2-14. Calibration/Compensation Memory 2-9
2-15. Self Test 2-9
2-16. Status Signals 2-9

3 **Performance Tests** **3-1**

3-1. INTRODUCTION 3-1
3-2. TEST EQUIPMENT 3-1
3-3. POWER-ON TEST 3-4
3-4. FREQUENCY ACCURACY TEST 3-5
3-5. SYNTHESIS TEST 3-5
3-6. HIGH-LEVEL ACCURACY TEST 3-6
3-7. MID-LEVEL ACCURACY TEST 3-9
3-8. LOW-LEVEL ACCURACY TEST 3-10
3-9. ALTERNATE LEVEL ACCURACY TEST 3-11
3-10. FLATNESS TEST 3-13

(continued on page ii)

SECTION TITLE PAGE

3-11. OUTPUT LEAKAGE TEST 3-14
3-12. HARMONIC AND LINE-RELATED SPURIOUS TEST 3-15
3-13. NON-HARMONIC SPURIOUS SIGNALS TEST USING RF SPECTRUM ANALYZER 3-16
3-14. PHASE NOISE, RESIDUAL FM, AND SPURIOUS SIGNALS TEST 3-16
3-15. RESIDUAL AM NOISE TEST 3-20
3-16. MODULATION TESTS 3-22
3-17. Amplitude Modulation Tests 3-23
3-18. Frequency Modulation Tests 3-26
3-19. Phase Modulation Tests 3-28
3-20. Internal Modulation Oscillator Tests 3-30
3-21. VOLTAGE STANDING-WAVE RATIO (VSWR) TESTS 3-31
3-22. PULSE TESTS 3-33
3-23. INTERMODULATION TEST 3-35
3-24. Equipment Verification 3-35
3-25. Intermodulation Distortion Test 3-36

4 Closed-Case Calibration 4-1

4-1. INTRODUCTION 4-1
4-2. Front Panel Calibration 4-1
4-3. Remote Calibration 4-1
4-4. Calibration Data 4-3
4-5. CALIBRATION SETUP 4-3
4-6. AM CALIBRATION 4-3
4-7. Front Panel AM Calibration Procedure 4-4
4-8. Remote AM Calibration Procedure 4-4
4-9. FM CALIBRATION 4-7
4-10. Front Panel FM Calibration Procedure 4-7
4-11. Remote FM Calibration 4-8
4-12. RF LEVEL CALIBRATION 4-9
4-13. Front Panel Level Calibration Procedure 4-10
4-14. Remote Level Calibration Procedure 4-10
4-15. REFERENCE OSCILLATOR CALIBRATION 4-12
4-16. Front Panel Reference Oscillator Calibration Procedure 4-12
4-17. Remote Reference Oscillator Calibration Procedure 4-13

5 Access Procedures 5-1

5-1. INTRODUCTION 5-1
5-2. SAFETY 5-1
5-3. PIVOTING SYNTHESIZER MODULE WARNING 5-2
5-4. LOCATION OF MAJOR ASSEMBLIES 5-2
5-5. ACCESS INSTRUCTIONS 5-2
5-6. Removing the Front Panel Section 5-2
5-7. Removing the Rear Panel Section 5-3
5-8. Raising and Lowering the Synthesizer Module 5-3
5-9. Removing the A2 Coarse Loop PCA 5-4
5-10. Removing the A3 Subsynthesizer VCO PCA 5-5
5-11. Removing the A4 Subsynthesizer PCA 5-5
5-12. Removing the A5 Coarse Loop VCO PCA 5-5
5-13. Removing the A6 Mod Oscillator PCA 5-6

(continued on page iii)

SECTION TITLE PAGE

5-14. Removing the A8 Output PCA 5-6
5-15. Removing the A9 Sum Loop VCO PCA 5-7
5-16. Removing the A10 Premodulator PCA 5-7
5-17. Removing the A11 Modulation Control PCA 5-7
5-18. Removing the A12 Sum Loop PCA 5-8
5-19. Removing the A13 Controller PCA 5-8
5-20. Removing the A14 FM PCA 5-9
5-21. Removing the A20 Attenuator/RPP Assembly 5-9
5-22. Removing the A22 Delay Line Assembly 5-10

6 Circuit Description, Troubleshooting, and Alignment 6-1

6-1. INTRODUCTION 6-1
6-2. TROUBLESHOOTING THE 6080A 6-2
6-3. Parts Replacement 6-5
6-4. MODULE REPLACEMENT 6-5
6-5. A1 Display PCA 6-5
6-6. A2 Coarse Loop PCA 6-5
6-7. A3 Subsynthesizer VCO PCA 6-5
6-8. A4 Subsynthesizer PCA 6-7
6-9. A5 Coarse Loop VCO PCA 6-7
6-10. A6 Mod Oscillator PCA 6-8
6-11. A7 Relay Driver PCA 6-8
6-12. A8 Output PCA 6-8
6-13. A9 Sum Loop VCO PCA 6-8
6-14. A10 Premodulator PCA 6-8
6-15. A11 Modulation Control PCA 6-8
6-16. A12 Sum Loop PCA 6-9
6-17. A13 Controller PCA 6-9
6-18. A14 FM PCA 6-9
6-19. A15 Power Supply PCA 6-9
6-20. A19 Switch PCA 6-9
6-21. A20 Attenuator/RPP Assembly (A7, A21) 6-9
6-22. A22 Delay Line Assembly (A25, A26, Delay Cable, Trim Cable) 6-9
6-23. UPDATING COMPENSATION MEMORY WITH MODULE EXCHANGE DATA 6-10
6-24. SELF TEST DESCRIPTION 6-11
6-25. Digital Tests 6-11
6-26. AM Tests 6-11
6-27. FM Tests 6-11
6-28. ϕM Tests 6-12
6-29. DC FM Test 6-12
6-30. Coarse Loop Tests 6-12
6-31. Subsynthesizer Tests 6-12
6-32. Sum Loop Tests 6-12
6-33. RF OUTPUT Tests 6-12
6-34. Pulse Modulator Tests 6-12
6-35. Filter Tests 6-13
6-36. STATUS SIGNALS AND STATUS CODES 6-13
6-37. SOFTWARE DIAGNOSTIC FUNCTIONS 6-13
6-38. Digital Control Latch Test 6-13
6-39. Instrument Diagnostic State 6-13

(continued on page iv)

SECTION TITLE PAGE

6-40. Set Internal DACs 6-13
6-41. Display Synthesizer Loop Frequencies 6-13

6A Power Supply **6A-1**

6A-1. POWER SUPPLY BLOCK DIAGRAM 6A-1
6A-2. POWER SUPPLY CIRCUIT DESCRIPTION 6A-1
6A-3. POWER SUPPLY TROUBLESHOOTING 6A-4
6A-4. Troubleshooting Procedure 6A-4
6A-5. POWER SUPPLY ADJUSTMENT PROCEDURE 6A-5

6B Digital Controller **6B-1**

6B-1. DIGITAL CONTROLLER BLOCK DIAGRAM 6B-1
6B-2. DIGITAL CONTROLLER CIRCUIT DESCRIPTION (A13) 6B-1
6B-3. Microprocessor 6B-1
6B-4. Memory 6B-1
6B-5. Memory Control 6B-3
6B-6. Front Panel Interface 6B-3
6B-7. IEEE-488 Interface 6B-3
6B-8. Attenuator Control Interface 6B-3
6B-9. Module I/O Interface 6B-3
6B-10. Status and Control Latches 6B-4
6B-11. DIGITAL CONTROLLER TROUBLESHOOTING 6B-4
6B-12. RF Control 6B-4
6B-13. Microprocessor Kernel 6B-5
6B-14. Clock 6B-5
6B-15. Power-On Reset 6B-5
6B-16. Unused Microprocessor Inputs 6B-5
6B-17. Bus Error 6B-5
6B-18. Interrupts 6B-5
6B-19. Microprocessor Bus 6B-6
6B-20. Address Decoder 6B-6
6B-21. I/O Diagnostic Tests 6B-7
6B-22. CALIBRATION/COMPENSATION MEMORY 6B-8
6B-23. Calibration/Compensation Memory Status 6B-8
6B-24. Repairing Calibration/Compensation Memory Checksum Errors 6B-9
6B-25. Calibration/Compensation Memory Origin Status 6B-9
6B-26. FRONT PANEL CIRCUIT DESCRIPTION 6B-9
6B-27. Display PCA 6B-10
6B-28. Data Communications 6B-10
6B-29. Display Filament Voltage 6B-10
6B-30. Bright-Digit Effect 6B-10
6B-31. Switchboard Interface 6B-10
6B-32. Remote Footswitch (AUX Connector) 6B-10
6B-33. Edit Knob Interface 6B-10
6B-34. Display Blanking 6B-11
6B-35. Operate/Standby Selection 6B-11
6B-36. FRONT PANEL TROUBLESHOOTING 6B-11

(continued on page v)

SECTION TITLE PAGE

6C Frequency Synthesis 6C-1

6C-1. FREQUENCY FAULT TREE 6C-1
6C-2. SUBSYNTHESIZER BLOCK DIAGRAM 6C-1
6C-3. A4 SUBSYNTHESIZER CIRCUIT DESCRIPTION 6C-1
6C-4. Single-Sideband Mixer 6C-1
6C-5. N-Divider 6C-4
6C-6. Phase Detector 6C-8
6C-7. Loop Amplifier 6C-9
6C-8. Low-Order Digits Generator 6C-9
6C-9. Dac's and Latches 6C-9
6C-10. SUBSYNTHESIZER TROUBLESHOOTING 6C-9
6C-11. SUBSYNTHESIZER ADJUSTMENTS 6C-13
6C-12. Steering DAC Full-Scale Adjustment 6C-13
6C-13. Lower Clamp Adjustment, R99 .... 6C-13
6C-14. Upper Clamp Adjustment, R98 .... 6C-14
6C-15. SSB Mixer LO Drive Adjustment, R106 .... 6C-14
6C-16. 10-kHz Notch Adjustment, L56 .... 6C-15
6C-17. A3 SUBSYNTHESIZER VCO CIRCUIT DESCRIPTION 6C-16
6C-18. SUBSYNTHESIZER VCO TROUBLESHOOTING 6C-16
6C-19. A2 COARSE LOOP CIRCUIT DESCRIPTION 6C-17
6C-20. Reference Section 6C-17
6C-21. Coarse Loop 6C-20
6C-22. COARSE LOOP TROUBLESHOOTING 6C-23
6C-23. Reference Section 6C-23
6C-24. Main Loop 6C-25
6C-25. COARSE LOOP PCA ADJUSTMENTS 6C-28
6C-26. Discriminator Video Amplifier Offset Adjustment, R102 .... 6C-30
6C-27. Steering Gain Adjustment, R221 .... 6C-30
6C-28. Acquisition Oscillator Level Adjustment, R227 .... 6C-31
6C-29. 40-MHz Oscillator Adjustment, L601 .... 6C-31
6C-30. 80-MHz Filter Tuning, L612 and L613 .... 6C-32
6C-31. 80-MHz Level Adjustment, R617 .... 6C-32
6C-32. 2-MHz Notch Adjustment, L205 .... 6C-33
6C-33. Alternate Reference Frequency Selection 6C-33
6C-34. A5 COARSE LOOP VCO CIRCUIT DESCRIPTION 6C-34
6C-35. COARSE LOOP VCO TROUBLESHOOTING 6C-35
6C-36. SUM LOOP BLOCK DIAGRAM 6C-35
6C-37. A12 SUM LOOP CIRCUIT DESCRIPTION 6C-37
6C-38. RF Section 6C-37
6C-39. Audio Section 6C-39
6C-40. LOOP AMPLIFIER 6C-39
6C-41. ACQUISITION CIRCUITS 6C-39
6C-42. SUM LOOP VCO STEERING CIRCUIT 6C-40
6C-43. SUM LOOP TROUBLESHOOTING 6C-41
6C-44. SUM LOOP ASSEMBLY ADJUSTMENTS 6C-45
6C-45. Steering Level Adjustment, R112 .... 6C-45
6C-46. Buffer Gain Match Adjustment, R121 .... 6C-45
6C-47. FM Null Adjustment, R116 .... 6C-46
6C-48. Loop Gain Adjustment, R167 .... 6C-47
6C-49. Acquisition Oscillator Level Adjustment, R132 .... 6C-47
6C-50. A9 SUM LOOP VCO CIRCUIT DESCRIPTION 6C-48

(continued on page vi)

SECTION TITLE PAGE

6C-51. SUM LOOP VCO TROUBLESHOOTING 6C-49
6C-52. SUM LOOP VCO ASSEMBLY ADJUSTMENT 6C-50

6D RF Level/AM 6D-1

6D-1. RF LEVEL FAULT TREE 6D-1
6D-2. RF LEVEL BLOCK DIAGRAM 6D-1
6D-3. RF LEVEL CIRCUIT DESCRIPTION 6D-4
6D-4. RF Path 6D-4
6D-5. Leveling Loop 6D-6
6D-6. Level Control 6D-7
6D-7. RF LEVEL TROUBLESHOOTING 6D-8
6D-8. Unleveled Condition 6D-8
6D-9. Output Assembly Test Point Signal Information 6D-10
6D-10. RF LEVEL ADJUSTMENTS 6D-10
6D-11. Mod Control PCA Level DAC Offset Adjustment, R23 .... 6D-12
6D-12. Mod Control PCA AM DAC Offset Adjustment, R8 .... 6D-12
6D-13. Mod Control PCA Detector Offset Adjustment, R28 .... 6D-13
6D-14. Mod Control PCA AM Depth Adjustment, R10 .... 6D-14
6D-15. Mod Control PCA RF Level Adjustment, R20 .... 6D-15
6D-16. Mod Control PCA External Modulation Level Indicator Adjustment, R71 .... 6D-16
6D-17. Mod Control PCA Sum Steer Gain Adjustment, R99 .... 6D-16
6D-18. Output PCA Het Mixer Level Adjustment, R72 .... 6D-17
6D-19. Output PCA Het Level Adjustment, R10 .... 6D-18
6D-20. Premodulator PCA Bandwidth Adjustment, R51 and C7 .... 6D-19
6D-21. Output PCA Q16 Bias Adjustment, R96 .... 6D-19
6D-22. Output PCA Q9 Bias Adjustment, R1 .... 6D-20
6D-23. Output PCA Gain Flatness Adjustment, C201 .... 6D-20
6D-24. FM Gain Adjustment, R82, on Mod Control PCA 6D-21
6D-25. FM Steer Gain, R101 on Mod Control PCA 6D-21
6D-26. FM INV Balance, R102 on Mod Control PCA 6D-21
6D-27. ATTENUATOR/REVERSE POWER PROTECTION (RPP) 6D-21
6D-28. ATTENUATOR/RPP TROUBLESHOOTING 6D-22

6E Frequency and Phase Modulation 6E-1

6E-1. FM/ϕM FAULT TREE 6E-1
6E-2. FM/ϕM BLOCK DIAGRAM 6E-1
6E-3. FM/ϕM CIRCUIT DESCRIPTION 6E-1
6E-4. Oscillator Section 6E-4
6E-5. Divider Section 6E-5
6E-6. Phase Detectors, Loop Circuits, and Logic Section 6E-6
6E-7. Modulation Section 6E-9
6E-8. MODULATION CONTROL CIRCUIT DESCRIPTION 6E-11
6E-9. FM Input Voltage Processing 6E-11
6E-10. FM STEER Voltage Generation 6E-12
6E-11. FM Control Signals Generation 6E-12
6E-12. FM TROUBLESHOOTING (A14) 6E-12
6E-13. Frequency Check 6E-12
6E-14. Modulation Check 6E-13
6E-15. Input Signals and Control Input Signals Checks 6E-14

(continued on page vii)

SECTION TITLE PAGE

6E-16. FM ADJUSTMENTS 6E-14
6E-17. Adjustments on the Modulation Control PCA (A11) 6E-14
6E-18. Alignment of FM PCA (A14) 6E-16

6F Internal Modulation Oscillator 6F-1

6F-1. MODULATION OSCILLATOR BLOCK DIAGRAM 6F-1
6F-2. INTERNAL MODULATION OSCILLATOR CIRCUIT DESCRIPTION 6F-1
6F-3. Direct Digital Synthesized Wave Generator 6F-1
6F-4. Pulse Generator 6F-3
6F-5. Signal Routing 6F-3
6F-6. MOD OSCILLATOR TROUBLESHOOTING AND ADJUSTMENTS 6F-4
6F-7. Direct Digital Synthesizer Troubleshooting 6F-4
6F-8. Pulse Generator Troubleshooting 6F-5

7 Compensation Procedures 7-1

7-1. INTRODUCTION 7-1
7-2. LEVEL FLATNESS COMPENSATION 7-1
7-3. Level Flatness Compensation Accuracy Notes 7-3
7-4. Level Flatness Compensation Limits 7-3
7-5. Level Compensation Data Mixing 7-4
7-6. Front Panel Output Flatness Compensation Procedure 7-5
7-7. Het Band Level Adjustment 7-8
7-8. Compensating Level Flatness Errors in an External System 7-9
7-9. Front Panel Output Compensation with Default Attenuator Data 7-9
7-10. Front Panel Attenuator Flatness Compensation Procedure 7-10
7-11. Front Panel Attenuator Flatness Compensation Procedure Using Power Meter 7-15
7-12. REMOTE LEVEL FLATNESS COMPENSATION PROCEDURES .. 7-18
7-13. Remote Output Compensation Procedures 7-18
7-14. Remote Attenuator Compensation Procedure 7-20
7-16. SUB-SYNTHESIZER COMPENSATION PROCEDURES 7-25
7-17. Front Panel Subsynthesizer Compensation Procedure 7-26
7-18. Remote Subsynthesizer Compensation Procedure 7-28
7-19. COARSE LOOP COMPENSATION PROCEDURES 7-29
7-20. Front Panel Coarse Loop Compensation Procedure 7-29
7-21. Remote Coarse Loop Compensation Procedure 7-31
7-22. SUM LOOP COMPENSATION PROCEDURES 7-31
7-22. Front Panel Sum Loop Compensation Procedure 7-32
7-24. Remote Sum Loop Compensation Procedure 7-33

8 List of Replaceable Parts 8-1

Table of Contents 8-1
8-1. INTRODUCTION 8-3
8-2. HOW TO OBTAIN PARTS 8-3
8-3. MANUAL STATUS INFORMATION 8-4
8-4. SERVICE CENTERS 8-4

(continued on page viii)

SECTION TITLE PAGE

9 Options 9-1

9-1. INTRODUCTION 9-1
9-2. 6080A-130 HIGH-STABILITY REFERENCE 9-1
9-3. Adjusting the Reference Frequency 9-1
9-4. List of Replaceable Parts 9-2
9-5. 6080A-132 MEDIUM-STABILITY REFERENCE 9-2
9-6. Adjusting the Reference Frequency 9-2
9-7. List of Replaceable Parts 9-3
9-8. OPTION 6080A-830 REAR OUTPUT/MODULATION INPUT 9-3
9-9. Theory of Operation 9-3
9-10. List of Replaceable Parts 9-4

10 Schematic Diagrams 10-1

Table of Contents 10-1

APPENDICES

Appendix A. Instrument Preset State A-1
Appendix B. Special Function Table B-1
Appendix C. Rejected Entry Codes C-1
Appendix D. Overrange/Uncal Status Codes D-1
Appendix E. Self Test Status Codes E-1
Appendix F. Using the Rear Panel AUX Connector F-1
Appendix G. Example Calibration Controller Programs G-1

List of Tables

TABLE	TITLE	PAGE
1-1.	Specifications for Model 6080A	1-3
2-1.	Frequency Coverage Bands	2-3
2-2.	FM Band Limits (Normal AC-Coupled FM Mode)	2-5
3-1.	Recommended Test Equipment	3-2
3-2.	High-Level Accuracy Test Conditions	3-8
3-3.	Sample High-Level Accuracy Test Conditions	3-8
3-4.	Spurious Signal Test Frequencies	3-17
3-5.	Phase Noise Requirements	3-17
3-6.	Residual FM Requirements	3-18
3-7.	AM Test Conditions	3-25
3-8.	FM 3-dB Bandwidth	3-27
3-9.	Intermodulation Requirements	3-35
4-1.	Front Panel Controls Function for Calibration Procedures	4-5
4-2.	Remote Programming Commands for AM Calibration Procedure	4-5
4-3.	Remote Programming Commands for FM Calibration Procedure	4-8
4-4.	Remote Programming Commands for Level Calibration Procedure	4-11
4-5.	Remote Programming Commands for Reference Oscillator	4-13
6-1.	6080A Module Exchange Assemblies	6-7
6-2.	General Self Test Results	6-14
6-3.	Digital Test Results	6-14
6-4.	AM Test Conditions	6-14
6-5.	FM Tests	6-14
6-6.	Phase Modulation Test Conditions	6-15
6-7.	DC FM Tests	6-15
6-8.	Coarse Loop Tests	6-15
6-9.	Subsynthesizer Tests	6-15
6-10.	Sum Loop Tests	6-16
6-11.	RF Output Tests	6-16
6-12.	Pulse Modulator Tests	6-16
6-13.	6080A Filter Tests	6-17
6-14.	6080 Status Signals and Codes	6-17
6-15.	Special Function 909 Diagnostic State Parameter Settings	6-18
6-16.	Special Functions for Setting DACs	6-18
6-17.	Special Functions for Displaying Internal Frequencies	6-18
6A-1.	Supplies Provided by Power Supply Assembly	6A-3
6C-1.	Subsynthesizer PCA Test Points	6C-11
6C-2.	A3 Subsynthesizer VCO PCA DC Voltages	6C-17
6C-3.	Reference Section Logic Control Line Summary	6C-24

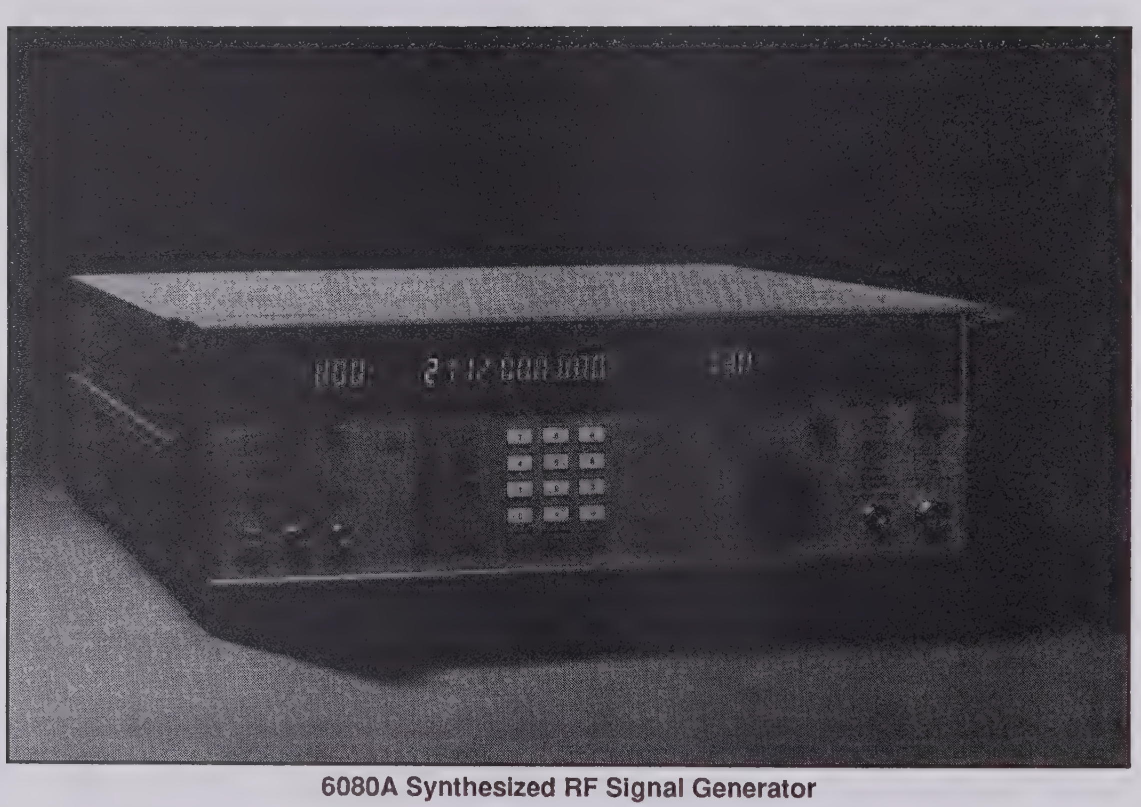
(continued on page x)

LIST OF TABLES, *continued*

TABLE	TITLE	PAGE
6C-4.	Coarse Loop RF Levels	6C-25
6C-5.	N-Divider Logic States	6C-27
6C-6.	Discriminator RF Section Levels	6C-28
6C-7.	A2 Coarse Loop PCA Test Points	6C-29
6C-8.	Setting SW502 for Alternate Reference Frequency	6C-33
6C-9.	Coarse Loop VCO Binary Band Control Signals	6C-34
6C-10.	A5 Coarse Loop VCO PCA Expected DC Voltages	6C-35
6C-11.	Sum Loop Frequencies	6C-37
6C-12.	Preliminary Sum Loop Troubleshooting Checks	6C-42
6C-13.	A12 Sum Loop PCA RF Circuitry Test Information	6C-43
6C-14.	A12 Sum Loop PCA RF Section DC Bias Voltages	6C-43
6C-15.	A12 Sum Loop PCA Test Points	6C-44
6C-16.	Sum Loop VCO Binary Control Signals	6C-48
6C-17.	A9 Sum Loop VCO PCA Expected DC Voltages	6C-50
6D-1.	Band, Filter, and Frequency Programming Logic Signals	6D-9
6D-2.	Frequency Band Logic States	6D-9
6D-3.	Modulator/Detector Nominal Voltages	6D-11
6D-4.	A11 Modulation Control PCA Test Points	6D-11
6D-5.	Attenuator Levels	6D-22
6D-6.	Attenuator Level Control	6D-23
6E-1.	Modulation Control Table (@ 800 MHz RF Frequency)	6E-8
6E-2.	Modulation Ranges and FM DAC Values	6E-10
6E-3.	FM Oscillator Frequency Check Table (Normal Operation)	6E-13
6E-4.	FM Oscillator Modulation Control (Normal Operation)	6E-14
6E-5.	FM Modulation Rate Specifications	6E-17
7-1.	Front Panel Controls for Output Flatness Compensation Procedure	7-6
7-2.	Attenuator Target Levels	7-11
7-3.	Front Panel Controls for Attenuator Flatness Compensation Procedure	7-12
7-4.	Attenuator Target Levels (Power Meter Procedure)	7-16
7-5.	Remote Programming Commands for Level Compensation Procedure	7-23
7-6.	Front Panel Controls for Subsynthesizer Compensation Procedure	7-27
7-7.	Remote Programming Commands for Subsynthesizer Compensation Procedure	7-29
7-8.	Front Panel Controls for Coarse Loop Compensation Procedure	7-30
7-9.	Remote Programming Commands for Coarse Loop Compensation Procedure	7-31
7-10.	Front Panel Controls for Sum Loop Compensation Procedure	7-32
7-11.	Remote Programming Commands for Sum Loop Compensation Procedure	7-33
9-1.	Option -130 High-Stability Reference	9-4
9-2.	Option -132 Medium-Stability Reference	9-4
9-3.	Option -830 Rear Panel RF Output and Modulation Input	9-4

List of Illustrations

FIGURE	TITLE	PAGE
3-1.	Two-Turn Loop	3-4
3-2.	Alternate Level Accuracy Test Equipment Setup	3-12
3-3.	Phase Noise and Non-Harmonic Spurious Test Setup	3-19
3-4.	Residual AM Noise Test Connection Diagram	3-21
4-1.	Basic Structure of Calibration Program	4-2
4-2.	Structure of the AM Calibration Program	4-6
4-3.	Basic Structure of FM Calibration Program	4-8
4-4.	Basic Structure of Level Calibration Program	4-11
4-5.	Basic Structure of the Reference Oscillator Calibration Program	4-16
6-1.	Functional Block Diagram	6-3
6-2.	Instrument Troubleshooting Tree	6-4
6-3.	Assembly Location Block Diagram	6-6
6A-1.	Power Supply Block Diagram	6A-2
6B-1.	A13 Controller Block Diagram	6B-2
6B-2.	Address Decoding	6B-7
6C-1.	Frequency Synthesis Fault Tree	6C-2
6C-2.	Subsynthesizer Block Diagram	6C-3
6C-3.	Triple Modulus Prescaler	6C-5
6C-4.	N-Divider	6C-6
6C-5.	N-Divider Timing Diagram	6C-7
6C-6.	Reference Section Block Diagram	6C-18
6C-7.	A5 Coarse Loop Block Diagram	6C-21
6C-8.	Sum Loop Block Diagram	6C-36
6D-1.	RF Level Fault Tree	6D-1
6D-2.	RF Level Block Diagram	6D-2
6D-3.	A10 Premodulator PCA Block Diagram	6D-3
6E-1.	FM/ϕM Fault Tree	6E-2
6E-2.	FM/ϕM Block Diagram	6E-3
6E-3.	Divider/Phase Detector Timing Diagram	6E-5
6F-1.	Oscillator Block Diagram	6F-2
7-1.	Basic Structure of an Output Compensation Program	7-18
7-2.	Basic Structure of an Attenuator Level Compensation Program	7-20
7-3.	Basic Structure of an Attenuator Compensation Program Using Power Meter	7-23
7-4.	Basic Structure of a Subsynthesizer Compensation Program	7-28
9-1.	Option -130 High and -132 Medium Stability Reference	9-44
9-2.	Option -830 Rear Panel RF Output and Modulation Input	9-45



6080A Synthesized RF Signal Generator

Section 1
Introduction and Specifications

INTRODUCTION 1-1.

The Model 6080A Synthesized RF Signal Generator is a fully programmable, precision, synthesized signal source. The 6080A is designed for applications that require good modulation, frequency accuracy, and output level performance with excellent spectral purity. The 6080A is well suited for testing a wide variety of RF components, subassemblies, and systems, including filters, amplifiers, mixers, and receivers, particularly off-channel radio testing.

Refer to the 6080A/82A Operator Manual for operating instructions, use of the front and rear panel features, remote programming, and all other information for the operator.

This service manual is a maintenance guide for the Signal Generator. The following topics are included:

- Theory of operation
- Closed-case calibration
- Performance testing
- Access procedures
- Troubleshooting and alignment
- Parts lists
- Schematic diagrams

OPTIONS 1-2.

Three options are available for the 6080A:

1. 6080A-830 Rear Output and Modulation Input
2. 6080A-130 High-Stability Reference (see Specifications)
3. 6080A-132 Medium-Stability Reference (see Specifications)

Theory of operation and schematics for these options are contained in the Options section in the 6080A Service Manual.

Refer to the Fluke catalog for price and ordering information. All three options are factory installable only.

OBTAINING FACTORY SERVICE 1-3.

Factory authorized service for the Signal Generator is available at selected Fluke Technical Service Centers. For service, return the Signal Generator to the nearest Fluke Technical Service Center. The local service center will handle transportation to and from the selected service center as required. A complete list of Fluke Sales and Technical Service Centers is provided following the parts lists in Section 10.

To reship the Signal Generator, use its original shipping carton. If the original carton is not available, use a container that provides adequate protection during shipment. Protect the Signal Generator with at least three inches of shock-absorbing material on all sides of the container. Do not use loose fill to pad the shipping container. Loose fill allows the signal generator to settle to one corner of the shipping container, which could result in damage during shipment.

SPECIFICATIONS 1-4.

Table 1-1 lists specifications for the 6080A. Specifications are valid after a warm-up period of 20 minutes. Specifications remain valid after 2 years only if the 6080A is calibrated as described in this manual, and every 2 years or more frequently thereafter. In the specification table, dBc refers to decibels relative to the amplitude of the carrier.

Table 1-1. Specifications for Model 6080A

FREQUENCY

Range: 10 kHz to 1056 MHz. (Also see Internal Modulation Oscillator for coverage from 0.1 Hz to 200 kHz.)

Frequency Bands: The carrier frequency band endpoints are shown below.

BAND DESIGNATION	APPROXIMATE CARRIER FREQUENCY BAND (MHz)	SPECIFIC CARRIER FREQUENCY BAND (MHz)
A	0.01 to 15	0.01 to 14.999,999
B	15 to 32	15 to 31.999,999
C	32 to 64	32 to 63.999,999
D	64 to 128	64 to 127.999,999
E	128 to 256	128 to 255.999,999
F	256 to 512	256 to 511.999,999
G	512 to 1056	512 to 1056

Resolution: 1 Hz

Display Resolution: 10 digits

Stability: Same as Internal Reference Oscillator

10 MHz INTERNAL REFERENCE OSCILLATOR

Type: Temperature Compensated Crystal Oscillator (TCXO)

Temperature Stability: Less than ±1 ppm p-p over the range 0 to +50°C

Typical Aging Rate: Less than ±1 ppm/yr

Reference Output: 10 MHz, >0 dBm for 50Ω load, available at the rear panel REF OUT connector.

PROVISION FOR EXTERNAL REFERENCE

The rear panel REF IN connector accepts an external source of 10 MHz ±10 ppm sine wave, 0.2 to 2.0V rms for a 50Ω load. One alternate external reference frequency setting of 1, 2, or 5 MHz is available at a time, through Special Function 761 or a remote command. The default alternate reference frequency is 5 MHz. See the Service Manual for setting internal DIP switches for use with a 1 or 2 MHz external reference.

AMPLITUDE

Range: +19 to -140 dBm for RF output frequency <512 MHz.
+17 to -140 dBm for RF output frequency >512 MHz.

Resolution: 0.1 dB (0.1% or 1 nV in volts). Annunciators for dB, dBm, V, mV, µV, dBf, dBµV, dBmV, and EMF

Display Resolution: 3 1/2 digits

Accuracy (0 to 50°C):

FREQUENCY (MHz)	AMPLITUDE IN dBm +19 +17 -127 -140
0.01 to 0.1	|<— ±3 dB —>|
0.1 to 0.4	|<— ±2 dB —>|<— ±3 dB —>|
0.4 to 512	|<— ±1 dB —>|<— ±3 dB —>|
512 to 1056	|<— ±1 dB —>|<— ±3 dB —>|

Table 1-1. Specifications for Model 6080A (cont.)

Source SWR: <1.5:1 below +6 dBm
<2.0:1 above +6 dBm

Flatness (0 to 50°C): ±0.75 dB at +10 dBm, for frequencies >0.1 MHz

Intermodulation Distortion (Amplitude of +4 dBm, CW only):

FREQUENCY (MHz)	SPACING 1 kHz	 25 kHz
0.01 to 128 MHz	-60 dBc	-75 dBc
128 to 512 MHz	-65 dBc	-75 dBc
512 to 1056 MHz	-65 dBc	-70 dBc

SPECTRAL PURITY (CW ONLY)

Spurious Signals: <-100 dBc for offsets greater than 10 kHz.

Fixed-frequency spurious signals are <-100 dBc or <-140 dBm, whichever is greater.

Harmonics: <-30 dBc for amplitudes less than +13 dBm.

Subharmonics: None.

Power Line Spurious Signals (offsets less than 10 kHz): <-56 dBc

Residual FM: (NOTE 1)

FREQUENCY BAND (MHz)	RESIDUAL FM 0.3 to 3 kHz	 50 Hz to 15 kHz
0.01 to 15	0.2	0.4
15 to 32	0.2	0.4
32 to 64	0.2	0.4
64 to 128	0.2	0.4
128 to 256	0.4	0.5
256 to 512	0.7	1.0
512 to 1056	1.5	2.0

SSB Phase Noise: (NOTE 1)

CARRIER FREQUENCY BAND (MHz)	OFFSET FREQUENCY 1 kHz (dBc/Hz)	 20 kHz (dBc/Hz)	 100 kHz (dBc/Hz)
0.01 to 15	-112	-138	-138
15 to 32	-124	-145	-146
32 to 64	-118	-144	-146
64 to 128	-112	-144	-145
128 to 256	-106	-141	-144
256 to 512	-100	-136	-142
512 to 1056	-94	-131	-138

Residual AM (50 Hz to 15 kHz Band): < .01% (-80 dBc)

NOTE 1: Allowable operating modes CW, AM, FM (peak dev. <1.5% of max in operating band), ØM (same comment as FM), Pulse.

Table 1-1. Specifications for Model 6080A (cont.)

AMPLITUDE MODULATION

Depth Range: 0% to 99.9% for RF output level <+10 dBm.

AM Resolution: 0.1%

AM Display: 3 digits

AM Accuracy: ±(2% + 4% of setting) for rate = 1 kHz and depth <90%

AM Distortion (Rate = 1 kHz) (NOTE 2): <1.5% THD to 30% AM
<3% THD to 70% AM
<5% THD to 90% AM

AM 3-dB Bandwidth (NOTE 2): AC-coupled AM, 20 Hz to 50 kHz
DC-coupled AM, dc to 50 kHz

Incidental ØM: <0.20 radian at 1 kHz rate and 30% AM

FREQUENCY MODULATION (NOTE 3)

FM Display Ranges: and Resolution	
	0 to 999 Hz Dev, 1 Hz Resolution
	1 to 9.99 kHz Dev, 10 Hz Resolution
	10 to 99.9 kHz Dev, 100 Hz Resolution
	100 to 999 kHz Dev, 1 kHz Resolution
	1 to 4.00 MHz Dev, 10 kHz Resolution

Maximum Deviation:

FREQUENCY BAND (MHz)	MAXIMUM DEVIATION			
	DC-COUPLED FM	AC-COUPLED FM (the smaller of)		
		ABSOLUTE MAXIMUM	RATE LIMITED MAXIMUM	
			DEV ≥ 1/64 MAX	DEV < 1/64 MAX
0.01 to 15	500 kHz	500 kHz	fmod x 5000	fmod x 78
15 to 32	125 kHz	125 kHz	fmod x 1250	fmod x 19
32 to 64	250 kHz	250 kHz	fmod x 2500	fmod x 39
64 to 128	500 kHz	500 kHz	fmod x 5000	fmod x 78
128 to 256	1 MHz	1 MHz	fmod x 10000	fmod x 156
256 to 512	2 MHz	2 MHz	fmod x 20000	fmod x 312
512 to 1056	4 MHz	4 MHz	fmod x 40000	fmod x 625

FM Distortion:

Standard Mode: <2% for 0.5 to 1.0 times maximum deviation; <1% for <0.5 times maximum deviation. Applies for rates of 50 Hz to 50 kHz.

Low-Distortion Mode (Special Function 731): <0.3% for @ 3.5 kHz peak deviation and rates 0.3 to 3 kHz.

FM Accuracy: ±(5% of setting + 10 Hz) for rates of 50 Hz to 50 kHz

---

NOTE 2: *AM specifications apply where (RF output frequency - mod frequency) >150 kHz.*

NOTE 3: *FM specifications apply where: (RF output frequency - deviation) >150 kHz and (RF output frequency - mod rate) >150 kHz.*

Table 1-1. Specifications for Model 6080A (cont.)

FM 3-dB Bandwidth:

DEVIATION	COUPLING	
	INTERNAL AC	EXTERNAL AC (DC)
0% to 25% Maximum	20 Hz to 175 kHz	20 Hz (dc) to 175 kHz
25% to 100% Maximum	20 Hz to 100 kHz	20 Hz (dc) to 100 kHz

Incidental AM: <1% depth for peak deviation <100 kHz at 1-kHz rate and carrier frequency >0.5 MHz
DC-Coupled FM Center Frequency Error, at 1 GHz, after dcFM internal cal, and without any FM range changes: <(.1% of dev + 500 Hz)
Low-Rate External AC-Coupled FM (Special Function 711):

FREQUENCY BAND (MHz)	MAX DEV, IN kHz (AT 10 Hz RATE)	
	SINE WAVE	SQUARE WAVE
0.01 to 15	80	40
15 to 32	20	10
32 to 64	40	20
64 to 128	80	40
128 to 256	160	80
256 to 512	320	160
512 to 1056	640	320

Droop: <30% on a 5 Hz square wave
3-dB Bandwidth: 0.5 Hz to 100 kHz (typical)
Maximum DC Input: ±10 mV
Incidental AM: <1% AM at 1 kHz rate and <10 kHz deviation

PHASE MODULATION (NOTE 4)
Display Ranges: 0 to .999 radians, 1 to 9.99 radians, 10 to 99.9 radians, 100 to 400 radians
Display Resolution: 3 digits

Maximum Deviation:

FREQUENCY BAND (MHz)	MAXIMUM DEVIATION (RADIANS)
0.01 to 15	50
15 to 32	12.5
32 to 64	25
64 to 128	50
128 to 256	100
256 to 512	200
512 to 1056	400

NOTE 4: Phase modulation specifications are valid where (RF frequency - mod frequency) >150 kHz

Table 1-1. Specifications for Model 6080A (cont.)

High-Rate Phase Modulation Maximum Deviation (Special Function 721):

FREQUENCY BAND (MHz)	MAXIMUM DEVIATION (RADIANS)
0.01 to 15	5
15 to 32	1.25
32 to 64	2.5
64 to 128	5
128 to 256	10
256 to 512	20
512 to 1056	40

Accuracy: ±(5% of setting + 0.1 radian) at 1-kHz rate

Distortion (NOTE 5): <2% THD from maximum deviation to 1/2 max deviation, and <1% THD at 1/2 maximum deviation or less at 1-kHz rate.

3-dB Bandwidth: AC-coupled phase modulation, 20 Hz to 15 kHz
DC-coupled phase modulation, dc to 15 kHz

High-Rate Phase Modulation 3-dB Bandwidth (Special Function 721):
AC-coupled phase modulation, 20 Hz to 100 kHz
DC-coupled phase modulation, dc to 100 kHz

Incidental AM (valid for output frequency >500 kHz): 1% AM at 1-kHz rate for peak deviation <10 radians.

PULSE MODULATION (For RF Output Frequencies >10 MHz)

On/Off Ratio: 40 dB minimum for frequencies from 100 to 1056 MHz
60 dB minimum for frequencies <100 MHz

Rise and Fall Times: <15 ns, 10% to 90%

Level Error: For pulse widths >50 ns, the power in the pulse is within ±0.7 dB of the measured CW level.

Duty Cycle (External Modulation): 0 to 100%

Repetition Rate (External Modulation): DC to 10 MHz

Internal Modulation: Internal rates and widths

External Modulation: The pulse input is TTL compatible, terminated in 50Ω with internal active pull-up. It can be modeled as 1.2V in series with 50Ω at the pulse mod input connector. The instrument senses input terminal voltage and turns the RF OUTPUT off when the terminal voltage drops below 1±0.1V. The maximum allowable input is ±10V.

PULSE MODULATION (For RF Output Frequencies <10 MHz)

Rise and Fall Times: <2 times the period of the RF output frequency

Level Error: For pulse widths >10 times the period of the RF output frequency, the power in the pulse is within ±0.7 dB of the measured CW level.

Other pulse specifications are the same as for the >10 MHz frequency range.

NONVOLATILE INSTRUMENT STATE MEMORY

50 instrument states are retained for typically 2 years, even with ac line power disconnected.

REVERSE-POWER PROTECTION

Protection Level: Up to 50 watts from a 50Ω source; up to 50V dc. RF OUTPUT is ac coupled. Protection is provided when the signal generator is turned off.

NOTE 5: *Valid for rates from 50 Hz to 50 kHz in high-bandwidth mode. Does not include effects of residual phase noise.*

Table 1-1. Specifications for Model 6080A (cont.)

Trip/Reset: A flashing RF OFF annunciator indicates a tripped condition. Pressing RF ON/OFF button resets the signal generator.

IEEE-488 REMOTE CONTROL

Extent of Remote Control: All controls except the POWER, REF/INT EXT, and CAL/COMP switches are remotely programmable via the IEEE-488 Interface (Std. 488.2-1987). All status including the option complement are available remotely.

Interface Functions Supported: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC1, DT1, C0, and E2.

INTERNAL MODULATION SOURCE (Sine Wave)

Rates: 0.1 Hz to 200 kHz, key-selectable 400/1000 Hz

Display Ranges: 00.1 to 99.9 Hz
100 to 999 Hz
1.00 to 9.99 kHz
10.0 to 99.9 kHz
100 to 200 kHz

Frequency Resolution: 0.1 Hz or 3 digits

Frequency Accuracy: Same as reference oscillator ±7 millihertz

Output Level Range: 0 to 4V pk into 600Ω

Output Level Resolution: 1 mV pk or 3 digits, whichever is greater.

Distortion: <0.15% THD for output levels >0.2V pk and modulation frequency <20 kHz.

Output Level Accuracy: ±(4% + 15 mV) for modulation frequency <100 kHz.

Output Impedance: 600Ω ±2%

Other Waveforms Available by Special Function:

- Square Wave (Special Function 752)
- Triangle Wave (Special Function 751)
- Pulse (Special Functions 758,759), width 100 ns to 1/Fmod in 100 ns or 3-digit increments, whichever is greater. Rate and width are coherent with signal generator time base.

EXTERNAL MODULATION

1V pk provides indicated modulation index. Nominal input impedance is 600Ω. Maximum level is ±5V pk.

MODULATION MODES

Any combination of AM, PULSE, and FM or ØM, internal or external, may be used.

DIGITAL FREQUENCY SWEEP

Sweep Modes: Auto, single, or manual

Adjustable Parameters: Sweep symmetry, sweep speed, sweep width, and sweep increment.

Sweep Speed: Minimum 40 ms/increment selectable as (minimum + dwell time) where dwell time can be 0, 20, 50, 100, 200, 500 ms, or 1, 2, 5, or 10s at each increment.

DIGITAL AMPLITUDE SWEEP

Sweep Type: Linear (volts) or logarithmic (dB)

Sweep Modes: Auto, single, or manual.

ADJUSTABLE PARAMETERS: Sweep symmetry, sweep speed, sweep width, and sweep increment.

Sweep Speed: Minimum 30 ms/increment selectable as (minimum + dwell time) where dwell time can be 0, 20, 50, 100, 200, 500 ms, or 1, 2, 5, or 10s at each increment.

SWEEP OUTPUT (AUX Connector Pin 5)

0 to +10V ±10%, up to 4096 points in a stepped ramp, load >2 kΩ.

Table 1-1. Specifications for Model 6080A (cont.)

PEN LIFT OUTPUT (AUX Connector Pin 4)

TTL level, high during sweep retrace, load >2 kΩ.

GENERAL SPECIFICATIONS

Temperature: Operating, 0 to +50°C (+32 to +122°F).
Nonoperating, -40 to +75°C (-40 to +167°F).

Operating Humidity Range: 95% to +30°C, 75% to +40°C, and 45% to +50°C.

Operating Altitude: Up to 10,000 ft.

Vibration: Nonoperating, 5 to 15 Hz at 0.06 in, 15 to 25 Hz at 0.04 in, and 25 to 55 Hz at 0.02 in, double amplitude (DA).

Shock: Nonoperating, bench handling per MIL T 28800C Class 5, Style E.

Electromagnetic Compatibility: The radiated emissions induce <0.5 µV (at RF carrier frequency) into a 1-inch diameter, 2-turn loop, 1-inch from any surface as measured into a 50Ω receiver.

Complies with Standards:

- CE03 of MIL-STD-461B (Power and interconnecting leads), 0.015 to 50 MHz.
- RE02 of MIL-STD-461B (14 kHz to 10 GHz).
- FCC Part 15, Class B.
- VDE 0871B
- CISPR 22

Size:	Width	Height	Depth
	43 cm	13.3 cm	59.7 cm
	17 in	5.25 in	23.5 in

Power Requirements: 100, 120, 220, or 240V, each ±10%; 48-63 Hz; 200 VA, <15 VA in standby, with any options installed.

Weight: 27 kg (60 lbs).

OPTION -130 HIGH-STABILITY REFERENCE

Aging Rate: $<\pm 5 \times 10^{-10}$/day, after 21 days continuous operation.

Temperature Stability: $<\pm 2 \times 10^{-10}$/°C. (Oven remains powered in standby.)

OPTION -132 MEDIUM-STABILITY REFERENCE

Aging Rate: $<\pm 1 \times 10^{-7}$/month after 5 days continuous operation.

Temperature Stability: $<\pm 1 \times 10^{-7}$ (0 to +50°C)

OPTION -830 REAR PANEL CONNECTORS

Moves connectors for MODULATION INPUT, MOD output, and RF OUTPUT to the rear panel. The front panel connector locations are covered with plugs.

SUPPLEMENTAL CHARACTERISTICS

The following characteristics are provided to assist in signal generator applications and to describe some other aspects of typical performance.

Frequency Switching Speed: <100 ms to settle within 100 Hz

Amplitude Switching Speed: <100 ms to settle within 0.1 dB

Pulse Modulation Delay: 80 ns typical

Section 2
Theory of Operation

INTRODUCTION 2-1.

This section begins with a description of how the functional blocks of the Signal Generator operate and how the functional blocks interrelate. Detailed circuit descriptions presented in Section 6 expand on the theory discussion.

Theory of operation is presented in the following three major topics:

1. General Description

   Briefly describes the Signal Generator's main functional sections.

2. Functional Description

   Describes functional blocks of the Signal Generator and how they relate to the main output parameters: frequency, amplitude, and modulation.

3. Digital Controller Software Description

   Gives an overview of the software and how it controls the hardware.

GENERAL DESCRIPTION 2-2.

The 6080A Synthesized Signal Generator is made up of the following four major sections:

1. The Front Panel section includes the display and keyboard for local operator interface control, including the primary controls, various external connectors, and indicators. All front panel keys and displays (except the main power switch) are monitored and handled by the A13 Controller PCA, which is housed in the output module.

2. The Synthesizer Module section includes four pca's that generate synthesized RF signals phase locked to a reference standard. The module also houses the modulation oscillator, which is the modulating source for internal AM, FM, ϕM, and pulse.

3. The Output Module section includes circuitry to further refine and process synthesized RF signals. Included is circuitry for properly programming frequency, modulation, and level control. Digital control circuits, including the Controller PCA, are also housed in this module.

NOTE

The Synthesizer and Output module sections house the circuit boards that generate the instrument output signal. These metal, multi-compartmented enclosures shield the circuits, provide an isolation barrier to spurious signals, and isolate circuitry from the outside environment.

4. The Rear Panel section includes the power supply, cooling fan, various external connectors, fuse holder, and line voltage selector.

FUNCTIONAL DESCRIPTION 2-3.

The functional description provides a general overview of the major circuit blocks in the Signal Generator. This description explains how the blocks relate to one another, how they are controlled, and how they generate or use signals. Refer to Section 6, Troubleshooting and Repair, for component-level theory of operation.

The functional blocks of the Signal Generator described in this section are listed below:

- Frequency
- Frequency Modulation
- Internal Modulation Oscillator
- Phase Modulation
- Level Control
- Amplitude Modulation
- Pulse Modulation
- Power Supply
- Digital Controller Software Description

Frequency 2-4.

The output frequency (Fo) is programmable, with 1-Hz resolution, from 10 kHz to 1056 MHz. The band controls are programmed in seven bands determined by the output frequency (Fo). A coarse loop and subsynthesizer frequency are determined for each output frequency.

The coarse loop frequency and the instrument-specific compensation data determine the programming of the coarse loop steering digital-to-analog converter (dac), compensation dac, and voltage controlled oscillator (vco) control bits.

The subsynthesizer frequency and the instrument-specific compensation data determine the programming of the subsynthesizer compensation dac.

The output frequency and the instrument-specific compensation data generate the programming of the sum loop steering and compensation dac's.

The 10-kHz to 1056-MHz frequency coverage is divided into the seven bands shown in Table 2-1.

The Sum Loop VCO assembly produces a signal that ranges from 480 to 1056 MHz. This signal is divided by factors of 2 to produce the bands shown in Table 2-1. The HET band is produced by mixing 80.01 to 94.999999 MHz (from the Divide-by-8 band) with 80 MHz to produce 0.01 to 14.999999 MHz.

Table 2-1. Frequency Coverage Bands

BAND	FREQUENCY COVERAGE
HET	0.01 to 14.999999 MHz
Divide-by-32	15 to 31.999999 MHz
Divide-by-16	32 to 63.999999 MHz
Divide-by-8	64 to 127.999999 MHz
Divide-by-4	128 to 255.999999 MHz
Divide-by-2	256 to 511.999999 MHz
Fundamental	512 to 1056 MHz

Three signals are combined in the Sum Loop PCA: the output of the Sum Loop VCO, the Coarse Loop output signal, and the 80 MHz signal from the FM PCA. These signals are combined as follows.

The first mixer combines the Sum Loop VCO PCA output (at the fundamental frequency, 480 to 1056 MHz) with the Coarse Loop frequency (576 to 960 MHz in 8 MHz steps) to produce a signal of 88 to 96 MHz. This signal is subsequently mixed with the 80 MHz signal from the FM PCA to produce 8 to 16 MHz. This 8 to 16 MHz signal is compared with an 8 to 16 MHz signal in 0.5 Hz steps that is derived on the Subsynthesizer VCO PCA. The comparison results in a dc control voltage that locks the loop.

If the Sum Loop output frequency is below 760 MHz, the FM and Subsynthesizer signals are subtracted from the Coarse Loop signal. If the Sum Loop output frequency is above 760 MHz, the FM and Subsynthesizer signals are added to the Coarse Loop signal.

The A2 Coarse Loop PCA contains the reference circuits and generates a 576-to 960-MHz signal in 8-MHz steps. The main reference frequency for the Signal Generator is a 40-MHz crystal oscillator. This oscillator is phase locked to either an internal 10-MHz TCXO or to an external reference. Either a 10-MHz (default) or an alternate 5-, 2-, or 1-MHz external reference may be selected by special function. (The setting of 5-, 2-, or 1-MHz for the alternate external reference is selectable by setting a switch on the Coarse Loop PCA. Its default is 5 MHz.) The Course Loop PCA doubles the 40-MHz reference frequency to 80 MHz. This frequency is the local oscillator for the HET band and is divided to 20 MHz for use as the reference for the A14 FM PCA.

The Coarse Loop generates the 576- to 960-MHz signal using a combination of phase lock and delay line discriminator frequency control circuitry to produce a low phase noise signal. The delay line is a 125-ns cable contained in the module.

The Subsynthesizer generates a 16- to 32-MHz signal with 1 Hz resolution. This is further divided on the Sum Loop PCA to 8 to 16 MHz. The subsynthesizer generates fine frequency steps using a modified N-divider loop with a single-sideband (SSB) mixer in the feedback path.

The reference frequency for the loop is 1 MHz, which would normally provide 1-MHz steps in a conventional N-divider loop. However, by using pulse deletion, which is controlled by a rate multiplier, the resolution is extended to 10 kHz. Additional resolution is gained by introducing a 10- to 20-kHz signal in a SSB mixer. This signal is produced by a gate array, which contains a 14-bit rate multiplier.

The A14 FM PCA generates an 80-MHz signal that can be frequency modulated.

Frequency Modulation 2-5.

The output signal is modulated by either the internal modulation oscillator or an external frequency source. Modulation rates can be varied from dc to 200 kHz, and the following modes of frequency modulation can be selected:

- Normal ac FM

  Bandwidth from 20 Hz to 200 kHz.

- Low-rate FM

  Certain applications require FM at very low modulation rates but cannot accept the FM loop unlocked condition associated with the dc FM mode. Bandwidth is enabled down to 0.5 Hz;, however, maximum deviations are limited.

- DC FM

  This mode allows the RF output signal to be frequency modulated by a dc signal. Maximum deviations can still be realized; however, the modulation loop oscillator is not locked to the Signal Generator's main timebase. When dc FM is enabled, the FM oscillator's center frequency (80 MHz) is set to the previously locked center frequency (±1 kHz) by an automatic zeroing circuit in conjunction with a software routine. This search for an FM loop correction voltage is called a dc FM cal cycle. The front panel displays the word "PAUSE" during this time. The time required to perform a cal cycle is determined by the internally selected FM deviation band (deviations in excess of 250 kHz can take a cal cycle up to 5 seconds). While dc FM is enabled, the RF output frequency slowly drifts with time.

- Low-distortion mode

  This mode provides the optimum phase noise-to-distortion performance at 3.5 kHz FM deviation at modulation frequencies of 300 Hz to 3 kHz.

Refer to Section 6E for more detailed information about frequency modulation.

Frequency modulation (FM) is programmable to three digits of resolution through six deviation ranges. The maximum programmable FM deviation depends on the RF frequency output. Deviation up to 4 MHz is possible (see Table 2-2, FM Band Limits) on the high RF band. The input modulating signal is level programmed using a 12-bit FM dac and then routed through two different paths for correct ranging. The two paths, high rate and low rate, are required for flat frequency response. These modulating signals are then summed into a phase-locked loop (PLL) circuit.

Table 2-2. FM Band Limits (Normal AC-Coupled FM Mode)

FREQ BAND FM BAND	512 to 1056 MHz	256 to 512 MHz	128 to 256 MHz	64 to 128 MHz and 0.01 to 15 MHz	32 to 64 MHz	15 to 32 MHz
6	4.00 MHz 1.01 MHz	2.00 MHz 501 kHz	1.00 MHz 251 kHz	500 kHz 126 kHz	250 kHz 62.6 kHz	125 kHz 31.3 kHz
5	1.00 MHz 251 kHz	500 kHz 126 kHz	250 kHz 62.6 kHz	125 kHz 31.3 kHz	62.5 kHz 15.7 kHz	31.2 kHz 7.82 kHz
4	250 kHz 62.6 kHz	125 kHz 31.3 kHz	62.5 kHz 15.7 kHz	31.2 kHz 7.82 kHz	15.6 kHz 3.91 kHz	7.81 kHz 1.96 kHz
3	62.5 kHz 15.7 kHz	31.2 kHz 7.82 kHz	15.6 kHz 3.91 kHz	7.81 kHz 1.96 kHz	3.90 kHz 977 Hz	1.95 kHz 489 Hz
2	15.6 kHz 3.91 kHz	7.81 kHz 1.96 kHz	3.90 kHz 977 Hz	1.95 kHz 489 Hz	976 Hz 245 Hz	488 Hz 123 Hz
1	3.90 kHz 0 Hz	1.95 kHz 0 Hz	976 Hz 0 Hz	488 Hz 0 Hz	244 Hz 0 Hz	122 Hz 0 Hz
0	CW MODE					

The PLL circuit is made up of four major sections: an 80-MHz oscillator, two programmable dividers, two selectable phase detectors, and a loop amplifier. These circuits, including the two modulating signal paths, are located on the A14 FM PCA.

The first of these sections is the 80-MHz oscillator. The 80-MHz FM oscillator has two selectable deviation modes to cover the deviation ranges. These deviation modes are:

1. The low (low noise) deviation mode. In this mode the oscillator runs in the high-Q mode.

2. The high-deviation mode. In this mode the tuning sensitivity of the oscillator is increased causing a higher level of phase noise. A linearizer circuit is added to the loop at higher deviation ranges to maintain low distortion.

The second PLL section consists of two programmable divider networks. These networks supply the needed frequencies for the phase detectors. One network divides the reference frequency while the other network divides the oscillator frequency. Both frequencies are divided by a predetermined amount (4,100 or 400) depending on them FM mode and deviation range.

The third PLL section consists of two selectable phase detector circuits. Only one of two phase detectors is active at any time. One of these is a standard dual flip-flop phase detector used in low deviation bands. The other is a N-PI phase detector (that uses a up/down counter and a dac), which allows a large amount of deviation at low modulating rates. The phase detectors produce output signals that are related to the phase relationship of the divided FM oscillator to the divided reference frequency. The output is then applied to the loop amplifier.

The fourth section in the PLL circuitry. The loop amplifier forms Control circuits select the loop amplifier's feedback path to control the phase-locked bandwidth. The output of the amplifier feeds through a low-pass filter before completing the loop back to the 80-MHz oscillator as the loop-control voltage.

Internal Modulation Oscillator 2-6.

The modulation oscillator operates as either a direct digital synthesizer (DDS) or as a pulse generator. Both functions are implemented in a custom integrated circuit and are synthesized from the main reference frequency source of the Signal Generator.

The DDS is the modulating source for internal AM, FM, and ϕM. It can digitally synthesize sine, triangle, and square waveforms at a specified modulating frequency.

The DDS wave generator frequency can be varied from 0.1 Hz to 200 kHz at a resolution of 0.1 Hz. The oscillator is based on an algorithmic wave generation method. This method provides a very accurate and stable signal source of high purity and low harmonic distortion level. The waveform data generated by the algorithm is stored in two EPROMs.

As mentioned earlier, the modulation oscillator can also be configured as a pulse generator whose pulse width and repetition rate are programmable. In the pulse generation mode, frequency can be programmed from 10 Hz to 200 kHz, which results in a pulse period of 100 ms through 500 us. The pulse width can be set from 100 ns to 100 ms with a resolution of 100 ns.

The modulator oscillator output signals are available at the front panel MOD OUTPUT BNC connector.

Refer to Section 6F for more information about the internal modulation oscillator.

Phase Modulation 2-7.

Phase modulation (ϕM) is programmable with three digits of resolution in six ranges. Phase modulation is internally normalized to 10 kHz, then programmed as FM deviation. The ϕM index is multiplied by 10 kHz (regardless of the modulation frequency) to get the equivalent FM deviation. Refer to Table 6E-2 (Section 6E) to determine the FM dac and range settings from this equivalent FM deviation.

The maximum programmable phase modulation deviation is dependent on the RF output frequency. Regardless of the output frequency, phase modulation deviations up to 400 radians may be entered. However, the STATUS indicator blinks and the FM dac clamps at full scale if the entry is beyond the allowed upper limit for that frequency band. The maximum programmable phase modulation deviation in each frequency band is listed in Section 4C of the Operator Manual.

Phase modulation is achieved by reconfiguring the modulation circuits to cause a true phase modulation response for both internal and external modulation inputs. The display is correspondingly changed to indicate deviation in radians. Two modes are available: large deviation at a limited bandwidth and limited deviation for a higher rate bandwidth.

Output/Level Control 2-8.

Two separate circuits provide output/level control: a step attenuator and a vernier level dac. The A20 Attenuator/RPP Assembly provides coarse level control in 6.02-dB steps. Fine level control is provided by a vernier level dac (level-control multiplying dac) that varies the leveling-loop control voltage. The controller microprocessor automatically controls the step attenuator and the multiplying factor of the vernier level dac so that they correspond to the programmed signal level. The multiplying factor also includes level correction information to compensate for the Signal Generator frequency response.

Level-correction data for both the A8 Output PCA and the A20 Attenuator/RPP Assembly is stored in the compensation memory located on the A13 Controller PCA. The level correction data is based on measurements taken of each assembly during level compensation of the Signal Generator.

Level-correction data is applied to the vernier level dac only and does not affect the coarse level control provided by the Attenuator/RPP Assembly. In other words, all Signal Generators have the same attenuator pads inserted at a selected level even though the correction data differs for each signal generator.

To help maintain level accuracy when temperature is varying, signal generator operating software compensates for temperature variations. This method of compensation relies on data that remains constant for all Model 6080A Signal Generators.

Amplitude Modulation 2-9.

A 12-bit multiplying AM dac programs the amplitude modulation depth from 0 to 99.9% with 0.1% resolution. A nominal setting of 2997 on the AM dac corresponds to 99.9% AM depth.

The AM dac receives a 1V pk modulating signal from the internal modulation oscillator or from the external MOD INPUT connector. The A13 Controller PCA calculates the multiplying factor of the dac signal and sums it with a fixed dc reference voltage. The multiplying factor of the dac corresponds to the programmed percentage of modulation.

The dc-plus-modulation composite signal is then summed with the leveling loop-control voltage of the level dac. The automatic level control (ALC) circuitry modulates the RF signal's amplitude by forcing the RF amplitude to track the loop-control voltage.

Refer to Section 6D-6 for more information about amplitude modulation.

Pulse Modulation 2-10.

A single-pole single-throw GaAs FET switch located at the input to the output amplifier acts as a pulse modulator. This switch is driven by the internal modulation oscillator or by an external signal. The GaAs FET switch provides a very fast, high on/off-ratio RF pulse.

Power Supply 2-11.

The power supply provides +15V, -15V, +5V, +37V, +30V, +24V, +23.4V dc, and 6V ac to the Signal Generator. All the supplies are series-pass regulated except the 6V ac display-filament supply. A fuse/filter/line-voltage selector allows the Signal Generator to operate from 100, 120, 220, or 240V ac.

Refer to Section 6A for more information about the power supply.

DIGITAL CONTROLLER SOFTWARE DESCRIPTION 2-12.

A 68HC000 microprocessor located on the A13 Controller PCA executes the Signal Generator software, which is stored in 512K bytes of ROM. The program stack and RAM variables are stored in 64K bytes of static RAM. 8K bytes of battery-backed CMOS RAM are available: 4K bytes act as a nonvolatile memory for front panel setups (instrument state memory), and 4K bytes are used for calibration/compensation data. In addition, an 8K byte EEPROM contains a redundant copy of the calibration/compensation data. The Controller PCA software performs the following general functions:

- Services the front panel and the IEEE-488 Interface.
- Configures the hardware to produce the required output then applies calibration and compensation data to optimize the performance.
- Implements a set of self test and diagnostic functions.

Refer to Section 6B for more detailed information about the digital controller.

User Interface 2-13.

The software operating system allows several tasks to operate in a round-robin fashion. Input and output to both the front panel and the IEEE-488 Interface execute at a higher priority and are handled as interrupt routines.

At power-on, the software performs a self test and initializes both the RAM and the RF hardware. Four tasks are continuously in operation:

- Diagnostic service task
- Front panel key task
- Knob task
- IEEE-488 task

The diagnostic service task monitors the instrument status signals. The front panel key task, knob task, and IEEE-488 task process user input. A fifth task controls the RF output when a frequency or amplitude sweep is active. A sixth task is activated only when needed to process certain STATUS (out-of-range or malfunction) or REJ ENTRY (rejected entry) conditions that cause the display to flash. A seventh task is activated when the automatic user compensation procedures have been initiated.

Calibration/Compensation Memory 2-14.

The calibration/compensation memory contains the instrument-specific compensation data for the coarse loop compensation dac, coarse loop steering dac, sum loop compensation dac, sum loop steering dac, subsynthesizer compensation dac, the Output assembly, and the Attenuator/RPP Assembly. In addition, the calibration/compensation memory stores the AM, FM, level, and reference oscillator calibration data. Since the integrity of this data is crucial to the performance of the Signal Generator, redundant copies of the data are kept in two separate nonvolatile memory ICs.

Hardware and software protection schemes guard against accidental erasure of calibration/compensation data. The rear panel switch (labeled CAL|COMP) must be set to the 1 (ON) position before updating the calibration/compensation memory.

The calibration/compensation memory self test verifies the CRC checksums of each data segment. A detailed report of the compensation memory status can be interrogated from the front panel or the IEEE-488 interface. If the self-test detects errors, the Signal Generator uses only the valid data segments. See Appendix F for the compensation memory status codes.

Self Test 2-15.

The Signal Generator automatically performs a self test of all circuits at power-on. If the instrument fails any of these self tests, the test results automatically display as error codes. Several special functions are available for additional tests. (See "Self Test Description" in Section 6.) Also, the microprocessor continuously monitors hardware status signals. (See Appendix E for self test codes.)

Status Signals 2-16.

Software continuously monitors the status of the rear panel REF EXT/INT reference switch. Depending on the position of this switch, the EXTREF annunciator on the front panel lights or stays off, and the Signal Generator configures itself for internal or external reference.

The RF output of the Signal Generator is usable, but it is not necessarily calibrated if the STATUS indicator is steadily lit. The STATUS indicator blinks on and off to indicate an unusable output due to a severe overrange condition or a circuit failure. See Appendices C and D for a listing of rejected entry and STATUS codes.

Section 3
Performance Tests

INTRODUCTION 3-1.

The information in Section 3 describes the performance tests for the key parameters of the 6080A Synthesized Signal Generator.

Instrument specifications are used as the performance standard. These closed-case performance tests may be used as:

- An acceptance test on receipt of the instrument.
- An indication that repair and/or calibration is required.
- A performance verification after completing repairs or calibration of the instrument.

Individual performance tests can also be used as troubleshooting aids.

Warm up the Signal Generator (or the UUT for Unit Under Test) being tested with all covers in place for at least 2 hours before beginning the performance tests.

Fluke recommends that closed-case calibration as described in Section 4 be performed at 2-year intervals.

TEST EQUIPMENT 3-2.

Table 3-1 lists the recommended test equipment to use for the performance tests, adjustment procedures, and for troubleshooting the Signal Generator. A two-turn loop is shown in Figure 3-1.

Table 3-1. Recommended Test Equipment

INSTRUMENT NAME	MINIMUM REQUIREMENT	MANUFACTURER DESIGNATION	NOTES 1
DVM	5 1/2-Digit, 0.3% DC to 20 kHz	JF 8840A-09	A,P
DMM	3 1/2-Digit, 1% DC and 1 kHz	JF 8020B	A,P,T
RMS Voltmeter	10 Hz to 20 MHz, low noise	JF 8922A	
Wideband Amplifier	> 25-dB gain, 0.1 to 1300 MHz NF < 9 dB.	HP 8447D-010	P
RF Spectrum Analyzer	0.1 to 1.7 GHz, 100 Hz BW	HP 8568A	P,T
Oscilloscope	Four-trace 300 MHz, 5-mV/div	TEK 2465-11	T,P
FET Probe	DC to 900 MHz	TEK 6201	T
500Ω Probe	DC to 3.5 GHz, 10X	TEK P6156	T,A
RF Voltmeter	0.01 to 700 MHz, 0.01 to 3V +/-10%	HI RF 801	T 2
Frequency Counter	0.1 to 1050 MHz; 10 Hz res; 0.1V	JF 7220A	A,P,T
Modulation Analyzer	Input: 0.15 to 1300 MHz, 0 to +20 dBm AM: 10 to 90%, +/-1% FM: 0.1 to 100 kHz dev +/-1% External LO capability	HP 8901A w/Option -003	A,P,T
Distortion Analyzer	1 to 10% range, +/-1 dB, 0.4 and 1 kHz	HP 339B	A,P,T
Power Meter	Instrumentation accuracy < +/-1%	HP 436A	A,P,T
Power Sensor (High Level)	-30 to 20 dBm; VSWR < 1.2 for 0.4 to 1 MHz, < 1.1 for 1 to 2000 MHz, < 1.3 for > 2000 MHz	HP 8482A	
Power Sensor (Low Level)	-67 to -20 dBm; VSWR < 1.4 for 10 to 30 MHz < 1.15 for 30 to 2100 MHz	HP 8484A	
Attenuator, 60, 13 dB	0.1 to 2100 MHz VSWR < 1.15	Narda 777C	P 4
LF Synthesized Signal Generator (LFSSG)	10 Hz to 11 MHz, 10 Hz steps, 1V pk, spurs and harmonics < -50 dB	JF 6011A	A,P
HF Synthesized SignalGenerator (HFSSG) (Low Residual)	0.01 to 1056 MHz	JF 6080A	P,T
Dynamic Signal Analyzer		HP 3561A	P
3-dB Hybrid	25-dB isolation 0.03 to 2.5 GHz	Anzac H-183-4	P
6-dB Resistive Combiner	DC to 2.5 GHz	Weinschel 1506A	P
Test Cable	Dual pin to BNC	JF 732891	A,T
Coaxial Adapter	50Ω Type "N" (m) to BNC(f)	JF Y9308	A,P,T
Service Adapter	50Ω Module output to SMA	JF 744177	T
Two-Turn Loop	For leakage test (See Figure 3-1)	Homebuilt	P,T 3
VSWR Bridge	10 to 2000 MHz	Wiltron 60N50	P

Table 3-1. Recommended Test Equipment (cont)

INSTRUMENT NAME	MINIMUM REQUIREMENT	MANUFACTURER DESIGNATION	NOTES 1
50Ω Termination	Type "N"	JF Y9317	P
Coaxial Cable, 50Ω	3 ft, BNC both ends	Y9111	A,P,T
Coaxial Cable, 50Ω	6 ft, BNC both ends	Y9112	A,P,T
Electric Screwdriver	Set to 7 inch-pounds torque	Jergens-CL6500/CLT50	A,T
Variable Power Supply	0 to 30V dc	Lambda	T
Measuring Receiver Set	10 to 1300 MHz	HP 8902A	P
Sensor Module	0.1 to 2600 MHz	HP 11722A	P
Pulse Generator	50-ns pulse width, 10-MHz repetition rate	HP 8012B	P
BNC Termination	50Ω	Midwest Microwave 2048M	P
Detector	3-GHz bandwidth, 5-ns rise time	Krytar D101	P
Phase Noise MeasurementSystem		HP 3048A	P
Tuning Tool	0.025-inch square drive	Johanson	

NOTES: 1. A = Adjustment; P = Performance Test; T = Troubleshooting.
2. Helper instruments.
3. Two-turn, 1-inch diameter loop made of #18 enamel wire soldered to a BNC connector.
4. VSWR verified and actual attenuation calibrated to +/-0.2 dB by the operator at application frequencies.

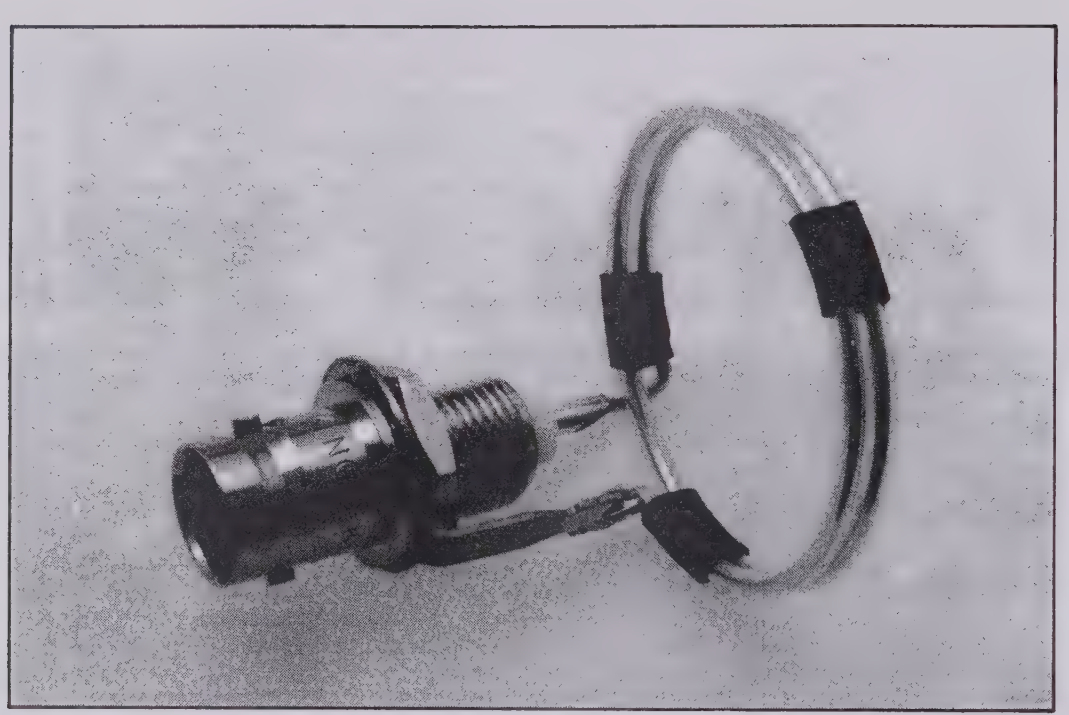


Figure 3-1. Two-Turn Loop

POWER-ON TEST 3-3.

Functional checks of the 6080A are performed by built-in self tests.

REQUIREMENT:

The Signal Generator must successfully pass the self test.

REMARKS:

Two self test routines are available. One test is the normal power-on self test (also invoked with SPCL 02), which does not allow RF power (not greater than -140 dBm) to be present at the output connector. The second test is a more complete, extended self test (invoked with SPCL 06). This extended test does allow RF levels up to -20 dBm to be present at the output connector. The normal self test begins each time the Signal Generator is turned on. Press any of the FUNCTION keys or the CRL/LCL key to abort the test.

PROCEDURE:

1. Start the test with the power off.
2. Press the POWER button on.

The Signal Generator automatically starts the self tests. This 5-second test includes lighting all indicators and every segment of the display.

If the instrument fails any of the self tests, failure codes appear in the four display fields. See Appendix E for an interpretation of the self test status codes.

If the Signal Generator passes the self tests, it automatically returns to the default state.

3. Begin the extended self test by entering SPCL 06.

The Signal Generator automatically starts the self tests. This 5-second test includes lighting all indicators and every segment of the display.

If the instrument fails any of the self tests, failure codes appear in the four display fields. See Appendix E for an interpretation of self test status codes.

If the Signal Generator passes the extended self tests, it automatically returns to the default state.

FREQUENCY ACCURACY TEST 3-4.

The internal time base is compared to a frequency standard.

REQUIREMENTS:

The frequency of the UUT time base is within the specified limits.

TEST EQUIPMENT:

- Frequency standard
- Frequency counter

PROCEDURE:

1. Connect the frequency standard output to the 10 MHZ REF IN connector on the frequency counter and switch the counter to EXT REF.
2. Switch the UUT to internal reference.
3. Connect the UUT REF OUT connector to the frequency counter CHANNEL A input connector.
4. Verify that the counter displays 10 MHz ±10 Hz.

SYNTHESIS TEST 3-5.

A frequency counter operating on a common reference with the Signal Generator measures the output frequency of the Signal Generator at several programmed frequencies.

REQUIREMENT:

The Signal Generator's measured and programmed frequencies agree within ±1 count.

TEST EQUIPMENT:

- Frequency counter

REMARKS:

If the UUT fails this test, the frequency synthesis circuitry is probably at fault.

PROCEDURE:

1. Connect the UUT 10 MHZ OUT to the frequency counter 10 MHZ REF IN, and connect the UUT RF OUTPUT to the frequency counter input.
2. Set the UUT REF INT/EXT switch to INT.
3. Program the UUT to RCL 98.
4. Program the UUT frequency to 111.111111 MHz.
5. Program the UUT frequency step to 111.111111 MHz.
6. Verify that the reading on the frequency counter agrees with the UUT frequency ±1 count as the frequency is stepped from 111.111111 to 999.999999 MHz.

HIGH-LEVEL ACCURACY TEST 3-6.

The output power is measured using a power meter at various frequencies. First the step attenuator is set for zero attenuation, then each attenuator section is individually programmed. Finally, the output level accuracy and attenuator section errors are computed.

If a measuring receiver is available for level testing, proceed directly to the "Alternate Level Accuracy Test" further on in this section.

TEST EQUIPMENT:

- Power meter
- Power sensor (high level)

REQUIREMENT:

The output level accuracy, the attenuator section errors, and the sum of the attenuator section errors at each test frequency are:

$<\pm 2.0$ dB from 0.1 to 0.4 MHz MHz
$<\pm 1.0$ dB from 0.4 to 1056 MHz

REMARKS:

If the UUT fails this performance test, it requires calibration or repair. Possible problem areas (if no power-on status codes are present) include the A8 Output PCA, the A21 Attenuator PCA, or the A7 Relay Driver PCA.

The test frequencies of this procedure provide reasonable confidence of the amplitude accuracy of the UUT. However, additional test frequencies may be included in this test.

This test verifies the high-level accuracy of the Signal Generator and checks that the amplitude correction factors for the individual attenuator sections are correct. This high-level test, in conjunction with the mid-level accuracy and low-level accuracy tests, verifies the overall level performance of the UUT. If a measuring receiver is available, you can skip to the Alternate Level Accuracy Test, which can be used instead of the following high-level, mid-level, and low-level accuracy tests.

NOTE

To test attenuator sections 4 through 7, program the 6080A Signal Generator to -12 dBm, and activate Special Functions SPCL 923 through SPCL 926, respectively.

PROCEDURE:

1. Calibrate and zero the power meter.

2. Program the UUT to RCL 98.

3. Connect the power sensor to the UUT RF OUTPUT.

4. Program the UUT to the levels and frequencies shown below, and verify that the errors are less than ±1 dB.

LEVEL	FREQUENCY
+19 dBm	0.4, 1, 5, 14, 20, 40, 80, 160, 320, 511.999999 MHz
+17 dBm	512, 550, 640, 700, 850, 950, 1056 MHz

5. Program the UUT frequency to 0.1 MHz and +12 dBm.

6. Select each attenuator section by programming the UUT amplitude to the levels shown in Table 3-2 and by using SPCL 923 through SPCL 926, and record the measured power at each level.

7. Compute the output power error for each programmed level of Table 3-2 by subtracting the programmed power in dBm from the measured power in dBm. These errors must not exceed the requirement stated above.

8. Subtract the measured power for section zero from the sum of the measured power for that section plus the nominal attenuation for that section. This is done for attenuator sections 1 through 7 only. (Example, (-M0+M1+6) for section 1.) The eight section errors and their sum must not exceed the requirement. Table 3-3 shows the parameters of the high-level accuracy test.

9. Repeat steps 4 through 7 with the UUT programmed to each of the following frequencies:

   1, 5, 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, 1056 MHz

Table 3-3 is an example of this procedure in which the measured power and the error calculations are shown. This example is for one frequency, and these measurements and calculations are repeated at other frequencies. In this case, the section errors and the sum of the section errors are within the test limits; therefore, the unit passed the high-level accuracy test.

Table 3-2. High-Level Accuracy Test Conditions

ATTENUATION		OUTPUT POWER		ERROR (dB)	SECTION ERROR (DB)	LIMIT (dB)
SECTION	NOMINAL	PROGRAMMED LEVEL (dBm)	MEASURED POWER (dBm)			
0	0	+12	M0	M0-12	M0-12	see test require-ments
1	6	+6	M1	M1-6	-M0+M1+6	
2	12	0	M2	M2-0	-MO+M2+12	
3	24	-12	M3	M3-12	-M0+M3+24	
4	24	-12	M4	M4-12	-M0+M4+24	
5	24	-12	M5	M5-12	-M0+M5+24	
6	24	-12	M6	M6-12	-M0+M6+24	
7	24	-12	M7	M7-12	-M0+M7+24	
					Sum of Errors	

Table 3-3. Sample High-Level Accuracy Test Conditions

ATTENUATION		OUTPUT POWER		ERROR (dB)	SECTION ERROR (dB)	LIMIT (dB)
SECTION	NOMINAL	PROGRAMMED LEVEL (dBm)	MEASURED POWER (dBm)			
0	0	+12	+12.2	+0.2	+12.2-12.0	= +0.2
1	6	+6	+05.9	-0.1	-12.2+5.9+6	= +0.3
2	12	0	-00.1	-0.1	-12.2-0.1+12	= -0.3
3	24	-12	12.1	-0.1	-12.2-12.1+24	= -0.3
4	24	-12	11.8	+0.2	-12.2-11.8+24	= +0.0
5	24	-12	12.0	+0.0	-12.2-12.0+24	= -0.2
6	24	-12	12.1	-0.1	-12.2-12.1+24	= -0.3
7	24	-12	11.9	+0.1	-12.2-11.9+24	= -0.1
					Sum of Errors	= -0.7

MID-LEVEL ACCURACY TEST 3-7.

The level accuracy is verified using a power meter with a low-level power sensor. This verification is done from -24 to -66 dBm at frequencies of 10, 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

REQUIREMENT:

Amplitude accuracy is:

< ±1.0 dB from 10 to 1056 MHz

TEST EQUIPMENT:

- Power meter
- Power sensor (low level)

REMARKS:

The mid-level accuracy test, in conjunction with the high-level and low-level accuracy tests, verifies the overall level performance of the UUT.

If the UUT fails this test after passing the high-level accuracy test, problems with the A21 Attenuator PCA or the A7 Relay Driver PCA are indicated.

Use the UUT RF OUTPUT ON/OFF control when zeroing the power meter.

PROCEDURE:

1. Program the UUT to RCL 98, 10 MHz, and -24 dBm.
2. Calibrate the power meter.
3. Zero the power meter.
4. Connect the power meter and power sensor to the UUT RF OUTPUT.
5. Measure the UUT output power (in dBm) with the power meter. The output should agree with the programmed level in the requirement.
6. Repeat step 5 for levels of -30, -36, -42, -48, -54, -60, and -66 dBm.
7. Repeat steps 5 and 6 for frequencies of 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

LOW-LEVEL ACCURACY TEST 3-8.

An RF spectrum analyzer and amplifier are used to verify the UUT level accuracy at -127 dBm and -140 dBm at frequencies of 10, 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

REQUIREMENT:

Amplitude accuracy is:

< ±1.0 dB from 10 to 1056 MHz for levels to -127 dBm.
< ±3.0 dB from 10 to 1056 MHz for levels between -127 dBm and -140 dBm.

TEST EQUIPMENT:

- 0.1 to 1300 MHz amplifier
- 60-dB attenuator
- 13-dB attenuator
- RF spectrum analyzer
- Power meter
- Power sensor (low level)

REMARKS:

This test, in conjunction with the mid-level and high-level accuracy tests, verifies the overall level performance of the UUT.

If the UUT fails this test after passing the high-level accuracy test and the mid-level accuracy test a problem in the A21 Attenuator PCA, the A7 Relay Driver PCA, or a leak-around problem in the attenuator assembly is indicated. The problem may be caused by loose or broken connections, loose screws, damaged or misplaced gaskets, or a broken feedthrough filter.

Use the UUT RF OUTPUT ON/OFF control when zeroing the power meter.

PROCEDURE:

1. Program the UUT to RCL 98, 10 MHz, and -67 dBm.

2. Calibrate the power meter (with its low-level power sensor) and connect it to the UUT RF OUTPUT.

3. Zero the power meter.

4. With the power meter, measure the UUT output power (in dBm) and record the measurement as the variable P.

5. Connect the UUT RF OUTPUT through the 60-dB attenuator and connect the 0.1 to 1300 MHz amplifier to the input of the RF spectrum analyzer. Use well shielded cables to avoid leakage that could affect the measurement.

6. Adjust the RF spectrum analyzer to display the signal, using a resolution bandwidth of 1 kHz and a vertical display of 1 dB/div.

7. Adjust the reference level so that the response is at a convenient reference point on the display (e.g., 2 dB below top scale). This signal response corresponds to a level of (P-A) dBm, where A is the value of the 60-dB attenuator.

8. Program the UUT to a level of -127 dBm, remove the 60-dB attenuator, and note the difference in the resulting response on the RF spectrum analyzer from the previous response (P-A). The actual UUT output level is (P-A) plus this difference and should agree with the programmed level within the test parameter requirements.

9. Repeat steps 1 through 8 adding another 13-dB attenuator (total 73 dB) to the UUT RF OUTPUT, and dial the Signal Generator level to -140 dBm. It may be necessary to reduce the spectrum analyzer resolution bandwidth.

10. Repeat steps 1 through 9 for frequencies of 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

ALTERNATE LEVEL ACCURACY TEST 3-9.

A measuring receiver is used to verify the UUT level accuracy at various amplitude and frequency settings that test all level ranges of the UUT on all RF bands.

REQUIREMENTS:

Amplitude accuracy is:

<±1 dB from 0.1 to 511.999999 MHz from +19 to 0 dBm
<±1 dB from 512 to 1056 MHz from +17 to 0 dBm
<±1 dB from 2.5 to 1056 MHz from 0 to -127 dBm

TEST EQUIPMENT:

- Measuring receiver
- Sensor module

REMARKS:

This alternate level accuracy test is a more comprehensive test then the high-level, mid-level, and low-level accuracy tests. It takes the place of those tests and is intended for those with a measuring receiver available.

If the UUT fails this test, the UUT must be calibrated or repaired.

If the UUT fails this test at higher levels, problems with the A8 Output PCA, the A21 Attenuator PCA, or the A7 Relay Driver PCA may be indicated.

If the UUT fails this test at lower levels, a problem with the A21 Attenuator PCA, the A7 Relay Driver PCA, or an RF-leakage problem with the attenuator assembly is probably indicated. The problem may be caused by loose or broken connections, loose screws, damaged or misplaced gaskets, or a broken feedthrough filter.

Because of operational subtleties in measuring receivers and with the intent of reducing the risk of measurement errors, the following procedure is written specifically for the HP 8902A as the receiver and refers to its front-panel controls and displays throughout.

NOTE

The calibration factors for the sensor module must be stored into the measuring receiver's "Cal Factor" table prior to performing calibrated RF power measurements. Correctly entered cal factors can be verified on the HP 8902A by using special functions 37.5 and 37.6. (Refer to the HP 8902A Owner's Manual.)

PROCEDURE (Level Measurements):

1. Perform the power meter "zero" and "self-calibration" for the measuring receiver. (Refer to the HP 8902A Owner's Manual.)

2. Connect all instruments as shown in Figure 3-2.

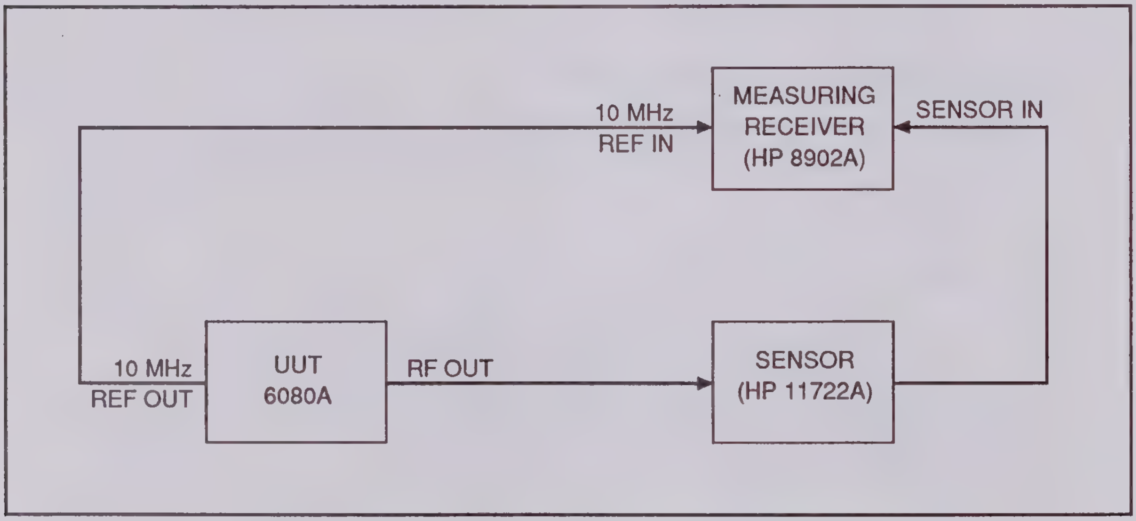


Figure 3-2. Alternate Level Accuracy Test Equipment Setup

3. Program the UUT to RCL 98 then set levels and frequencies as below and verify that there are no errors greater than ±1 dB.

LEVEL	FREQUENCY
+19 dBm	0.1, 1, 5, 14, 20, 40, 80, 160, 320, 511.999999 MHz
+13 dBm	same
+6.9 dBm	same
+0 dBm	same
+17 dBm	512, 550, 640, 700, 850, 950, 1056 MHz
+13 dBm	same
+6.9 dBm	same
+0 dBm	same

4. Program the UUT to RCL 98, 2.5 MHz, +0.8 dBm, and AMPL STEP 6.1 dB.

5. Program the measuring receiver to RF-POWER mode, and toggle the LOG/LIN button to display dBm. To enable the correct cal factor selection, tune the internal LO. on the measuring receiver to that of the UUT RF OUTPUT (2.5 MHz for the first frequency).

6. Step the UUT level from +0.8 dBm to -11.4 dBm using the STEP [v] key. Verify that each level measured with the measuring receiver agrees with the UUT programmed level and is within ±1.0 dB.

7. Select TUNED-RF LEVEL on the measuring receiver, wait for a displayed reading, then press the CALIBRATE button. Verify that the Recal annunciator goes out and a stable reading is displayed again.

8. Step the UUT from -11.4 to -127.3 dBm, again observing that each stepped level is within ±1.0 dB.

NOTE

When the Recal annunciator on the measuring receiver lights while stepping through UUT levels, press the CALIBRATE button on the measuring receiver and wait for a stable reading.

9. Repeat steps 5 through 8 for each of the following UUT frequencies:

   5, 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz

FLATNESS TEST 3-10.

A power meter and sensor are used to verify the high level flatness of the Signal Generator.

REQUIREMENT:

Amplifier flatness is:

$<$ ±0.75 dB at +10 dBm over the frequency range of 0.1 to 1056 MHz.

TEST EQUIPMENT:

- Power meter
- Power sensor (high level)

REMARKS:

If the UUT fails this test, calibration or repair is necessary. If no power-on status codes are present, likely problem areas needing repair include the A8 Output PCA, the A21 Attenuator PCA, or the A7 Relay Driver PCA.

PROCEDURE:

1. Calibrate and zero the power meter.

2. Connect the power sensor to the Signal Generator RF OUTPUT.

3. Program the UUT to RCL 98 and then to 0.1 MHz and +10 dBm.

4. Verify that the power meter reads +10 ±0.75 dBm.

5. Repeat step 4 for the following frequencies:

   a. 0.2 to 2.0 MHz in 0.1 MHz steps
   b. 2.0 to 20.0 MHz in 1.0 MHz steps
   c. 20.0 to 200.0 MHz in 10.0 MHz steps
   d. 200.0 to 1056.0 MHz in 20.0 MHz steps

OUTPUT LEAKAGE TEST 3-11.

The output signal leakage is verified using a 1-inch diameter, two-turn loop as shown in Figure 3-1. The induced signal is measured with an RF spectrum analyzer and compared to a 0.5-μV reference established at each reference frequency. The two-turn loop must be 1 inch away from any surface of the UUT.

REQUIREMENT:

Radiated emissions induce <0.5 μV of the Signal Generator's output signal.

TEST EQUIPMENT:

- 0.1- to 1050-MHz amplifier
- RF spectrum analyzer
- Two-turn loop
- 50Ω Type "N" termination
- Screen room, depending on the RF environment

REMARKS:

If the UUT fails this test, possible problems include a broken feedthrough filter, loose or broken connections, loose screws, damaged or misplaced gaskets.

PROCEDURE:

1. Connect the UUT RF OUTPUT to the 0.1 to 1300 MHz amplifier input, and connect the amplifier output to the RF spectrum analyzer input. Use well shielded cables to avoid leakage that could affect the measurement.

2. Program the UUT to RCL 98.

3. Program the UUT to 9 MHz and -113 dBm. (0.5 μV).

4. Adjust the RF spectrum analyzer to display the UUT signal for a convenient reference. Make this adjustment using a vertical scale of 10 dB/div, a resolution bandwidth of 3 kHz, and a span/div of 5 kHz/div.

5. Disconnect the 0.1 to 1300 MHz amplifier from the UUT and terminate UUT output with the 50Ω Type "N" termination.

6. Connect the two-turn loop to the 0.1 to 1300 MHz amplifier input.

7. Program the UUT to +13 dBm.

8. Verify that the leakage indicated by the RF spectrum analyzer is less than -113 dBm (0.5 μV) by moving the two-turn loop over the UUT surface at a distance of 1 inch.

9. Repeat steps 3 through 8 at 14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

HARMONIC AND LINE-RELATED SPURIOUS TEST 3-12.

The Harmonic and Line-Related Spurious Test uses an RF spectrum analyzer to compare the level of the harmonic signal and close-in spurious signals to the desired signal at various programmed frequencies.

REQUIREMENTS:

- RF harmonics: <-30 dBc for levels <= +13 dBm.
- Power line spurious signals: -56 dBc (signals within 10 kHz of carrier)

TEST EQUIPMENT:

- RF spectrum analyzer

PROCEDURE:

1. Connect the UUT RF OUTPUT to the RF spectrum analyzer input.

2. Connect the RF spectrum analyzer 10 MHz output to the UUT 10 MHz input, and set the UUT to EXT REF.

3. Program the UUT to RCL 98.

4. Program the UUT to +13 dBm and 10 kHz.

5. Set the RF spectrum analyzer controls to display the UUT output signal and its harmonics (at least three harmonics wherever possible). Be careful not to overload the analyzer input. Overloading the RF spectrum analyzer causes it to generate harmonics, thus invalidating the test.

6. Verify that all the harmonics are more than 30 dB below the fundamental signal.

7. Verify that all the harmonics are more than 30 dB below the fundamental signal for the following frequencies:

   14, 20, 40, 80, 160, 320, 550, 640, 700, 850, 950, and 1056 MHz.

8. Set the RF spectrum analyzer to display the UUT output signal with a 2-kHz span and 10-Hz resolution. Verify that all spurious signals are below -56 dBc for the frequencies listed in step 7.

9. Set the RF spectrum analyzer to display the UUT output signal with a 50-kHz span and 30-Hz resolution. Verify that all spurious signals within 10 kHz of the carrier are below -56 dBc for the frequencies listed in step 7.

NON-HARMONIC SPURIOUS SIGNALS TEST USING RF SPECTRUM ANALYZER 3-13.

REQUIREMENTS:

Non-harmonic spurious signals <-100 dBc for offsets greater than 500 kHz.

TEST EQUIPMENT:

- RF spectrum analyzer

REMARKS:

An RF spectrum analyzer cannot be relied on to make -100 dBc spurious signal measurements, because analyzers generate internal spurious signals above -100 dBc at a variety of RF output frequencies. A way around this is to use the spectrum analyzer in a cohered narrow span, with the spectrum analyzer reference level set 20 dB off scale. This causes the 50-dB reference line to be at -70 dBc, thereby obtaining a noise floor of -110 dBc. In this way you can measure spurious signals at the -100 dBc level at offsets greater than approximately 500 kHz from the carrier.

PROCEDURE:

1. Connect the UUT RF OUTPUT to the RF spectrum analyzer input.
2. Connect the RF spectrum analyzer 10 MHz output to the UUT 10 MHz input. Set the UUT to EXT REF.
3. Program the UUT to RCL 98.
4. Program the UUT to +16 dBm, 14.9 MHz.
5. Program the RF spectrum analyzer to 5.5 MHz, reference level to -14 dBm, span to 10 kHz. Verify that the spurious signal in the center of the screen is below -100 dBc, which is more than 80 dB down from the top of the screen.
6. Program the RF spectrum analyzer and UUT to the frequencies listed in Table 3-4, and verify that the spurious signal in the center of the screen is below -100 dBc.

PHASE NOISE, RESIDUAL FM, AND SPURIOUS SIGNALS TEST 3-14.

Verify spurious signals (between 10 and 100 kHz offset) and phase noise by using a LO (HFSSG) and an RF mixer to cancel the carrier, providing a zero difference beat frequency. Examine this frequency for spurious signals and phase noise on a low-frequency dynamic signal analyzer.

REQUIREMENT:

Spurious signals are <-100 dBc for offsets greater than 10 kHz of the carrier.

Phase Noise: as listed in Table 3-5.

Residual FM: as listed in Table 3-6.

Table 3-4. Spurious Signal Test Frequencies

UUT FREQUENCY (MHz)	RF SPECTRUM ANALYZER FREQUENCY (MHz)
14.9	9.40
14.9	20.4
10.111111	10.999
11	13
11	20
11	80
11	91
527.91	528.54
536.11	536.66
538.76	539.32
540.65	541.20
542.08	542.72
615.93	616.49
703.93	704.56
792.07	792.63
880.07	880.70
968.07	968.77
896.01	912.03
896.01	904.02
1024	936
1024	944
1024	1029

Table 3-5. Phase Noise Requirements

CARRIER FREQUENCY BAND (MHz)	OFFSET FREQUENCY		
	1 kHz (dBc/Hz)	20 kHz (dBc/Hz)	100 kHz (dBc/Hz)
512 to 1056	-94	-131	-138
256 to 512	-100	-136	-142
128 to 256	-106	-141	-144
64 to 128	-112	-144	-145
32 to 64	-118	-144	-146
15 to 32	-124	-145	-146
0.01 to 15	-112	-138	-138

Table 3-6. Residual FM Requirements

APPROXIMATE CARRIER FREQUENCY BAND (MHz)	POST-DETECTION BANDWIDTH	
	0.3 kHz TO 3 kHz (CCITT) Hz RMS	0.5 kHz TO 15 kHz Hz RMS
512 to 1056	1.5	2.0
256 to 512	0.7	1.0
128 to 256	0.4	0.5
0.1 to 128	0.2	0.4

TEST EQUIPMENT:

- HP 3048A Phase Noise Test Set
- Fluke 6080A Signal Generator (HFSSG)

REMARKS:

The following tests use the HP 3048A Phase Noise Test Set and an additional 6080A Signal Generator to measure phase noise and spurious signals. The phase noise is specified at a 20-kHz offset, and the spurious signals are specified for greater than a 10-kHz offset.

By using two presumably identical generators, the measured phase noise is 3 dB higher than each individual generator, and the measured spurious signals could be as much as 6 dB higher than each individual generator. If the measured results are within specification, both reference and UUT are within specification individually. If the measured results are out of specification, it is difficult to determine whether the reference or the UUT is out of specification without using a third 6080A. Alternatively, by using a reference generator with much better specified phase noise than the 6080A, the ambiguity can be reduced.

The following procedure assumes that you are familiar with the operation of the HP 3048A Phase Noise Test Set. The procedure outlines setting up the system and entering various test parameters. Refer to the HP 3048A instruction manual for more information.

PROCEDURE:

1. Configure the system as described in Appendix A of the HP 3048A instruction manual.

2. Load the system software as described on pages A-10 through A-11 of the HP 3048A instruction manual. The screen should show HP3048A PHASE NOISE SYSTEM MAIN SOFTWARE LEVEL. This screen is subsequently referred to as the main menu.

3. Connect the equipment as shown in Figure 3-3.

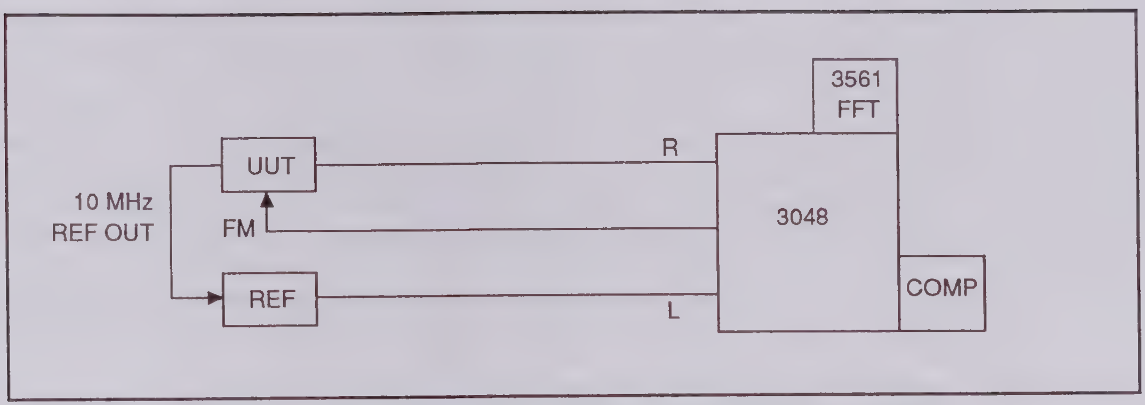


Figure 3-3. Phase Noise and Non-Harmonic Spurious Test Setup

4. Set the reference 6080A (L input) to 1056 MHz, +17 dBm, external reference.

5. Set the UUT 6080A (R input) as follows:

   a. Frequency 1056 MHz
   b. Amplitude +10 dBm
   c. FM 2 kHz
   d. EXT DC FM

NOTE

Warm up both the UUT and reference 6080A for at least 2 hours.

6. Select System Config. Menu. Using the Delete Instr. softkey, delete all instruments except the FFT ANALYZER and INTERFACE. Select DONE to return to the main menu. Be sure the address on the HP 3561 is the same as in the menu on the display.

7. In the main menu select Define Msrmnt. In the menu that appears, select Type/Range. It is not necessary to change any parameters, so select DONE.

8. Select Instr. Params. In the menu that appears, set the carrier frequency to 1.056E9 Hz, set Detector/Discr., set Input Frequency to 1.056E9 Hz, VCO Tuning Constant to 2000 Hz/V, Center Voltage of VCO Tuning Curve 0V, Voltage Tuning Range of VCO ±1V, VCO Tune-port Input Resistance to 600Ω. Phase Detector - Internal Phase Detector: 5 MHz to 1600 MHz. Select DONE to return to the Measurement Definition Menu.

9. Select Calibr Process. In this menu select Measure the Detector Constant, Compute from expected T. Constant, and The PLL Suppression WILL be verified by using the appropriate softkey. Select DONE to return to the Measurement Definition Menu.

10. Select Source Control. In this menu select DUT: USER'S SRCE SYSTEM CONTROL (then select CONTROL and this should change to DUT: USER'S SRCE MANUAL CONTROL), REF SOURCE: USER'S SRCE MANUAL CONTROL, TUNE VOLTAGE line to DUT, by using the appropriate softkey. Select DONE to return to the Measurement Definition Menu.

11. Select Define Graph. Change the title as appropriate. Select DONE to return to the Measurement Definition menu. Select DONE to return to the main menu.

12. To start the measurement, select New Msrmnt. Select Yes. Proceed to verify this is a new measurement. After the diagram of the setup appears on the screen, turn UUT DCFM off, then turn it on again, and select Proceed. The measurement is complete when a phase noise plot appears on the screen. To accurately measure the phase noise at 20-kHz offset, select Other Keys, then select Marker ON/OFF (which should turn the marker on). Use the knob on the keyboard to position the marker at 20 kHz. The phase noise should be below -130 dBc/$\sqrt{\text{Hz}}$ assuming the reference and UUT 6080A are identical. All spurs >10 Hz offset should below -100 dBc. All spurs <10 kHz offset should be below -56 dBc.

    Generate a spur list, as necessary, by selecting Computd Outputs, Spur List, List Spurs, Next Page.

    If you are not measuring residual FM or ϕM, select DONE three times to return to the main menu.

    Repeat for output frequencies: 14, 31, 63, 127, 255, and 511 MHz. Use appropriate specs for band.

13. Residual FM or ϕM is measured from the Computd Outputs Menu. If measuring residual FM or ϕM after the Spur List, select DONE, then select Integr. Noise.

    To verify that residual FM meets the requirements in Table 3-6, select Data Type Snu (f) and input Start Freq. 300 Hz, Stop Freq. 3000 Hz. Select Eval. Intgrl.

    Repeat for Start Freq. 50 Hz, Stop Freq. 15E3 Hz. The residual FM should meet the requirements in Table 3-6. Repeat for output frequencies: 14, 31, 63, 127, 255, and 511 MHz. Use appropriate specs for band.

RESIDUAL AM NOISE TEST 3-15.

Use the HP 3048A Phase Noise Test Set and an additional AM detector to measure the residual AM noise. The procedure assumes that you are familiar with the operation of the HP 3048A Phase Noise Test Set. The following procedure outlines setting up the system and entering various test parameters. Refer to the HP 3048A instruction manual for more information.

REQUIREMENT:

Residual AM: <0.01% of 50 Hz to 15 kHz post-detection bandwidth.

TEST EQUIPMENT:

- HP 3048A Phase Noise Test Set
- HP 8472 AM detector, polarity negative (or equivalent)
- Narda 4780-3, 3-dB pad (or equivalent)
- 300 μF, 6V (or greater), tantalum electrolytic capacitor
- 1000Ω, 1%, ⅛ W, metal film resistor

PROCEDURE:

1. Configure the system as described in Appendix A of the HP 3048A instruction manual.

2. Load the system software as described on pages A-10 through A-11 of the HP 3048A instruction manual. The screen should show HP3048A PHASE NOISE SYSTEM MAIN SOFTWARE LEVEL (main menu).

3. Connect the equipment as shown in Figure 3-4.

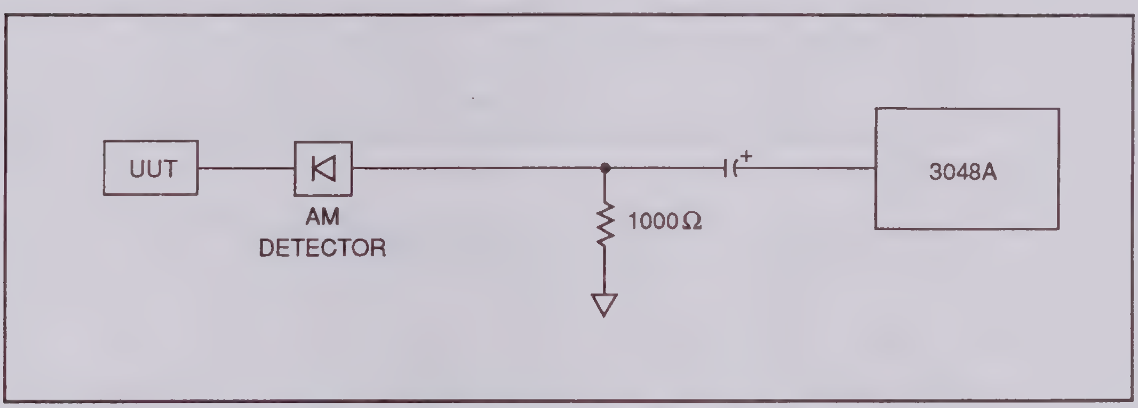


Figure 3-4. Residual AM Noise Test Connection Diagram

4. Set the UUT 6080A as follows:

   a. Frequency 1056 MHz
   b. Amplitude +7 dBm

NOTE

Warm up both the UUT and reference 6080A for at least 2 hours.

5. Select System Config. Menu. In this menu delete all instruments except the FFT ANALYZER and INTERFACE. Return to the main menu by selecting DONE. Be sure the address on the HP 3561 is the same as in the menu on the display.

6. In the main menu select Define Msrmnt. In this menu select Type/Range. Select AM Noise using Next Type softkey. Select DONE to return to Measurement Definition Menu.

7. Select Instr. Params. In this menu, set the carrier frequency to 1.056E9 Hz, Detector/Discr. Set Input Frequency to 1.056E9 Hz. Use Select Detect to select External Phase/AM Detector softkey. Select DONE to return to the Measurement Definition Menu.

8. Select Calibr Process. In this menu Use Next Method softkey to select Derive From Double Sided Spur. Enter Amplitude -40 dBc, Frequency 10E3 Hz. Select DONE to return to the Measurement Definition Menu.

9. Select Source Control. In this menu, use the appropriate softkey to select DUT: USER'S SRCE MANUAL CONTROL, AM DETECTOR USER'S DEV. MANUAL CONTRL., and CAL SOURCE USER'S SRCE MANUAL CONTRL. Select DONE to return to the Measurement Definition Menu.

10. Select Define Graph. Change the title as appropriate. Selecting DONE to return to the Measurement Definition Menu. Select DONE to return to the main menu.

11. To start the measurement, select New Msrmnt. Select Yes, Proceed to verify this is a new measurement. After the diagram of the test setup appears on the screen, select Proceed.

    When instructed to Apply Calibration spur to carrier, set the UUT to AM 2%, MOD FREQ 10 kHz, and INT AM.

    When instructed to Remove calibration spur, press INT AM on the UUT (this turns off internal AM). The measurement is complete when a noise plot appears on the screen.

    Select Other Keys, Computd Outputs, then Integr. Noise. Data Type should be L (f). Enter 50 Hz for Start Freq. and 15E3 Hz for Stop Freq.

    Select Eval Intgrl. The noise should be below -80 dBc (.01%).

    Select DONE three times to return to the main menu.

12. Change UUT to 14 MHz. Select Define Msrmnt, then Instr. Params. Change both Carrier Frequency and Detector/Discr. Input Frequency to 14E6. Return to main menu.

13. To start the measurement select New Msrmnt. When instructed to Apply calibration spur to carrier, set the UUT to AM 2%, MOD FREQ 10 kHz, and INT AM.

    When instructed to Remove calibration spur, press INT AM on the UUT (this turns off internal AM). The measurement is complete when a noise plot appears on the screen.

    Select Other Keys, Computd Outputs, the Integr. Noise. Data Type should be L(f).

    Enter 50 Hz for Start Freq. and 15E3 Hz for Stop Freq. Now select Eval Intgrl. The noise should be below -80 dBc (0.01%).

MODULATION TESTS 3-16.

The following tests use a modulation analyzer to verify modulation accuracy and incidental modulation of the UUT. The modulation distortion is verified by measuring the demodulated output of the modulation analyzer with a distortion analyzer. The internal modulation oscillator frequency is measured using a frequency counter on the modulation output. The internal modulation oscillator amplitude is measured using an rms voltmeter.

Amplitude Modulation Tests 3-17.

REMARKS:

If the UUT fails these performance tests, calibrate and/or repair the associated circuitry.

The UUT settings in this procedure are chosen to provide strong confidence in the modulation performance of the UUT throughout its range; however, you can also check the performance at other instrument settings.

TEST EQUIPMENT:

- Modulation analyzer
- Distortion analyzer
- Low-frequency synthesized signal generator (LFSSG)
- High-frequency synthesized signal generator (HFSSG)
- DVM

REQUIREMENTS:

AM Accuracy: ±(2% + 4% of setting), up to 90% depth, 1-kHz rate.

AM Distortion at 1-kHz rate: <1.5%, 0-30% depth, <3%, 30-70% depth, <5%, 70-90% depth.

AM 3 dB Bandwidth: 20 Hz to 50 kHz, ac coupled, dc to 50 kHz, dc coupled.

Incidental Phase Modulation: <0.2 rad at 30% AM and 1-kHz rate.

NOTE

The following procedures must be performed in the order given to ensure that the proper equipment is connected and the appropriate programs are enabled.

PROCEDURE (Internal AM Accuracy Test):

1. Program the UUT to: RCL 98, 90% Internal am, 1-kHz rate, +10 dBm level.

2. Program the Modulation Analyzer to measure AM depth in a 0.05 to 15-kHz bandwidth.

3. Measure the mean AM depth, (+PEAK plus -PEAK)/2, using the modulation analyzer.

4. Verify that the mean AM depth is between 84.4 and 95.6%.

PROCEDURE (AM Accuracy and Distortion Test):

1. Connect the LFSSG output to the UUT MOD INPUT connector and the DVM. (Use a BNC T connector.)

2. Program the UUT for a frequency of 0.2 MHz, +10 dBm level, and EXT AM at 30% AM depth.

3. Program the LFSSG for 1 kHz at 0.7071V rms as measured by the dvm.

4. Connect the modulation output of the modulation analyzer to the input of the distortion analyzer.

5. Set the distortion analyzer to measure the THD of the 1-kHz modulation signal.

6. Verify that the mean AM depth (+PEAK plus -PEAK)/2 is between 25.5 and 34.5%.

7. Verify that the THD is less than 3%.

8. Program the remaining combinations of RF frequency, level, and am depth listed in Table 3-7. Verify that the accuracy and distortion requirements are met.

9. Repeat step 8 at a level of +4 dBm.

PROCEDURE (AM Bandwidth Test):

1. Program the UUT for 50% INT AM at 1 kHz rate at 100 MHz, and +10 dBm.

2. With the modulation analyzer reading AM%, press the RATIO DB key to normalize the reading to 0.0 dB.

3. Set the modulation frequency to 50 kHz and read the change in level in AM in dB. Verify that the reading is greater than -3.0 dB.

4. Repeat steps 1 through 3 at 14, 20, 30, 40, 60, 80, 160, 250, 320, 400, 550, 640, 700, 850, 950, and 1056 MHz.

5. Repeat steps 1 through 4 at +4 dBm.

PROCEDURE (Incidental Phase Modulation Test):

1. Program the UUT for 30% INT AM at 1 kHz, at 640 MHz, and +10 dBm.

2. Program the modulation analyzer to measure peak phase deviation in a 0.3- to 3-kHz bandwidth. Connect the HFSSG to the external Local Oscillator input.

3. Verify that the incidental phase modulation is less than 0.2 rad.

NOTE

It may be necessary to compensate for residual noise effects using the procedure presented in the manual provided with the Modulation Analyzer.

4. Repeat step 3 at frequencies of 320, 160, 80, 40, 20, and 14 MHz.

Table 3-7. AM Test Conditions

FREQUENCY (MHz)	LEVEL (dBm)	AM (%)
1056	+10	30 50 90
950	+10	30 50 90
700	+10	30 50 90
640	+10	30 50 90
550	+10	30 50 90
320	+10	30 50 90
160	+10	30 50 90
80	+10	30 50 90
40	+10	30 50 90
20	+10	30 50 90
14	+10	30 50 90

Frequency Modulation Tests 3-18.

REMARKS:

If the UUT fails these performance tests, calibrate and/or repair the associated circuitry.

The UUT settings in this procedure are chosen to provide strong confidence in the modulation performance of the UUT throughout its range; however, you can also check the performance at other instrument settings.

TEST EQUIPMENT:

- Modulation analyzer
- Distortion analyzer

REQUIREMENTS:

FM Accuracy: ±(5% of setting +10 Hz) for rates from 50 Hz to 50 kHz.

FM Distortion:

> Standard Mode: <2% for 0.5 to 1.0 times maximum deviation; <1% for <0.5 times maximum deviation. Applies for rates of 50 Hz to 50 kHz.
>
> Low Distortion Mode: <0.3% for <=3.5 kHz peak deviation and rates 0.3 to 3 kHz.

FM 3-dB Bandwidth: as listed in Table 3-8.

Incidental AM: <1% depth for deviation <100 kHz at 1 kHz rate and carrier frequency >0.5 MHz.

PROCEDURE (FM Accuracy and Distortion Test):

1. Connect the modulation analyzer to the UUT RF OUTPUT.
2. Program the modulation analyzer to measure peak FM in a 0.3- to 3-kHz bandwidth.
3. Program the UUT frequency to 640 MHz, +7 dBm, 20-kHz deviation, INT FM and 1-kHz modulation rate.
4. Set the distortion analyzer to measure distortion at 1 kHz.
5. Verify that the modulation analyzer reading is between 19 and 21 kHz, and that the THD is less than 1%. Repeat at deviations of 5 and 10 kHz. Verify that the modulation analyzer reading is within ±5% of the programmed value.
6. Program the UUT to deviations of 50, 100, and 200 kHz.
7. Verify that the modulation analyzer reading and distortion is per the requirements.

Table 3-8. FM 3 dB Bandwidth

DEVIATION	COUPLING	
	INTERNAL AC	EXTERNAL AC (DC)
0% to 25% Maximum	20 Hz to 175 kHz	20 Hz to 175 kHz
25% to 100% Maximum	20 Hz to 100 kHz	20 Hz (ac) to 100 kHz

NOTE

Change the modulation analyzer bandwidth and distortion analyzer frequency appropriately for modulation frequency for steps 8 through 16.

8. Repeat steps 4 through 7 with the modulation rate set to 100 Hz. Verify distortion only.

9. Repeat steps 4 through 7 with the modulation rate set to 50 kHz. Verify distortion only.

10. Program UUT to 40-MHz frequency, 25-kHz deviation, and 1-kHz INT modulation frequency.

11. Verify that the modulation analyzer reading and distortion is per the requirements.

12. Program the UUT to deviations of 50, 100, 200, and 250 kHz.

13. Verify that the modulation analyzer readings and distortion meet the requirements.

14. Repeat steps 10 through 13 with the modulation rate set to 100 Hz. Verify distortion only.

15. Repeat steps 10 through 13 with the modulation rate set to 50 kHz. Verify distortion only.

NOTE

It may be necessary to compensate for residual noise effects using the procedure presented in the manual provided with the Modulation Analyzer.

PROCEDURE (Incidental AM Test):

1. Program the UUT for 100-kHz deviation, INT FM on at 1 kHz, EXT FM off, a level of +7 dBm, and a frequency of 14 MHz.

2. Program the modulation analyzer to measure peak AM in a 0.3- to 3-kHz bandwidth.

3. Verify that the incidental AM is less than 1%.

4. Repeat steps 1 through 3 at frequencies of 20, 30, 40, 60, 80, 100, 160, 250, 320, 400, 550, 640, 700, 850, 950, and 1056 MHz.

PROCEDURE (FM Bandwidth Test):

1. Program the UUT to 14 MHz, +7 dBm, 1 kHz Mod Rate, INT FM, and 25% of Max Dev (125 kHz at 14 MHz).
2. Set the modulation analyzer low-pass filtering to all off, read FM Peak+, and press Ratio DB key. (Normalize the reading to 0.00 dB.)
3. Set the UUT modulation frequency to 175 kHz. Verify that the modulation meter reading is greater than -3dB.
4. Repeat steps 1 through 3 for the following frequencies: 20, 40, 100, 200, 300, and 750 MHz.
5. Repeat steps 1 through 4 with the FM deviation set at the maximum for each frequency and the modulation rate set for 100 kHz.

Phase Modulation Tests 3-19.

REMARKS:

If the UUT fails these performance tests, calibrate and/or repair the associated circuitry.

The UUT settings in this procedure are chosen to provide strong confidence in the modulation performance of the UUT throughout its range; however, you can also check the performance at other instrument settings.

TEST EQUIPMENT:

- Modulation analyzer
- Distortion analyzer

REQUIREMENTS:

Phase Modulation Accuracy: ±(5% of setting + 0.1 radian) at 1-kHz rate.

Phase Modulation Distortion: <2% for 0.5 to 1.0 times maximum deviation; <1% for <0.5 times maximum deviation. Applies for 1-kHz rate in standard mode, and from 50 Hz to 50 kHz in high rate mode.

Phase Modulation 3-dB External Bandwidth: Standard Mode: 20 Hz to 15 kHz, ac coupled; dc to 15 kHz, dc coupled. High rate mode: 20 Hz to 100 kHz, ac coupled; dc to 100 kHz, dc coupled.

Incidental AM: <1% depth for peak deviation <10 radians at 1-kHz rate and carrier frequency >0.5 MHz.

PROCEDURE (ϕM Accuracy and Distortion Test):

1. Connect the modulation analyzer to the UUT RF OUTPUT.

2. Program the modulation analyzer to measure peak ϕM in a 0.3- to 3-kHz bandwidth.

3. Program the UUT frequency to 640 MHz, +7 dBm, 20 radians, INT ϕM and 1-kHz modulation rate.

4. Set the distortion analyzer to measure distortion at 1 kHz.

5. Verify that the modulation analyzer reading is between 19 and 21 radians, and that the THD is less than 1%. Repeat at deviations of 5 and 10 radians. Verify that the modulation analyzer reading is within ±5% of programmed value. (See the following NOTE.)

NOTE

For steps 8 through 15, change the modulation analyzer bandwidth and distortion analyzer frequency appropriately for modulation frequency.

6. Program the UUT to deviations of 50, 100, and 200 radians.

7. Verify that the modulation analyzer reading and distortion is per the requirements.

8. Repeat steps 4 through 7 with the modulation rate set to 100 Hz. Verify distortion only.

9. Program the UUT to 40-MHz frequency, 2.5 radians deviation and 1-kHz INT modulation frequency.

10. Verify that the modulation analyzer reading is between 2.375 and 2.625 and that the distortion is less than 5%.

11. Program the UUT to deviation of 5, 10, 20, and 25 radians.

12. Verify that the modulation analyzer readings and the distortion meets the requirements.

13. Repeat steps 9 through 12 with the modulation rate set to 100 Hz. Verify distortion only.

NOTE

It may be necessary to compensate for residual noise effects using the procedure presented in the manual provided with the modulation analyzer.

PROCEDURE (Incidental AM Test):

1. Program the UUT for 10 radians deviation, INT ϕM on, 1 kHz mod rate, EXT ϕM off, a level of +7 dBm, and a frequency of 14 MHz.

2. Program the modulation analyzer to measure peak AM in a 0.3- to 3-kHz bandwidth.

3. Verify that the incidental AM is less than 1%.

4. Repeat steps 1 through 3 at frequencies of 20, 30, 40, 60, 80, 100, 160, 250, 320, 400, 550, 640, 700, 850, 950, and 1056 MHz.

PROCEDURE (ϕM Bandwidth Test):

1. Program the UUT to: 14 MHz, +7 dBm, 1 kHz mod rate, INT ϕM, and 25% of maximum deviation (12.5 radians at 14 MHz).

2. Set the modulation analyzer low-pass filtering to all off, read ϕM Peak+, press the Ratio ϕM key (normalize reading to 0.00 dB).

3. Set the UUT modulation frequency to 15 kHz. Verify that the modulation meter reading is greater than -3 dB.

4. Repeat steps 1 through 3 for frequencies: 20, 40, 100, 200, 300, and 750 MHz.

Internal Modulation Oscillator Tests 3-20.

REMARKS:

If the UUT fails these performance tests, calibrate and/or repair the associated circuitry.

The UUT settings in this procedure are chosen to provide strong confidence in the modulation performance of the UUT throughout its range; however, you can also check the performance at other instrument settings.

TEST EQUIPMENT:

- Oscilloscope
- Distortion analyzer
- Frequency counter
- RMS voltmeter

REQUIREMENTS:

Modulation Frequency Accuracy: same as reference ±7 mHz. Output Level Accuracy: ±(4% +15 mV) for rates <100 kHz, sinusoidal waveform. Sinusoidal Distortion: <0.15% for rates <20 kHz and level >0.2V pk.

PROCEDURE (Frequency):

1. Set the 6080A to internal AM modulation with 50% depth and 100 kHz RF output frequency.

2. Set the modulation oscillator frequency to 10 kHz.

3. Use an oscilloscope to observe both the RF output signal and the modulation output signal on two channels.

   Trigger the oscilloscope with the source. Verify that the modulation envelope appears coherent with the modulation frequency. That is, the RF signal is clearly visible within the modulation envelope (synchronized with the modulation signal).

PROCEDURE (Distortion):

1. Connect a 600Ω load to the UUT MOD OUTPUT connector.
2. Set the internal modulation oscillator to sine wave output at 2V peak and to the desired output frequency.
3. Connect the distortion analyzer, oscilloscope and rms voltmeter in parallel with the load resistor.
4. Connect the distortion analyzer to measure distortion with its low pass filter set to a frequency at least four times higher than the set modulation frequency.
5. Measure the distortion.
6. Repeat the above measurements for various modulation frequencies within the specified range.

PROCEDURE (Level):

1. Using the JF 8922A rms voltmeter with a 600Ω termination, verify that the level of the modulation output is within the above specification.
2. Repeat the above for various frequencies and output level settings.

VOLTAGE STANDING-WAVE RATIO (VSWR) TESTS 3-21.

The Voltage Standing-Wave Ratio (VSWR) tests use a VSWR bridge and a spectrum analyzer to verify VSWR of the UUT.

REQUIREMENTS:

The output VSWR is less than 1.5:1 for output levels < +6 dBm; < 2.0:1 for levels above +6 dBm.

TEST EQUIPMENT:

- VSWR bridge
- RF spectrum analyzer
- High-frequency synthesized signal generator (HFSSG)

REMARKS:

The UUT settings in this procedure are chosen to provide confidence in the VSWR performance of the UUT throughout its range; however, you can also check the performance at other instrument settings.

VSWR problems are most likely to involve the A8 Output PCA or the A21 Attenuator PCA.

NOTE

The following procedures must be performed in the order given to ensure that the proper equipment is connected and appropriate programs are enabled.

PROCEDURE (Low-Level Test):

1. Turn on the UUT and program it to RCL 98.
2. Program the UUT to 640 MHz at +6 dBm.
3. Press SPCL 51 to select the fixed range special function on the UUT.
4. Use the EDIT function on the UUT to edit the amplitude to -30 dBm. Verify that the UNCAL annunciator lights.

NOTE

This procedure leaves the output attenuators set as they would be for a ×6 dBm output level but uses the electronic control to turn down the RF level coming out of the UUT.

5. Connect the UUT to the Device Under Test port of the VSWR bridge.
6. Connect the RF spectrum analyzer to the RF OUT port of the VSWR bridge.
7. Connect the HFSSG to the RF IN port of the VSWR bridge.
8. Program the HFSSG to 10 MHz at +13 dBm.
9. Set the RF spectrum analyzer to display approximately 10 to 1056 MHz and set the reference level to +10 dBm.
10. Step the HFSSG from 10 to 1056 MHz in 10-MHz steps. Locate the frequency at which the reflected signal (displayed by the RF spectrum analyzer) is maximum and record this level. This is the point with the worst-case VSWR.
11. Disconnect the UUT from the VSWR bridge and record the new level.
12. Calculate the return loss (difference) between the two recorded levels. The difference must be at least 14 dB (14 dB of return loss = 1.5:1 VSWR).

PROCEDURE (High-Level Test):

1. Program the UUT to +10 dBm.
2. Press SPCL 51 to select the special function fixed range on the UUT.
3. Use the EDIT function on the UUT to edit the amplitude to -30 dBm.
4. Connect the UUT to the Device Under Test port of the VSWR bridge.
5. Step the HFSSG from 10 to 1056 MHz in 10-MHz steps. Locate the frequency at which the reflected signal is maximum and record this level.
6. Disconnect the UUT from the VSWR bridge and record the new level.
7. Calculate the return loss between the two recorded levels. The difference must be at least 9.5 dB (9.5 dB of return loss = 2.0:1 VSWR).

PULSE TESTS 3-22.

The Pulse Tests check the static and dynamic operation of pulse modulation.

REQUIREMENTS:

Proper pulse operation is tested by checking the following:

On/Off Ratio: 60 dB for frequencies <100 MHz
40 dB for frequencies >100 MHz

Rise/Fall time: <15 ns, 10% to 90%. Typically 7.5 ns. Output Level Accuracy: Within ±0.7 dB of CW accuracy for pulse widths >50 ns.

TEST EQUIPMENT:

- RF spectrum analyzer
- Pulse generator
- Power meter
- Power sensor (high-level)
- 50Ω Type "N" termination
- Oscilloscope
- Detector

NOTE

The following procedures must be performed in the order given to ensure that the proper equipment is connected and the appropriate programs are enabled.

PROCEDURE (Static Test):

1. Program the UUT to 1056 MHz and +10 dBm.
2. Connect a 50Ω termination to the pulse modulation input connector.
3. Connect the UUT RF OUTPUT to the RF spectrum analyzer input.
4. Set the RF spectrum analyzer controls to display the output of the UUT using a span of approximately 0.1 MHz to 1056 MHz.
5. Activate pulse modulation by pressing the External Pulse key on the UUT.
6. Observe the level change on the RF spectrum analyzer. The change should exceed 40 dB.
7. Deactivate external pulse by pressing the External Pulse key on the UUT, and repeat steps 4 through 6 for UUT frequencies of 950, 850, 700, 640, 550, 400, 320, 250, 160, and 100 MHz.
8. Repeat steps 6 and 7 for the following frequencies: 80, 60, 40, 30, 20, 14, 5, 1, and 0.1 MHz. Verify that the observed level change is greater than 60 dB.

PROCEDURE (Dynamic Test):

1. Program the UUT to 640 MHz, +10 dBm, and external pulse modulation.
2. Connect the pulse generator to the UUT pulse input connector.
3. Set the pulse generator to a repetition rate of 5 MHz, +3V pulse level, and roughly a 50% duty cycle.
4. Connect the output of the UUT to the detector.
5. Terminate the detector into 50Ω at the oscilloscope input.
6. Set the time base of the oscilloscope to 10 nanoseconds (or smaller) per division.
7. Use the oscilloscope channel to invert the detector output signal.
8. Trigger the oscilloscope on this signal.
9. Set the variable position and gain on the oscilloscope so that the signal extends from 0% to 100% on the graticule.
10. Measure the rise/fall time from the 90% to the 10% coordinates.
11. Verify that the rise/fall time is $<$ 15 nanoseconds.

PROCEDURE (Level Error Test):

1. Remove the UUT, and reconnect the pulse generator directly into the oscilloscope.
2. Set the pulse generator to 5-MHz repetition rate, +3V level, and 50% duty cycle.
3. Adjust the oscilloscope position and gain controls for easy full scale viewing.
4. Readjust the pulse duty cycle for exactly 50% as measured at the 1V level of the oscilloscope.
5. Remove the pulse generator from the oscilloscope, and reconnect it to the pulse input of the UUT.
6. Program the UUT to 100 MHz, +7dBm, and external pulse modulation.
7. Connect the UUT output to the RF spectrum analyzer input.
8. Set the RF spectrum analyzer to observe a three-line spectra on either side of the center line spectra. The center spectra may be verified by turning pulse modulation off. (Use a spectrum analyzer setting of 5 MHz/div span and 100 kHz resolution bandwidth.)
9. Adjust the duty cycle of the pulse generator for exactly 50% duty cycle by nulling the second line from the center line (approximately 10-MHz offset). A null of -30 dBc or below should be established.
10. Replace the RF spectrum analyzer with the power meter, and set the power meter to the reference setting.

11. Turn the UUT pulse modulation off and note the meter reading. The difference between the meter reading and 3.01 dB is the pulse level error. This error should be less than 0.7 dB.

12. Repeat steps 6 through 11 for 500 and 1056 MHz.

INTERMODULATION TEST 3-23.

Third-Order Intermodulation: Applies with each signal level at +4 dBm into a resistive combiner.

REQUIREMENTS: As shown in Table 3-9.

TEST EQUIPMENT:

- RF spectrum analyzer
- 3-dB hybrid
- High-frequency synthesized signal generator (HFSSG)
- 6-dB resistive combiner

REMARKS:

The first part of this test is necessary to verify that the spectrum analyzer has a low enough level of internally generated intermodulation distortion (IMD) to allow the UUT measurement to be valid.

Table 3-9. Intermodulation Requirements

APPROXIMATE CARRIER FREQUENCY BAND (MHz)	SIGNAL SPACING	
	1 kHz	25 kHz
512 to 1056	-65 dBc	-70 dBc
128 to 512	-65 dBc	-75 dBc
0.01 to 128	-60 dBc	-75 dBc

Equipment Verification 3-24.

PROCEDURE:

1. Connect the UUT and the HFSSG to the spectrum analyzer through isolated ports of the 3 dB hybrid.

2. Connect the spectrum analyzer 10 MHz output to the UUT and HFSSG 10 MHz inputs and set the UUT and HFSSG to EXT REF.

3. Program the UUT to RCL 98, 50 MHz, and +4 dB.

4. Program the HFSSG to RCL 98, 50.025 MHz, and +4 dBm.

5. Set the starting spectrum analyzer settings to the following:

   a. RF attenuation 20 dB.
   b. Reference level 0 dBm.
   c. Center frequency 49.975 MHz.
   d. Frequency span 100 kHz.

6. Adjust the reference level to place the UUT signal at the top graticule of the display.

7. Place a marker on the IMD product at 49.975 MHz.

8. Increase the spectrum analyzer RF attenuation to 30 and then to 40 dB while observing the IMD product at the marker. It will be necessary to reduce the frequency span to 1 kHz or less and reduce both the resolution bandwidth and video bandwidth to 10 Hz.

9. The IMD product at 49.975 MHz should be 85 dB or more down from the UUT carrier level.

10. Repeat steps 3 through 9 at 500 and 1000 MHz. Measurement values should be -85 and -80 dBc or below respectively. If these values (from steps 9 and 10) cannot be realized, the measurements on the UUT will likely not be valid.

Intermodulation Distortion Test 3-25.

1. Connect the UUT and the HFSSG to the spectrum analyzer through the 6-dB resistive combiner.

2. Connect the spectrum analyzer 10 MHz out to the UUT and HFSSG 10-MHz inputs and set the UUT and HFSSG to EXT REF.

3. Program the UUT to RCL 98, 50 MHz, and +4 dBm.

4. Program the HFSSG to RCL 98, 50.025 MHz, and +4 dBm.

5. Set the starting spectrum analyzer settings to the following:

   a. RF attenuation 20 dB.
   b. Reference level 0 dBm.
   c. Center frequency 49.975 MHz.
   d. Frequency span 100 kHz.

6. Adjust the reference level to place the UUT signal at the top graticule of the display.

7. Place a marker on the IMD product at 49.975 MHz.

8. Change the spectrum analyzer settings to the following:

   a. Frequency span 1 kHz.
   b. Resolution bandwidth 10 Hz.
   c. Video bandwidth 10 Hz.

9. To meet the requirements, the IMD product must be -75 dBc or below.

10. Repeat steps 3 through 9 at 500 and 1000 MHz. The measurements should be -75 and -70 dBc or below, respectively.

Section 4
Closed-Case Calibration

INTRODUCTION 4-1.

The procedures in this section calibrate the RF output level, AM depth, FM deviation, and the internal 10-MHz reference oscillator without requiring that the the instrument covers be removed. You can perform the procedures directly by pressing the front panel keys, or remotely under the control of an IEEE-488 bus controller.

Perform the calibration procedures at the specified 2-year calibration intervals or as needed to optimize 6080A Synthesized RF Signal Generator performance.

Each procedure includes the following steps:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.
2. Initiate the calibration procedure.
3. Connect the required measurement equipment to the Signal Generator's RF OUTPUT.
4. Adjust the parameter of interest until the meter reading matches a predetermined target value.
5. Store the updated calibration factor.

These calibration procedures cannot correct hardware failures. If calibration fails to adjust the Signal Generator to proper specifications, consult Section 6, Circuit Descriptions, Troubleshooting, and Alignment for troubleshooting and repair information.

Front Panel Calibration 4-2.

The front panel calibration procedures describe the steps required to perform each test. The edit knob increases or decreases the bright-digit value. You must adjust the bright-digit value until the 6080A reading matches the target value.

Remote Calibration 4-3.

Remote calibration procedures allow the Signal Generator to be automatically calibrated by an IEEE bus controller. When connected to the required measurement equipment and under control of appropriate bus controller software, calibration consists of simply connecting cables to the instruments and executing the program.

The basic structure of a calibration program is shown in Figure 4-1.

```
initiate 6080A calibration procedure
initialize measurement equipment

loop
    ask 6080A for RF output frequency
    exit loop if frequency is special end code "9E+09"
    get reading from measurement equipment
    send reading to the 6080A
    end loop

save calibration data
exit calibration procedure
```

Figure 4-1.Basic Structure of Calibration Program

A remote calibration procedure begins when the bus controller initializes the measurement equipment by initiating the firmware calibration program located in the Signal Generator. The controller then requests the Signal Generator's RF output frequency and waits for a response. The controller requests the RF output frequency each time through the main loop to synchronize the controller with the Signal Generator and to provide an exit point when the procedure is complete.

When the bus controller receives the response from the Signal Generator, it gets a reading from the measurement equipment, ensures the reading is settled and valid, and converts the reading into a format understood by the Signal Generator. The controller then sends the reading to the Signal Generator, which uses the reading to update its internal settings. The Signal Generator does not respond to the next frequency query until it is ready for another reading. The controller waits for the Signal Generator's output to settle before taking another measurement reading.

The Signal Generator continues to receive readings and make internal adjustments until it gets two consecutive readings within the error tolerance for the procedure. The error tolerance is defined for each procedure as a range of readings around the target value that the Signal Generator expects to receive when the adjustment is correct. When two readings are within the error tolerance, the adjustment is considered valid.

The program remains in the main loop until the Signal Generator returns the end code "9E+09 HZ", in response to the next frequency query. When the controller receives the end code, it exits the loop and saves the measurement data in the Signal Generator's calibration memory.

The division of responsibility between the controller and Signal Generator allows the use of measurement equipment from various manufacturers. Adding a different meter to the system requires only that a new driver module be written for the controller.

NOTE

The accuracy of the remote calibration procedure depends largely on the design of the controller software. Before sending the result to the 6080A, determine that the readings are settled, and average several readings. Where applicable, apply meter-specific calibration factors to the readings.

Sample controller programs for each remote procedure are included in Appendix G. The programs are written in Fluke BASIC and are provided as examples of the programs that will run on a Fluke 1722A controller.

Calibration Data 4-4.

After making internal adjustments, the Signal Generator stores calibration data along with compensation data in non-volatile memory. Two copies of data provide a redundant storage scheme to enhance data integrity. The two copies are stored in separate locations: one copy is stored in the battery-backed RAM and an identical copy is stored in the EEPROM.

Calibration data are generated either by the Fluke factory or by the user. Each calibration data segment contains a data origin code that specifies how the data segment was created.

The calibration and compensation data origin codes display when special function 05 is entered. Origin code 00 signifies that the data originated at the Fluke factory; therefore, no user calibration or compensation procedures have been performed. If any user calibration procedures have been performed, the corresponding code is displayed. For example, if the AM calibration procedure has been performed by the user, the data origin special function displays the code 528. A complete list of the data origin codes is given in Appendix F.

Refer to the Operator Manual for more information about special functions.

CALIBRATION SETUP 4-5.

Before beginning the procedures, set the rear panel slide switch labeled CAL|COMP to the 1 (on) position. Setting the rear panel switch to this position causes the CAL and COMP annunciators to blink, indicating that a calibration procedure can be selected when SPCL is pressed. When a calibration procedure is initiated, the CAL and COMP annunciators stop blinking and the CAL annunciator remains lit until the procedure is complete. When the rear panel switch is in the 0 (off) position, the data is write-protected in hardware.

AM CALIBRATION 4-6.

The AM calibration procedures allow a single point calibration of the AM depth. An RF modulation meter is connected to the 6080A's RF output and the AM calibration factor is adjusted based on the meter reading. The parameters specific to this procedure are listed below:

- Adjustment Range: ± 5% AM Depth
- Adjustment Resolution: 0.1%
- Target Value: 50.0%
- RF Frequency: 300.000000 MHz
- RF Level: +10.0 dBm
- Internal AM: ON
- Modulation Frequency: 1 kHz
- External Equipment: RF Modulation Analyzer (HP 8901A or equivalent)

When performing the front panel procedure, use the edit knob to adjust the AM depth until the measured AM depth matches the target value. During the remote calibration procedure, a program running on an IEEE-488 bus controller directs the procedure.

Both the front panel and remote calibration procedures reconfigure the front panel display in the following ways: the target level displays in the modulation field, the RF frequency displays in the frequency field, the adjustment value displays in the amplitude field, and the CAL annunciator lights.

All adjustments update a temporary copy of the AM calibration factor. The copy in the calibration memory updates only after the store command is given explicitly. After the store command has been given, the internal calibration factor is calculated from the displayed adjustment value and is stored in the calibration memory. Subsequent AM programming commands use the new calibration factor.

Front Panel AM Calibration Procedure 4-7.

This procedure disables several of the front panel controls or causes them to operate differently than they normally do. It also reconfigures the display.

Table 4-1 lists the front panel controls used in the calibration procedures and describes the function of each.

Proceed as follows to perform the front panel AM calibration procedure:

1. Set the rear panel CAL|COMP switch to 1 (on) position.
2. Enter special function 991 to initiate the AM calibration procedure.
3. Connect the RF OUTPUT of the 6080A to the modulation meter.
4. Select the peak+ mode, enable the 50-Hz high-pass filter, and enable the 3 kHz low-pass filter on the modulation meter.
5. Use the edit knob to change the adjustment value until the modulation meter reads 50.0%.
6. Press STO twice to store the new data.

Remote AM Calibration Procedure 4-8.

The following paragraphs describe the remote AM calibration procedure, the remote commands needed for this procedure, and the elements required to build a functioning controller program. Refer to the Remote Calibration, eariler in this section, for general information about remote calibration.

A sample controller program for the remote AM calibration procedure is contained in Appendix G. The program is written in Fluke BASIC and is provided as an example of the programs that will run on a Fluke 1722A controller.

Table 4-2 provides information needed to create a remote calibration program. This table lists specific commands that must be included in the AM calibration program. Table 5B-3 in Section 5B of the Operator Manual describes the syntax of each command.

Table 4-1. Front Panel Controls Function for Calibration Procedures

CONTROLS	FUNCTION AND DESCRIPTION
◁ ▷	Bright-Digit Editing
KNOB	Turn the edit knob to change the adjustment value. Use the left/right arrow keys to move the bright-digit within the adjustment field. The bright-digit is always located in the adjustment field.
ON/OFF	RF on/off Toggles the RF output on/off.
STATUS	Overrange/uncal or Rejected Entry Status Normally displays the overrange/uncal status. Displays the rejected entry status code if there is a rejected entry.
STO	Store Measured Data Press once; the prompt "Sto ?" is displayed. Press again to store the data. The message "--Sto--" is displayed to confirm the the selection. The updated calibration factor is stored in the calibration memory, and the last valid instrument state is restored. Press any other key to cancel the store operation and resume the procedure.
CLR|LCL	Abort the Cal Procedure Press once; the prompt "Clr ?" is displayed. Press again to abort the procedure. The message "--Clr--" is displayed to confirm the selection. All measured data is discarded and the previous instrument state is restored. Press any other key to resume the procedure.

Table 4-2. Remote Programming Commands for AM Calibration Procedure

COMMANDS	DESCRIPTION
CAL_AM	Initiate the remote AM calibration procedure
CC_RDAM	Send the mod meter reading to the 6080A
CC_FREQ?	Request the RF frequency
CC_TARGET?	Request the target value
RFOUT	Program the RF output on/off
CC_SAVE	Save the measured data
CC_EXIT	Abort the cal procedure immediately
ERROR?	Request the rejected entry status
STATUS/STATUS?	Load/request the overrange/uncal status

Figure 4-2 outlines the operation of the program in this procedure.

```
initiate the AM calibration procedure with "CAL_AM"
initialize modulation meter

MAIN_LOOP:
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    read modulation meter
    send reading to 6080A with "CC_RDAM"

    goto MAIN_LOOP

DONE:
store new data in calibration memory with "CC_SAVE"
end
```

Figure 4-2. Structure of the AM Calibration Program

Proceed as follows to initiate the remote AM calibration procedure:

1. Set the rear panel CAL|COMP switch to 1 (on) position.

2. Initiate the bus controller program.

During the operation of the remote calibration procedure, the controller requests the Signal Generator's center frequency with the command CC_FREQ? and waits for a response.

When a response is received, the controller gets a modulation meter reading. The controller program ensures that each modulation meter reading is settled before sending the reading to the Signal Generator with the command CC_RDAM.

The Signal Generator receives the reading, adjusts its internal settings, and programs the new AM depth. The program continues to loop until the Signal Generator receives two consecutive readings within an error tolerance of 0.1%. At that point it considers the adjustment value correct and returns the end code "9E+09, HZ" to the controller in response to the CC_FREQ? command.

The program exits the main loop and the saves the data by sending out the CC_SAVE command.

FM CALIBRATION 4-9.

The FM calibration procedure allows a single point calibration (see listing below) of the FM deviation. The adjustment of the FM calibration factor is based on the reading of an RF modulation meter connected to the 6080A's RF output. The specific parameters for this procedure are listed below:

- Adjustment Range: ± 10 kHz
- Adjustment Resolution: 0.1 kHz
- Target Value: 100 kHz
- Frequency: 640.000000 MHz
- RF Level: +10.0 dBm
- Internal FM: ON
- Modulation Frequency: 1 kHz
- External Equipment: RF Modulation Analyzer (HP 8901A or equivalent)

To perform the front panel procedure, use the edit knob to adjust the FM deviation until the measured deviation matches the target value. During the remote calibration procedure, a program running on an IEEE-488 bus controller directs the procedure.

Both the front panel and remote calibration procedures reconfigure the front panel display in the following ways: the target level displays in the modulation field, the RF frequency displays in the frequency field, the adjustment value displays in the amplitude field, and the CAL annunciator lights.

All adjustments update a temporary copy of the FM calibration factor. The copy in the calibration memory is updated only after the store command is given explicitly. After the store command has been given, the internal calibration factor is calculated from the displayed adjustment value and is stored in the calibration memory. Subsequent FM programming commands use the new calibration factor.

Front Panel FM Calibration Procedure 4-10.

The display is reconfigured for the front panel FM calibration procedure. Several of the front panel controls are disabled or operate differently than they normally do. Table 4-1 lists the active front panel controls and describes their function during the calibration procedure.

Proceed with the following steps to execute the front panel FM calibration procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.

2. Enter special function 992 to initiate the FM procedure.

3. Connect the 6080A's RF OUTPUT to the modulation meter.

4. Select the peak+ mode, enable the 50 Hz high-pass filter, and enable the 3 kHz low-pass filter on the modulation meter.

5. Use the edit knob to change the adjustment value until the modulation meter reads 100 kHz.

6. Press the STO key twice to store the new data.

Remote FM Calibration 4-11.

The following paragraphs describe the remote FM calibration procedure, the remote commands needed for this procedure, and the elements required to build a functioning controller program. Refer to the Remote Calibration, paragraph 4-3, for general information about remote calibration.

A sample controller program for the remote FM calibration procedure is contained in Appendix G. The program is written in Fluke BASIC and is provided as an example of the programs that will run on a Fluke 1722A controller.

Table 4-3 provides information needed to create a remote calibration program. This table lists specific commands that must be included in the FM calibration program. Table 5B-3 in Section 5B of the Operator Manual describes the syntax of each command.

Figure 4-3 outlines the operation of the program in this procedure.

Table 4-3. Remote Programming Commands for FM Calibration Procedure

COMMANDS	DESCRIPTION
CAL_FM	Initiate the remote FM calibration procedure
CC_RDFM	Send the mod meter reading to the 6080A
CC_FREQ?	Request the RF output frequency
CC_TARGET?	Request the target value
RFOUT	Program the RF output on/off
CC_SAVE	Save the measured data
CC_EXIT	Abort the cal procedure immediately
ERROR?	Request the rejected entry status
STATUS/STATUS?	Load/request the overrange/uncal status

```
initiate the FM calibration procedure with "CAL_FM"
initialize modulation meter

Main Loop
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    read modulation meter
    send reading to 6080A with "CC_RDFM"

    goto Main Loop

DONE
store new data in calibration memory with "CC_SAVE"
end
```

Figure 4-3. Basic Structure of FM Calibration Program

Proceed as follows to initiate the remote FM calibration procedure:

1. Set the rear panel CAL|COMP switch to 1 (on) position.

2. Initiate the bus controller program.

The bus controller initiates the procedure with the CAL_FM command. The controller requests the Signal Generator's center frequency with the CC_FREQ? command and waits for a response.

When a response is received, the controller gets a mod meter reading. The controller program ensures that each meter reading is settled before sending the reading to the Signal Generator with the command CC_RDFM.

Each time the Signal Generator receives a reading from the controller, it adjusts its internal settings and programs the new FM deviation.

The program remains in the main loop until the Signal Generator receives two consecutive readings within 0.1 kHz of the target value (100 kHz). At this time it considers the displayed adjustment value correct and returns the end code "9E+09, HZ" in response to the CC_FREQ? command.

The program exits the main loop and the saves the data by sending out the CC_SAVE command.

RF LEVEL CALIBRATION 4-12.

The RF level calibration procedures perform a single-point calibration of the RF output level. An RF power meter is connected to the Signal Generator's RF OUTPUT and the level calibration factor is adjusted based on the meter reading. The parameters specific to this procedure are as follows:

- Adjustment Range: ± 1.00 dB
- Adjustment Resolution: 0.01 dB
- Target Value: 10.0 dBm
- Frequency: 300.000000 MHz
- RF Level: +10.0 dBm
- External Equipment: RF Power Meter (HP 436A or equivalent)

When performing the front panel procedure, use the edit knob to adjust the level until the measured level matches the target level. The remote calibration procedure is controlled by a program running on an IEEE-488 bus controller.

Both the front panel and remote calibration procedures reconfigure the front panel display in the following ways: the target level displays in the modulation field, the RF frequency displays in the frequency field, the adjustment value displays in the amplitude field, and the CAL annunciator lights.

All adjustments update a temporary copy of the adjustment value. The copy in the calibration memory is updated only after the store command is given explicitly by the user or remote controller. After the store command is received by the Signal Generator, the internal calibration factor is calculated from the displayed adjustment value and is stored in the calibration memory. Subsequent amplitude programming commands use the new calibration factor.

Front Panel Level Calibration Procedure 4-13.

The display is reconfigured for the procedure. Several of the front panel controls are disabled or operate differently than they normally do.

Table 4-1 lists the active front panel controls and describes the function of each.

Proceed as follows to execute the front panel level calibration procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.
2. Enter special function 993 to initiate the level calibration procedure.
3. Connect the Signal Generator's RF OUTPUT to the power meter.
4. Set the appropriate power meter calibration factor (if required) and zero the power meter.
5. Use the edit knob to change the adjustment value until the power meter reads +10 dBm.
6. Press the STO key twice to store the new data.

Remote Level Calibration Procedure 4-14.

The following paragraphs describe the remote level calibration procedure, the remote commands needed for this procedure, and the elements required to build a functioning controller program. Refer to Remote Calibration, earlier in the section, for general information about remote calibration.

A sample controller program for the remote level calibration procedure is contained in Appendix G. The program is written in Fluke BASIC and is provided as an example of the programs that will run on a Fluke 1722A controller.

Table 4-4 provides information needed to create a remote calibration program. This table lists specific commands that must be included in the level calibration program. Table 5B-3 in Section 5B of the Operator Manual describes the syntax of each command.

Figure 4-4 outlines the operation of the program in this procedure.

Proceed as follows to initiate the remote level calibration procedure:

1. Set the rear panel CAL|COMP switch to 1 (on) position.
2. Initiate the bus controller program.

The bus controller initiates the procedure by sending out the CAL_LEVEL command. The controller requests the Signal Generator's center frequency with the CC_FREQ? command and waits for a response.

When the Signal Generator responds, the controller gets a power meter reading and sends it to the Signal Generator with the CC_RDPOWER command. The controller program ensures that each reading is settled before sending the reading to the Signal Generator.

Each time the Signal Generator receives a reading from the controller, it adjusts its internal settings and programs the new level. The program remains in the main loop until the Signal Generator receives two consecutive readings within 0.01 dB of the target value (10.00 dBm). The Signal Generator then considers the displayed adjustment value correct and returns the end code “9E+09, HZ” in response to the CC_FREQ? command.

The program exits the main loop and the saves the data by sending out the CC_SAVE command.

Table 4-4. Remote Programming Commands for Level Calibration Procedure

COMMANDS	DESCRIPTION
CAL_LEVEL	Initiate the remote level calibration procedure
CC_RDPOWER	Send the power meter reading to the 6080A
CC_FREQ?	Request the RF frequency
CC_TARGET?	Request the target value
RFOUT	Program the RF output on/off
CC_SAVE	Save the measured data
CC_EXIT	Abort the cal procedure immediately
ERROR?	Request the rejected entry status
STATUS/STATUS?	Load/request the overrange/uncal status

```
initiate the level calibration procedure with "CAL_LEVEL"
initialize power meter

Main Loop
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    read power meter
    send reading to 6080A with "CC_RDOWER"

    goto Main Loop

DONE
store new data in calibration memory with "CC_SAVE"
end
```

Figure 4-4. Basic Structure of the Level Calibration Program

REFERENCE OSCILLATOR CALIBRATION 4-15.

The reference oscillator calibration procedures perform a single-point calibration of the internal 10-MHz reference oscillator. A frequency counter is connected to the 6080A's RF OUTPUT, and the reference oscillator calibration factor is adjusted based on the counter reading. The following lists the specific parameters of this procedure:

- Adjustment Range: 256 counts (6 ppm minimum)
- Adjustment Resolution: 1 count
- Target Value: 100 MHz ±10 Hz
- RF Frequency: 100 MHz
- External Equipment: Frequency Counter (Fluke 1953A or equivalent)

When performing the front panel procedure, use the edit knob to adjust the calibration factor until the measured frequency matches the target value. During the remote calibration procedure, a program running on an IEEE-488 bus controller directs the procedure.

Both the front panel and remote calibration procedures reconfigure the front panel display in the following ways: the target level displays in the modulation field, the RF frequency displays in the frequency field, the adjustment value displays in the amplitude field, and the CAL annunciator lights.

The Signal Generator saves a copy of all adjustment values in temporary memory until it receives the store command. After receiving the store command, the Signal Generator calculates the internal calibration factor from the displayed adjustment value stores it in the calibration memory.

NOTE

This procedure can be used only to adjust the frequency of the internal reference oscillator. It cannot be used to adjust the frequency of the optional high-stability or medium-stability references (Options -130 and -132).

Front Panel Reference Oscillator Calibration Procedure 4-16.

The display is reconfigured for the procedure. Several of the front panel controls are disabled or operate differently than they normally do.

Table 4-1 lists the active front panel controls and describes the function of each.

Proceed as follows to execute the front panel reference oscillator calibration procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.
2. Enter special function 994 to initiate the oscillator calibration procedure.
3. Connect the 6080A's RF OUTPUT to the FLUKE 1953A's FREQA input.
4. Select the FREQA input, 1 second gate time, and the continuous trigger mode.
5. Use the edit knob to change the adjustment value until the counter reads 100 MHz ±10 Hz.
6. Press the STO key twice to store the new data.

Remote Reference Oscillator Calibration Procedure 4-17.

The following paragraphs describe the remote reference oscillator calibration procedure, the remote commands needed for this procedure, and the elements required to build a functioning controller program. Refer to Remote Calibration, earlier in this section, for general information about remote calibration.

A sample controller program for the remote reference oscillator calibration procedure is contained in Appendix G. The program is written in Fluke BASIC and is provided as an example of the programs that will run on a Fluke 1722A controller.

Table 4-5 provides information needed to create a remote calibration program. This table lists specific commands that must be included in the reference oscillator calibration program. Table 5B-3 in Section 5B of the Operator Manual describes the syntax of each command.

Figure 4-5 outlines the operation of the program in this procedure.

Table 4-5. Remote Programming Commands for Reference Oscillator

COMMANDS	DESCRIPTION
CAL_REFOSC	Initiate the remote reference oscillatorcalibration procedure
CC_RDFREQ	Send the counter reading to the 6080A
CC_FREQ?	Request the RF frequency
CC_TARGET?	Request the target value
RFOUT	Program the RF output on/off
CC_SAVE	Save the measured data
CC_EXIT	Abort the cal procedure immediately
ERROR?	Request the rejected entry status
STATUS/STATUS?	Load/request the overrange/uncal status

```
initiate the reference oscillator calibration procedure with "CAL_REFOSC"
initialize frequency counter

Main Loop
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    read frequency counter
    send reading to 6080A with "CC_RDFREQ"

    goto Main Loop

DONE
store new data in calibration memory with "CC_SAVE"
end
```

Figure 4-5. Basic Structure of the Reference Oscillator Calibration Program

Proceed as follows to initiate the remote reference oscillator calibration procedure:

1. Set the rear panel CAL|COMP switch to 1 (on) position.

2. Initiate the bus controller program.

The bus controller initiates the calibration procedure by sending out the CAL_REFOSC command. The controller requests the center frequency of the Signal Generator with the CC_FREQ? command and waits for a response.

When the Signal Generator responds, the controller gets a counter reading, ensures that the reading is settled, and sends it to the Signal Generator with the command CC_RDFREQ.

Each time the Signal Generator receives a reading from the controller, it adjusts its internal settings and programs the new reference oscillator DAC setting.

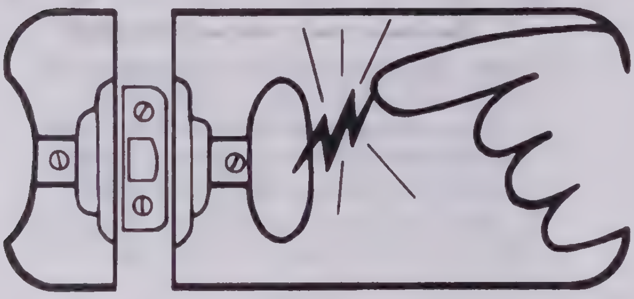
The program remains in the main loop until the Signal Generator receives two consecutive readings within 10 Hz of the target value (100 MHz). At that point, the Signal Generator considers the displayed adjustment value correct and returns the end code "9E+09, HZ" in response to the CC_FREQ? command.

The program exits the main loop and the saves the data by sending out the CC_SAVE command.

static awareness

A Message From

John Fluke Mfg. Co., Inc.



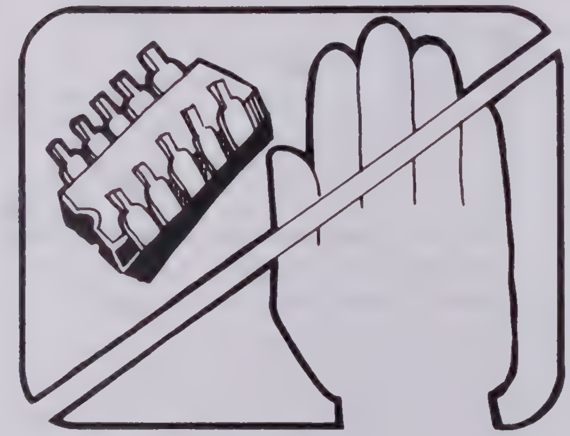
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

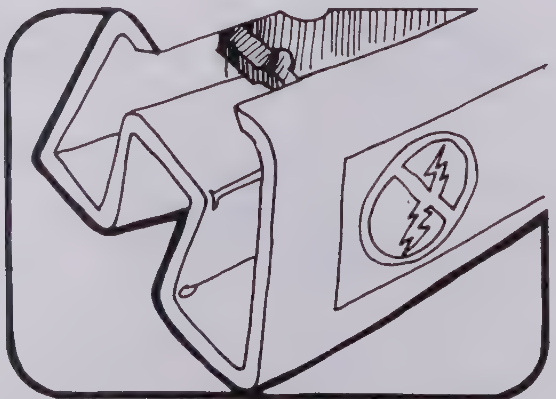
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol

"⊗"

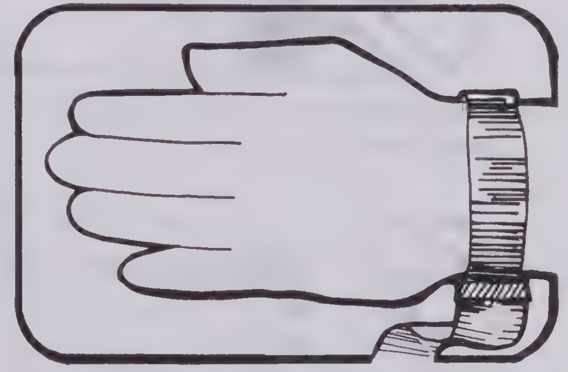
The following practices should be followed to minimize damage to S.S. devices.



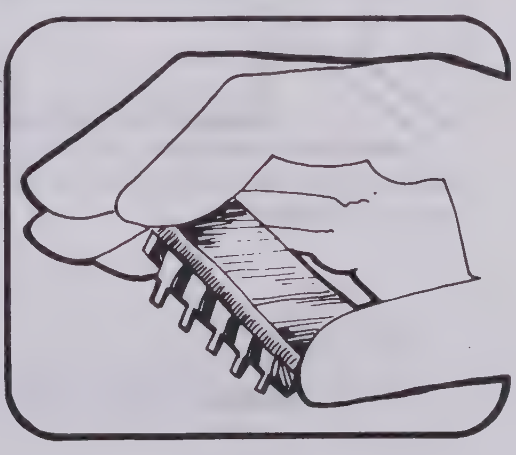
1. MINIMIZE HANDLING



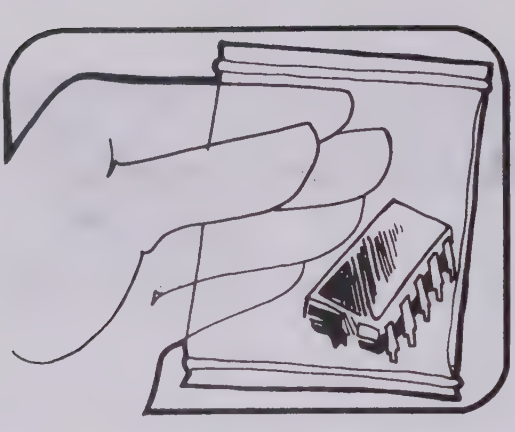
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



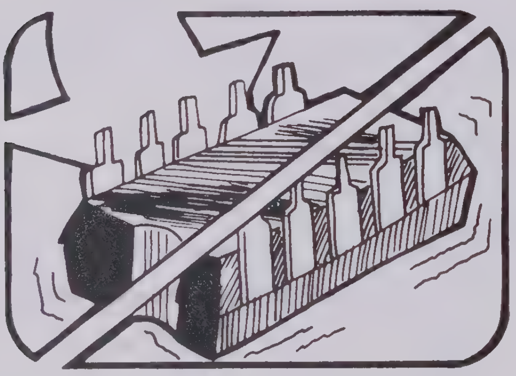
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



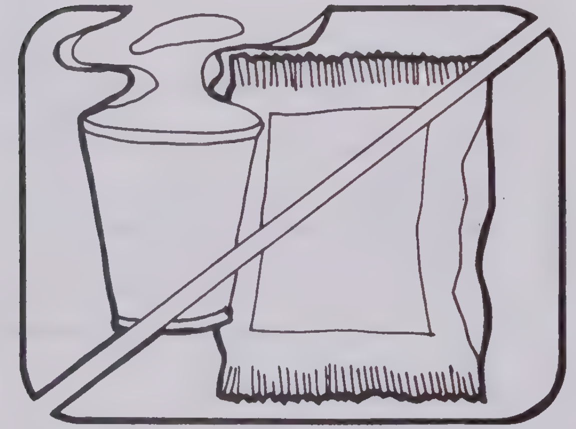
4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT

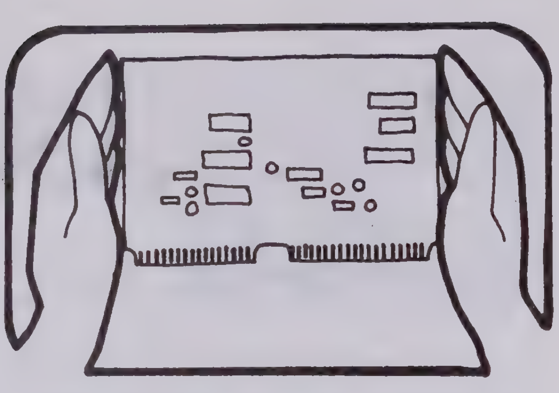


6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE

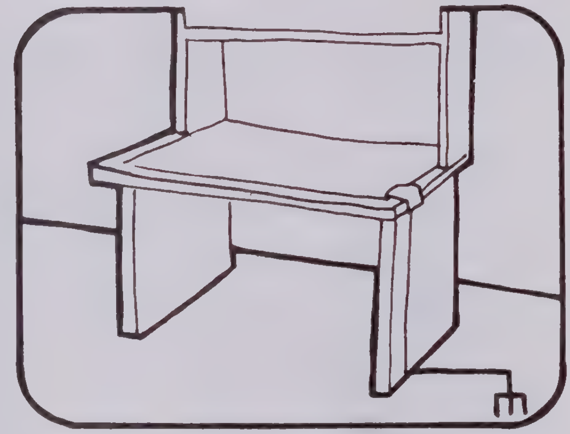


7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

PORTIONS REPRINTED
WITH PERMISSION FROM TEKTRONIX, INC.
AND GENERAL DYNAMICS, POMONA DIV.



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

® Dow Chemical

J0089D-07U8604/SE EN Litho in U.S.A.
Rev. 1 MAR 86

Section 5
Access Procedures

INTRODUCTION 5-1.

Section 5 describes access procedures for the following major assemblies:

- Front Panel Section
- Rear Panel Section
- A2 Coarse Loop PCA
- A3 Subsynthesizer VCO PCA
- A4 Subsynthesizer PCA
- A5 Coarse Loop VCO PCA
- A6 Mod Oscillator PCA
- A8 Output PCA
- A9 Sum Loop VCO PCA
- A10 Premodulator PCA
- A11 Modulation Control PCA
- A12 Sum Loop PCA
- A13 Controller PCA
- A14 FM PCA
- A20 Attenuator/RPP Assembly
- A22 Delay Line Assembly

Some assemblies found in the Signal Generator are not listed here because access descriptions are not required to remove them.

SAFETY 5-2.

Read the following paragraphs for important information on how to safely access the assemblies in the Signal Generator.

Refer to the safety sheet at the front of the manual for additional safety information.

WARNING

TO AVOID ELECTRIC SHOCK, DISCONNECT THE POWER CORD BEFORE REMOVING COVERS FROM THE SIGNAL GENERATOR.

The Signal Generator remains energized when the POWER switch is in the STBY position. Before accessing circuit boards, disconnect ac power by unplugging the power cord from the rear panel power receptacle before removing protective panels, replacing components, or soldering.

Some components and assemblies in the Signal Generator are susceptible to damage from electrostatic discharge. Refer to the parts lists in Section 8. Static sensitive components and assemblies are marked with an asterisk (*).

Refer to the Static Awareness sheet that appears at the front of this section for guidelines on proper handling of static sensitive devices.

PIVOTING SYNTHESIZER MODULE WARNING 5-3.

To gain access to many of the circuit boards in the synthesizer module, you must raise a pivoting module. This synthesizer module is heavy and could cause severe injury if it were to drop unexpectedly. A gas strut holds the module in the raised position while the unit is being serviced. When raising or lowering the module, observe the following warning to avoid injury.

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING THE MODULE. TEST THE GAS STRUT SUPPORT BY ATTEMPTING TO CLOSE THE MODULE RAPIDLY. THE STRUT SHOULD RESIST RAPID CLOSING OF THE MODULE.

A decal on the synthesizer module and the text under "Raising and Lowering the Synthesizer Module" describe the correct method of opening and closing the module. Read that information before attempting to raise the pivoting module.

LOCATION OF MAJOR ASSEMBLIES 5-4.

In Section 8, List of Replaceable Parts, illustrations show the location of the major assemblies of the Signal Generator.

Refer to Section 6, Circuit Descriptions, Troubleshooting, and Alignment for information on exchanging modules.

ACCESS INSTRUCTIONS 5-5.

Access instructions for some assemblies of the 6080A Signal Generator are provided in the following paragraphs.

To install the assemblies, reverse the disassembly steps. Be certain the pin connectors and filter sockets are straight when replacing a printed circuit assembly (pca). Make sure that pca pulls and RF cables are not pinched between the modules and module covers.

Removing the Front Panel Section 5-6.

Proceed as follows to remove the front panel section:

1. Remove the two #6 pan-head screws that attach the RF connector bracket to the output module near the A20 Attenuator assembly. One screw is accessible from the top of the instrument, the other from the bottom.

2. Disconnect the RF output cable W1 from the Type "N" RF OUTPUT connector J1.

3. Remove the decals from both front panel handles. (Removing the decals ruins them. To restore instrument appearance to new condition, attach new decals when reassembling. The decal part number is listed in Section 10, Table 10-1.)

4. Remove the five flat-head screws from each front panel handle, and slide the front panel forward.

5. Disconnect power ribbon cable W20 and controller ribbon cables W18 and W36 from the front panel A1 Display PCA.

6. Disconnect the inner part of the BNC connectors on the mod input and mod output cables W2, W3, W4, and W5.

Removing the Rear Panel Section 5-7.

Proceed as follows to remove the rear panel section:

1. Disconnect the synthesizer and output module power cables W22 and W23, and the front panel power cable W20 from the A15 Power Supply PCA.

2. Disconnect the controller-IEEE ribbon cable W17 from the A16 IEEE PCA.

3. Disconnect the REF IN and REF OUT RF cables W6 and W7 from the synthesizer module.

4. Remove the decals from both rear panel handles. (Removing the decals ruins them. To restore instrument appearance to new condition, attach new decals when reassembling. The decal part number is listed in Section 10, Table 10-1.)

5. Remove the five flat-head screws from each handle. Remove the rear panel section.

Raising and Lowering the Synthesizer Module 5-8.

The synthesizer module, which must be raised to gain access to many of the circuit boards, is very heavy. For protection, a gas strut is installed to support the module. The top (synthesizer) module pivots up to allow access to all parts of the Signal Generator. To avoid injury when raising or lowering the module, read the following warning and observe the following procedures.

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE FOLLOWING PROCEDURE BEFORE RAISING THE MODULE. TEST THE GAS STRUT SUPPORT BY ATTEMPTING TO RAPIDLY CLOSE THE MODULE. THE STRUT SHOULD RESIST RAPID CLOSING OF THE MODULE.

Proceed as follows to raise the synthesizer module:

1. Remove the three #8 pan-head screws that secure the module to the chassis sides.

2. Grasp the handle and lift the module.

3. Lock the module in the up position by inserting two of the previously removed #8 screws into the bosses protruding from the chassis sides near the hinges.

Proceed as follows to lower the synthesizer module:

1. Support the module in the raised position and remove the two lock-up screws.
2. Keep hands clear and use the handle to lower the module.
3. Lock the module in the down position using the three #8 pan-head screws.

CAUTION

THE GAS STRUT CAN SWING THE SYNTHESIZER MODULE OPEN WHEN THE INSTRUMENT IS TURNED ON ITS SIDE. TO AVOID THIS, ALWAYS LOCK THE SYNTHESIZER MODULE IN THE DOWN POSITION AFTER LOWERING IT.

Removing the A2 Coarse Loop PCA 5-9.

Proceed as follows to remove the A2 Coarse Loop PCA:

1. Disconnect RF cables W6, W7, and W15 from the connectors at the rear of the synthesizer module, and remove the nuts and lock washers from the connectors.

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

2. Raise the synthesizer module.
3. Remove the #6 screws holding the bottom synthesizer module cover, and remove the cover.
4. Remove plug-in capacitor C1 and resistor R1, which are between the A22 Delay Cable assembly and the A2 Coarse Loop PCA.

NOTE

When reinstalling C1, be certain to put it between J1 on the A22 Delay Cable assembly and J9 on the A2 Coarse Loop. J2 on A22 and J10 on the A2 PCA are not used.

5. Remove the #6 screws holding the heat sinks on U305 and U310, and remove the heat sinks.
6. Remove the #6 screws holding the PCA.
7. Carefully remove the A2 Coarse Loop PCA.

Removing the A3 Subsynthesizer VCO PCA 5-10.

Proceed as follows to remove the A3 Subsynthesizer VCO PCA:

1. Disconnect RF cable W13 from the connector at the front of the synthesizer module, and remove the nut and lock washer from the connector.

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

2. Raise the synthesizer module.
3. Remove the #6 screws holding the bottom synthesizer module cover, and remove the cover.
4. Remove the #6 screws holding the PCA.
5. Carefully remove the A3 Subsynthesizer VCO PCA.

Removing the A4 Subsynthesizer PCA 5-11.

Proceed as follows to remove the A4 Subsynthesizer PCA:

1. Remove the #6 screws holding the top synthesizer module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
2. Remove the #6 screws holding the PCA.
3. Carefully remove the A4 Subsynthesizer PCA.

Removing the A5 Coarse Loop VCO PCA 5-12.

Proceed as follows to remove the A5 Coarse Loop VCO PCA:

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

1. Raise the synthesizer module.
2. Disconnect RF cable W14 from the connector at the front of the synthesizer module, and remove the nut and lock washer from the connector.
3. Lower the synthesizer module.
4. Remove the #6 screws holding the top synthesizer module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)

5. Remove the #6 screws holding the PCA.
6. Carefully remove the A5 Coarse Loop VCO PCA.

Removing the A6 Mod Oscillator PCA 5-13.

Proceed as follows to remove the A6 Mod Oscillator PCA:

1. Remove the #6 screws holding the top synthesizer module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
2. Remove the #6 screws holding the PCA.
3. Carefully remove the A6 Mod Oscillator PCA.

Removing the A8 Output PCA 5-14.

Proceed as follows to remove the A8 Output PCA:

WARNING

AVOID PERSONAL INJURY. THE SYNTHESIZER MODULE IS HEAVY; BE FAMILIAR WITH THE INSTRUCTIONS IN PARAGRAPH 5-8 BEFORE PERFORMING THE FOLLOWING PROCEDURE.

1. Raise the synthesizer module.
2. Disconnect RF cable W15 from the connector at the back of the output module, and remove the nut and lock washer from the connector.
3. Lower the synthesizer module.
4. Remove the #6 screws holding the bottom output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
5. Disconnect the RF cable, which is part of the A8 Output PCA, from the A10 Premodulator PCA.
6. Disconnect the two mod control-output ribbon cables W33 and W35 from the Output PCA.
7. Remove the #6 screws holding the output amplifier cover, and remove the cover.
8. Remove the #6 screws holding the output barrier.
9. Remove the remaining #6 screws holding the PCA. Do not remove the #4 screws that are in the output amplifier area.
10. Carefully remove the A8 Output PCA.

Removing the A9 Sum Loop VCO PCA 5-15.

Proceed as follows to remove the A9 Sum Loop VCO PCA:

1. Remove the #6 screws holding the bottom output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
2. Remove plug-in capacitor C1 between the A10 Premodulator PCA and the A9 Sum Loop VCO PCA.
3. Remove the #6 screws holding the PCA.
4. Carefully remove the A9 Sum Loop VCO PCA.

Removing the A10 Premodulator PCA 5-16.

Proceed as follows to remove the A10 Premodulator PCA:

1. Remove the #6 screws holding the bottom output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
2. Disconnect the RF cable, which is part of the A8 Output PCA, from the A10 Premodulator PCA.
3. Disconnect mod control-premodulator ribbon cable W34 from the A10 Premodulator PCA.
4. Remove plug-in capacitor C1 between the A10 Premodulator PCA and the A9 Sum Loop VCO PCA.
5. Remove the #6 screws holding the PCA.
6. Carefully remove the A10 Premodulator PCA.

Removing the A11 Modulation Control PCA 5-17.

Proceed as follows to remove the A11 Modulation Control PCA:

1. Remove the #6 screws holding the bottom output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
2. Disconnect mod control-premodulator ribbon cable W34 from the A11 Mod Control PCA.
3. Disconnect mod control-output ribbon cables W33 and W35 from the A11 Mod Control PCA.
4. Remove the #6 screws holding the PCA.
5. Carefully remove the A11 Modulation Control PCA.

Removing the A12 Sum Loop PCA 5-18.

Proceed as follows to remove the A12 Sum Loop PCA:

1. Disconnect RF cables W13 and W14 from the connectors at the front edge of the output module, and remove the nuts and lock washers from the connectors.

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

2. Raise the synthesizer module.
3. Remove the #6 screws holding the top output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
4. Disconnect FM-sum loop ribbon cable W32 from the A12 Sum Loop PCA.
5. Remove plug-in capacitor C2 between the A12 Sum Loop PCA and the A14 FM PCA.
6. Remove the #6 screws holding the sum loop lid, and remove the lid.
7. Remove the #6 screws holding the PCA.
8. Carefully remove the A12 Sum Loop PCA.

Removing the A13 Controller PCA 5-19.

Proceed as follows to remove the A13 Controller PCA:

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

1. Raise the synthesizer module.
2. Remove the #6 screws holding the top output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
3. Disconnect front panel display ribbon cables W18 and W36 from the A13 Controller PCA.
4. Disconnect IEEE ribbon cable W17 from the A13 Controller PCA.
5. Disconnect controller-synthesizer ribbon cable W16 from the A13 Controller PCA.
6. Disconnect power supply cable W22 from the A13 Controller PCA.

7. Disconnect relay driver ribbon cable W19 from the A13 Controller PCA.
8. Remove the #6 screws holding the PCA.
9. Carefully remove the A13 Controller PCA.

Removing the A14 FM PCA 5-20.

Proceed as follows to remove the A14 FM PCA:

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

1. Raise the synthesizer module.
2. Remove the #6 screws holding the top output module cover, and remove the cover. (The #10 screws are adjustment-access screws and need not be removed.)
3. Disconnect FM-sum loop ribbon cable W32 from the A14 FM PCA.
4. Remove plug-in capacitor C2 between the A12 Sum Loop PCA and the A14 FM PCA.
5. Remove the #6 screws holding the PCA.
6. Carefully remove the A14 FM PCA.

Removing the A20 Attenuator/RPP Assembly 5-21.

Proceed as follows to remove the A20 Attenuator/RPP Assembly:

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

1. Raise the synthesizer module.
2. Disconnect the RF output cable W1 at the Attenuator.
3. Disconnect controller-relay driver ribbon cable W19 from A20.
4. Remove the 13 #6 screws holding the Attenuator.

Removing the A22 Delay Cable Assembly 5-22.

Proceed as follows to remove the A22 Delay Cable Assembly:

WARNING

THE SYNTHESIZER MODULE IS HEAVY AND MAY CAUSE INJURY IF IT COLLAPSES. READ THE INSTRUCTIONS ON THE DECAL AFFIXED TO THE MODULE OR THE PROCEDURE IN THIS MANUAL BEFORE RAISING OR LOWERING THE MODULE.

1. Raise the synthesizer module.
2. Remove the #6 screws holding the bottom synthesizer module cover, and remove the cover.
3. Remove plug-in capacitor C1 and resistor R1, which are between the A22 Delay Cable PCA and the A2 Coarse Loop PCA.

NOTE

When reinstalling C1, make sure to put it between J1 on the A22 Delay Cable assembly and J9 on the A2 Coarse Loop. J2 on A22 and J10 on the A2 PCA are not used.

4. Remove the four #6 screws holding the A25 Discriminator PCA. Do not remove the screws holding the clamp that attaches the delay line to the PCA.
5. Remove the two #6 screws holding the lower delay cable retainer.
6. Remove the two #6 screws holding the upper delay cable retainer that holds the A26 Delay Cable PCA in place. Do not remove the screws holding the clamp that attaches the delay line to the PCA; do not disconnect the SMA connector on the semi-rigid trim cable.
7. Remove the A22 Delay Line assembly.

Section 6
Circuit Description, Troubleshooting, and Alignment

INTRODUCTION 6-1.

Section 6 describes the component-level circuit operation of the 6080A Synthesized Signal Generator. In addition, this portion of the manual includes troubleshooting information and procedures for adjusting the circuit assemblies.

There are seven parts to Section 6: 6A through 6F, and this introductory section. Sections 6A through 6F are laid out similarly to each other. Each section contains a detailed circuit description, followed by troubleshooting information, and finally by adjustment procedures where they apply.

This introductory section presents additional information needed to replace assemblies, perform tests, decipher codes, and understand diagnostic functions. Since the information in these paragraphs applies to Sections 6A through 6E, we recommend that you read the rest of this section before proceeding. This section covers the following major topics:

- Troubleshooting the 6080A

  General troubleshooting practices and information as they relate to the 6080A, plus parts replacement information.

- Module Replacement

  Procedures for obtaining a replacement module, including part numbers for the assemblies. Also brief overview of adjustments necessary for each module.

- Updating Compensation Memory With Module Exchange Data

  A procedure for transferring the compensation data to the new EPROM after exchanging a module.

- Self Tests Descriptions

  Explanation of the power-up self tests and their codes.

- Status Signals and Status Codes

  A listing of hardware status signals and their codes.

- Software Diagnostic Functions

  Descriptions of the built-in diagnostic functions.

Once you have determined the cause of the failure, proceed in one of the following three ways:

1. Return the failed Signal Generator to an authorized Fluke Service Center (refer to Section 8 for Service Center locations).
2. Identify the failed module and replace it through the Module Exchange Center (refer to the Module Replacement paragraph in this section).
3. Troubleshoot and replace the failed components. Refer to Section 8 for part numbers and other ordering information when ordering components.

Refer to the information in the rest of this section to help you determine which module or component has failed.

TROUBLESHOOTING THE 6080A 6-2.

Signal Generator failures may be caused by any of several conditions: operator error, out-of-specification performance, or by catastrophic failure. The functional block diagram, Figure 6-1, and the troubleshooting tree, Figure 6-2, will aid you in determining the cause of the Signal Generator malfunction.

Once you have isolated the problem to a specific area or circuit, the functional descriptions in Section 2, the information contained in this section, and the schematics in Section 10 will help you isolate the defective module or component. The Signal Generator must perform according to the specifications in Table 1-1 to be considered repaired and working properly.

Most operator errors are indicated by either a steady or flashing STATUS indicator or by the REJ ENTRY front panel display annunciator. However, some operator errors are not indicated this way, and may be mistaken for out-of-specification conditions. If you suspect an operator error, review the operating instructions in the Operator Manual.

Use the performance tests (Section 3, Performance Tests) to determine which parameters need adjustment. You can usually correct out-of-specification performance by performing the appropriate calibration procedure. (Refer to Section 4, Closed-Case Calibration.)

If the problem is not caused by an operator error and cannot be corrected by calibration, the Signal Generator has suffered a catastrophic failure. The STATUS and Self-Test failure codes usually provide a good indication of the cause of the failure. Use the troubleshooting tree along with the detailed troubleshooting information and the performance tests to help isolate the failure.

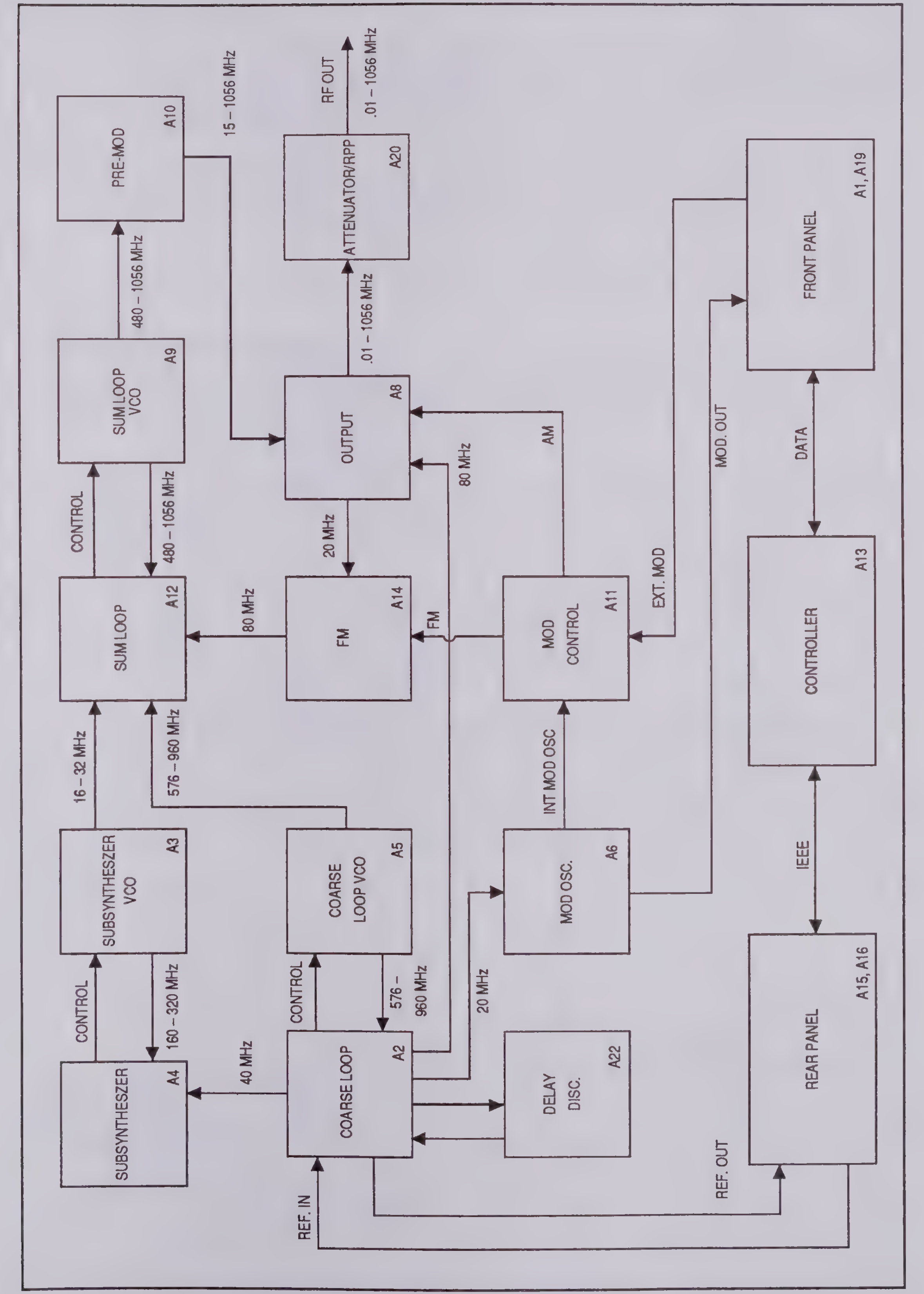

PRE-MOD
A10
15 – 1056 MHz
RF OUT
.01 – 1056 MHz
ATTENUATOR/RPP
A20
480 – 1056 MHz
.01 – 1056 MHz
FRONT PANEL
A1, A19
SUM LOOP VCO
A9
OUTPUT
A8
AM
MOD. OUT
CONTROL
480 – 1056 MHz
80 MHz
DATA
20 MHz
EXT. MOD
SUM LOOP
A12
80 MHz
FM
A14
FM
MOD CONTROL
A11
CONTROLLER
A13
16 – 32 MHz
576 – 960 MHz
INT MOD OSC
IEEE
SUBSYNTHESZER VCO
A3
COARSE LOOP VCO
A5
MOD OSC.
A6
CONTROL
160 – 320 MHz
CONTROL
576 – 960 MHz
20 MHz
SUBSYNTHESZER
A4
40 MHz
COARSE LOOP
A2
DELAY DISC.
A22
REAR PANEL
A15, A16
REF. OUT
REF. IN

Figure 6-1. Functional Block Diagram

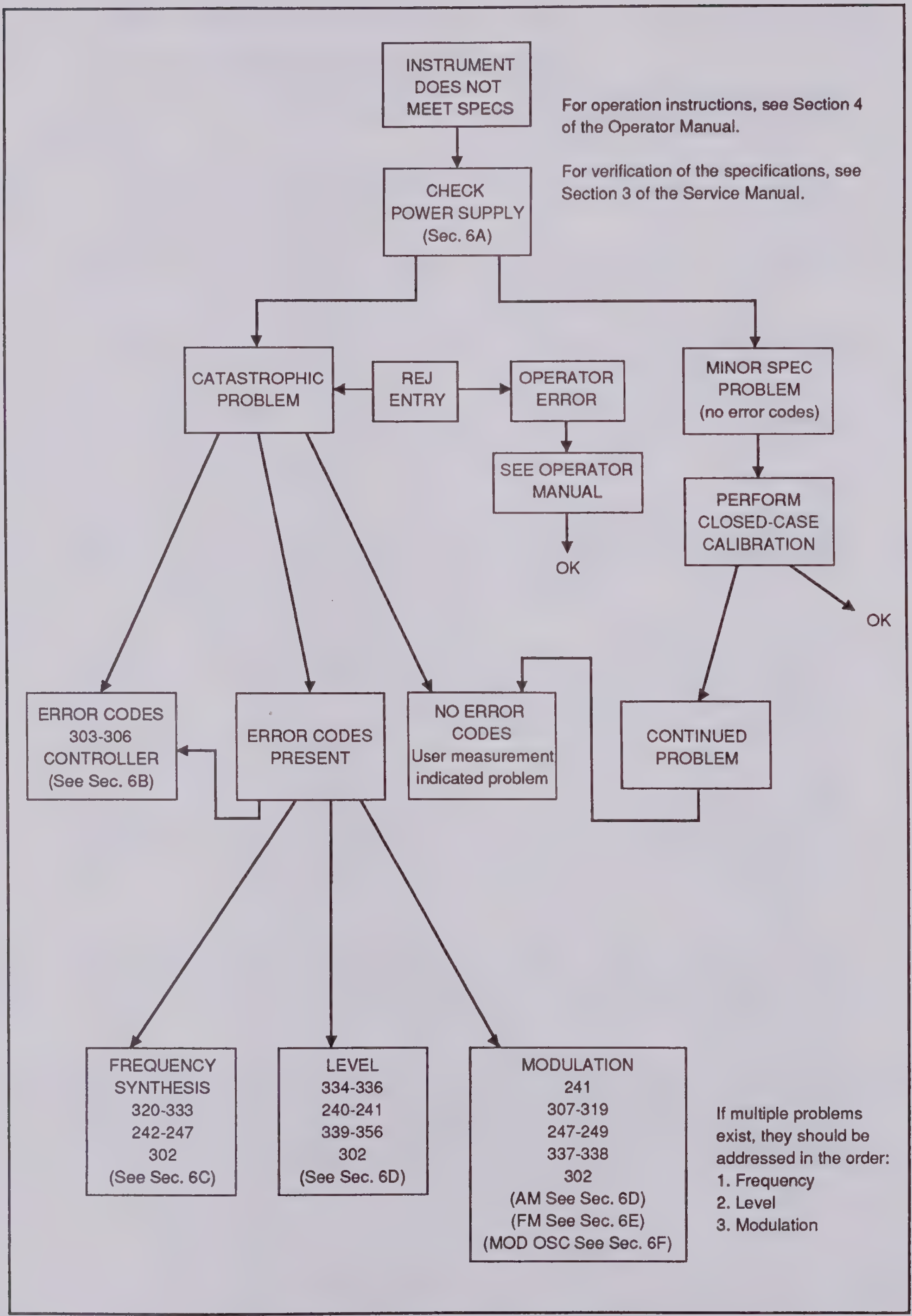

INSTRUMENT DOES NOT MEET SPECS
For operation instructions, see Section 4 of the Operator Manual.
For verification of the specifications, see Section 3 of the Service Manual.
CHECK POWER SUPPLY (Sec. 6A)
CATASTROPHIC PROBLEM
REJ ENTRY
OPERATOR ERROR
MINOR SPEC PROBLEM (no error codes)
SEE OPERATOR MANUAL
OK
PERFORM CLOSED-CASE CALIBRATION
OK
ERROR CODES 303-306 CONTROLLER (See Sec. 6B)
ERROR CODES PRESENT
NO ERROR CODES User measurement indicated problem
CONTINUED PROBLEM
FREQUENCY SYNTHESIS 320-333 242-247 302 (See Sec. 6C)
LEVEL 334-336 240-241 339-356 302 (See Sec. 6D)
MODULATION 241 307-319 247-249 337-338 302 (AM See Sec. 6D) (FM See Sec. 6E) (MOD OSC See Sec. 6F)
If multiple problems exist, they should be addressed in the order:
1. Frequency
2. Level
3. Modulation

Figure 6-2. Instrument Troubleshooting Tree

Parts Replacement 6-3.

Most parts are replaced using ordinary methods. However, when replacing surface-mount components, use a 600° F soldering iron (such as an Ungar 50T7) with a number 76 heater, a number 88 tip, and 2% silver solder paste (such as Electro Science Fabrication SP-37D1, or similar wire solder).

See appropriate sections of this manual for information on components that require alignment, compensation, and/or calibration when they are replaced. Use the performance tests in Section 3 to verify the results of the repairs.

Refer to Section 8 for part numbers and other ordering information when ordering components.

MODULE REPLACEMENT 6-4.

Figure 6-3, Assembly Location Block Diagram, illustrates the physical layout of the 6080A assemblies. This layout indicates how the pca's are interconnected and illustrates signal flow between assemblies.

To order a replacement module through the Module Exchange Center, use Table 6-1 to locate the part number for the assembly. This table identifies all assemblies that are available as a module exchange part.

The access procedures in Section 5 provide instructions for removing and replacing modules. The paragraphs under Module Replacement in this section describe the replaceable modules, and state whether adjustments are necessary after you install a replacement module in the Signal Generator. Refer to Sections 6A through 6F for details on troubleshooting and aligning the modules.

After replacing (and aligning if necessary) a module, proceed to Section 3 and perform the related performance tests to ensure that the failure has been fixed.

After verifying that the replacement module corrects the problem, pack the failed module in the shipping container (use the prepaid return shipping papers and label), and return it to your nearest Fluke Service Center.

A1 Display PCA 6-5.

Adjustments: None.

A2 Coarse Loop PCA 6-6.

Adjustments: None.

Perform Reference Oscillator Calibration as described under the heading with the same title in Section 4.

A3 Subsynthesizer VCO PCA 6-7.

Adjustments:

- R106 on Subsynthesizer PCA. See "SSB Mixer LO Drive Adjustment, R106" in Section 6C.
- R99 on the Subsynthesizer PCA. See "Lower Clamp Adjustment" in Section 6C.

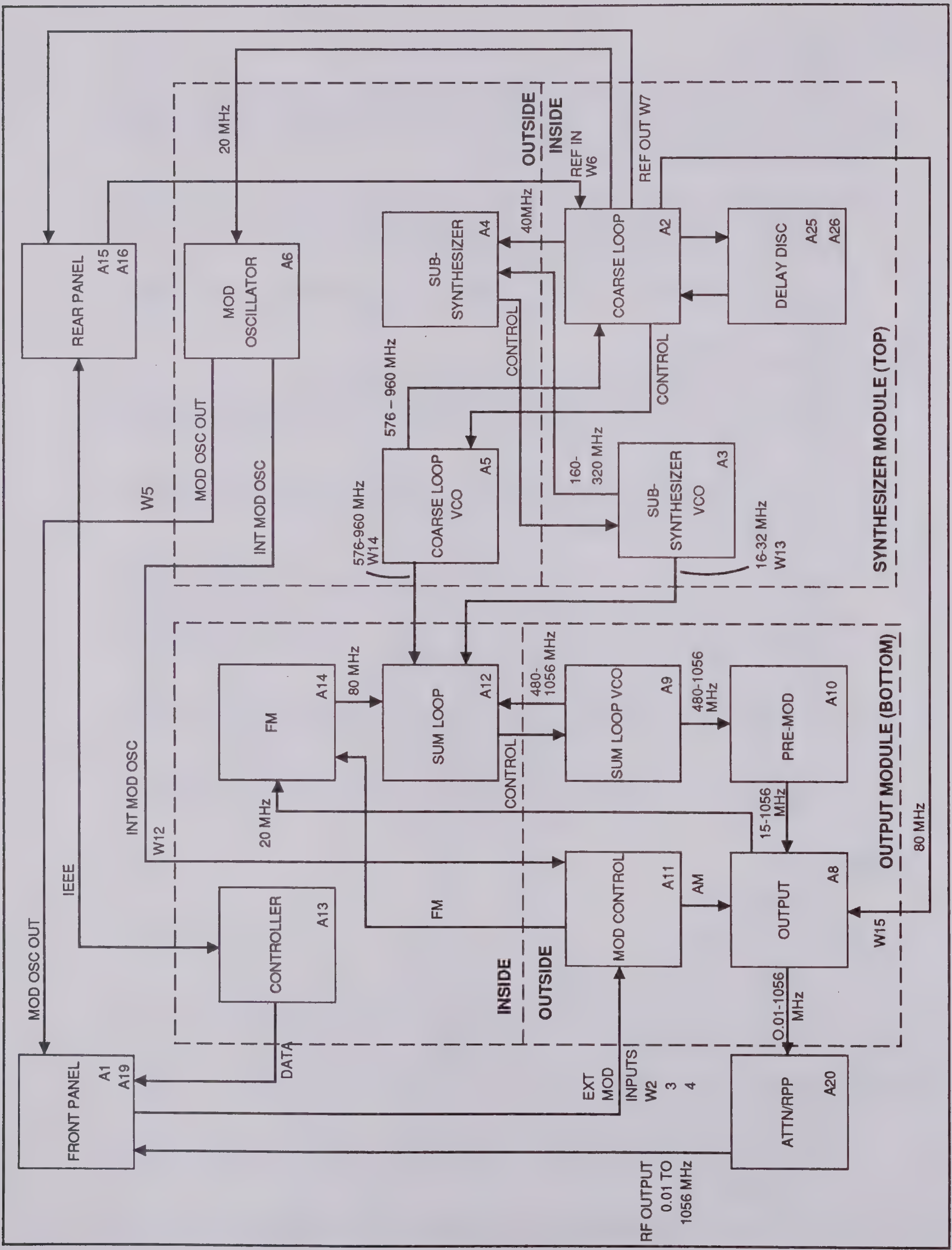

REAR PANEL
A15
A16
MOD OSCILLATOR
A6
20 MHz
W5
MOD OSC OUT
INT MOD OSC
OUTSIDE
INSIDE
REF IN W6
REF OUT W7
40MHz
SUB-SYNTHESIZER
A4
COARSE LOOP
A2
DELAY DISC
A25
A26
CONTROL
CONTROL
576 – 960 MHz
COARSE LOOP VCO
A5
576-960 MHz W14
160-320 MHz
SUB-SYNTHESIZER VCO
A3
16-32 MHz W13
SYNTHESIZER MODULE (TOP)
INT MOD OSC
W12
IEEE
MOD OSC OUT
FM
A14
80 MHz
SUM LOOP
A12
480-1056 MHz
SUM LOOP VCO
A9
480-1056 MHz
PRE-MOD
A10
20 MHz
CONTROL
15-1056 MHz
OUTPUT MODULE (BOTTOM)
80 MHz
CONTROLLER
A13
FM
MOD CONTROL
A11
AM
OUTPUT
A8
W15
INSIDE
OUTSIDE
0.01-1056 MHz
DATA
FRONT PANEL
A1
A19
EXT MOD INPUTS W2 3 4
ATTN/RPP
A20
RF OUTPUT 0.01 TO 1056 MHz

Figure 6-3. Assembly Location Block Diagram

Table 6-1. 6080A Module Exchange Assemblies

ASSEMBLY NO.	MEC P/N	DESCRIPTION
A1	882068	Display PCA
A2	882071	Coarse Loop PCA
A3	882076	Subsynthesizer VCO PCA
A4	882084	Subsynthesizer PCA
A5	882089	Coarse Loop VCO PCA
A6	882097	Mod Oscillator PCA
A7	882022	Relay Driver PCA
A8	882030	Output PCA
A9	882035	Sum Loop VCO PCA
A10	882055	Premodulator PCA
A11	882063	Mod Control PCA
A12	882043	Sum Loop PCA
A13	882048	Controller PCA
A14	882050	FM Board PCA
A15	882100	Power Supply PCA
A19	860858	Switch PCA
A20	860812	Attenuator/RPP Assembly (A7+A21
A22	860887	Delay Line Assembly (A25+A26+Delay Cable+Trim Cable

- R98 on the Subsynthesizer PCA. See “Upper Clamp Adjustment” in Section 6C.

A compensation data EPROM containing VCO tuning data is included. See “Updating Compensation Memory With Module Exchange Data” in this section for data transfer instructions.

A4 Subsynthesizer PCA 6-8.

Adjustments:

- R106 on the Subsynthesizer PCA. See “SSB Mixer LO Drive Adjustment, R106” in Section 6C.
- R99 on the Subsynthesizer PCA. See “Lower Clamp Adjustment” in Section 6C.
- R98 on the Subsynthesizer PCA. See “Upper Clamp Adjustment” in Section 6C.

Perform Reference Oscillator Calibration as described under the heading with the same title in Section 4.

A5 Coarse Loop VCO PCA 6-9.

Adjustments: None.

Perform Coarse Loop compensation as described in Section 7.

A6 Mod Oscillator PCA 6-10.

Adjustments: None.

A7 Relay Driver PCA 6-11.

Adjustments: None.

A8 Output PCA 6-12.

Adjustments:

- R28, detector offset/linearity. See "Mod Control PCA Detector Offset Adjustment, R28" in Section 6D.
- R20, RF Level adjustment. See "Mod Control PCA RF Level Adjustment, R20" in Section 6D.
- R10, AM Depth adjustment. See "Mod Control PCA AM Depth Adjustment, R10" in Section 6D.
- R96, Q16 Bias adjustment. See "Output PCA Q16 Bias Adjustment, R96" in Section 6D.

A compensation data EPROM containing Output PCA level correction data is included. See "Updating Compensation Memory With Module Exchange Data" in this section for data transfer instructions.

A9 Sum Loop VCO PCA 6-13.

Adjustments:

- R51 and C7 on the A10 Premodulator PCA, AM bandwidth adjustment. See "Premodulator PCA Bandwidth Adjustment, R51 and C7" in Section 6D.
- R23, Amplifier gain adjustment. See "Sum Loop VCO Assembly Adjustment" in Section 6C.

Perform Sum Loop compensation as described in Section 7.

A10 Premodulator PCA 6-14.

Adjustments: R51, 256 to 1056 MHz level adjustment. See "Premodulator PCA Level Adjustment, R51" in Section 6D.

A11 Modulation Control PCA 6-15.

Adjustments:

- R28, detector offset/linearity. See "Mod Control PCA Detector Offset Adjustment, R28" in Section 6D.
- R20, RF Level adjust. See "Mod Control PCA RF Level Adjustment, R20" in Section 6D.
- R10, AM Depth adjust. See "Mod Control PCA AM Depth Adjustment, R10" in Section 6D.

A12 Sum Loop PCA 6-16.

Adjustments:

- R23, Amplifier gain adjustment. See "Sum Loop VCO Assembly Adjustment" in Section 6C.
- R116, FM null adjustment. See "FM Null Adjustment, R116" in Section 6C.

A13 Controller PCA 6-17.

Adjustments: None.

To preserve the instrument calibration/compensation data, transfer the battery backed RAM IC U8 and the EEPROM U9 from the old Controller PCA to the replacement controller. If either U8 or U9 are bad, review "Calibration/Compensation Memory" (Section 6B) then replace the faulty IC.

A14 FM Board PCA 6-18.

Adjustments:

- R107, FM deviation high-rate. See "Alignment of FM PCA (A14)" in Section 6E.
- R39, HIDEV volts/steering. See "Alignment of FM PCA (A14)" in Section 6E.
- R35, LOWDEV volt/steering. See "Alignment of FM PCA (A14)" in Section 6E.
- R116 on Sum Loop PCA. See "FM Null Adjustment, R116" in Section 6C.

A15 Power Supply PCA 6-19.

Adjustments: None.

A19 Switch PCA 6-20.

Adjustments: None.

A20 Attenuator/RPP Assembly (A7, A21, A30) 6-21.

Adjustments: R20, RF Level. See "Mod Control PCA RF Level Adjustment, R20" in Section 6D.

A compensation data EPROM containing Attenuator/RPP level correction data is included. See "Updating Compensation Memory With Module Exchange Data" in this section for data transfer instructions.

A22 Delay Line Assembly (A25, A26, Delay Cable, Trim Cable) 6-22.

Adjustments: None.

UPDATING COMPENSATION MEMORY WITH MODULE EXCHANGE DATA 6-23.

After installing the A20 Attenuator/RPP, A8 Output, or A3 Subsynthesizer VCO module exchange assemblies, load the data from the corresponding compensation EPROM into the compensation memory. The module exchange EPROM is installed in a socket on the A13 Controller PCA. Transfer the compensation data by one of three special functions, depending on which of the three assemblies has been replaced.

Perform the following steps to update the compensation memory with the new module exchange data:

1. Verify that the power to the 6080A Signal Generator is turned off.
2. Access the A13 Controller PCA as described by the access procedure in Section 5. Leave the controller in place with all cables attached since it must be operational.
3. Install the module exchange EPROM into the socket on the controller labeled U10.
4. Power up the 6080A.
5. Remove the sticker labeled "CAL|COMP" from the rear panel and set the CAL|COMP switch to the "1" position.
6. Verify that the CAL and COMP annunciators on the front panel are flashing.
7. Enter Special Function 961 to transfer the Attenuator/RPP data, Special Function 962 to transfer the Output data, or Special Function 963 to transfer the Subsynthesizer VCO data.
8. Respond to the prompt "Att Sto?", "Out Sto?" or "Sub Sto ?" by pressing the STO key.

   The message "—Sto—" is displayed for 12 seconds for the Attenuator, and 5 seconds for the Output and Subsynthesizer while the data is transferred.

CAUTION

Do not turn the POWER switch off or change the CAL|COMP switch until the store operation is complete. Doing so could damage the contents of the compensation memory.

9. Set the rear panel CAL|COMP switch to the "0" position.
10. Verify that the CAL and COMP annunciators no longer flash.
11. Turn the power off and remove the module exchange EPROM, if desired.
12. Reassemble the instrument by reversing the disassembly steps.

SELF TEST DESCRIPTION 6-24.

Instrument self tests are automatically performed on power-up or when initiated by Special Function 02. If any test fails, the message "FAIL" displays along with the corresponding status code. A complete list of the test failures displays upon completion. Use the STATUS key to scroll the list if there are more than four failures.

During the tests, the RPP relay opens to protect instruments connected to the RF OUTPUT from possible damage. The RF output (334-336) and pulse modulator (337 and 338) tests are not performed at power-up or by Special Function 02 because signals as high as -20 dBm may be present at the RF output connector during these tests. Use Special Function 06 to perform a complete self test including the RF output and pulse modulator tests.

Special Function 904 runs the self tests in a troubleshooting mode. The software stops after each test that fails, leaving the hardware in the test configuration and the error code in the display. The RF OUTPUT is enabled so measurement equipment can be connected. Press any key to continue the test.

You can display self test results (see Table 6-2) by entering Special Function 03. Status code 00 indicates no failures. Status code 301 indicates the tests were aborted before completion; therefore, the reported results may be incomplete.

Digital Tests 6-25.

The digital tests (see Table 6-3) perform basic checks of the circuitry on the A13 Controller PCA.

The calibration/compensation memory test verifies the CRC checksums of each calibration/compensation data segment in the battery-backed RAM (U8) and in the EEPROM (U9). If any of the tests fail, status code 302 is reported. See "Calibration/ Compensation Memory Status" in Section 6B for further details.

The system RAM (U6 and U7) is tested at power-up by writing data to each memory location and verifying that the same data can be read back. The four program EPROMs (U2, U3, U4 and U5) are tested by verifying their checksums. The nonvolatile RAM is tested by verifying the checksum of each memory location.

Communication with the IEEE-488 interface IC is verified by writing data to the IEEE-488 talker/listener IC (U28), then reading it back.

AM Tests 6-26.

The AM tests program normal and overmodulation conditions and then check the state of the ALC loop-leveled indicator. Table 6-4 lists the test conditions.

FM Tests 6-27.

The FM tests program normal and overmodulation conditions, then check the state of the FM loop-lock indicator. The locked condition is expected in four of the FM bands and once with the Low-Rate FM mode enabled. The unlocked condition is expected when a very wide deviation is programmed at a low modulation rate. Table 6-5 lists the test conditions.

ϕM Tests 6-28.

The phase modulation tests verify that the FM loop remains locked when two valid phase modulation settings are programmed. The first test is performed at a high deviation. The second test is performed with the high-rate ϕM mode enabled. Table 6-6 lists the test conditions.

DC FM Test 6-29.

The dc FM test (see Table 6-7) verifies the operation of the DC FM status indicator. This indicator reports the relative position of the dc FM dac setting to the corresponding ac FM control voltage. When the dc FM dac is set to full scale, the indicator should report that it is too high.

Coarse Loop Tests 6-30.

The first three Coarse Loop tests in Table 6-8 program a frequency in each of the three coarse loop vco bands with the normal steering dac value. The loop should remain locked. The fourth test in the table programs a valid frequency but the steering dac is set to zero. This should force the loop to unlock.

Subsynthesizer Tests 6-31.

The first Subsynthesizer test in Table 6-9 programs a valid frequency near the center of the Subsynthesizer range and expects the Subsynthesizer to remain locked. The next two tests in the table force the Subsynthesizer to frequencies outside of its normal operating range with the expectation that it will unlock.

Sum Loop Tests 6-32.

The first four Sum Loop tests in Table 6-10 program a frequency in each of the four Sum Loop VCO bands with the normal steering dac value with the expectation the loop will remain locked. The fifth test in the table programs a valid frequency but the steering dac is set to zero. This should force the loop to unlock.

The next two tests program 4 MHz of FM deviation at a low and a high modulation rate and with the expectation that the sum loop will remain locked.

RF OUTPUT Tests 6-33.

The RF output tests (see Table 6-11) verify the presence of an RF signal at the output of the Attenuator/RPP assembly. The sensitivity of the RPP detection circuitry is increased so that it can be used as a RF signal detector. The first test programs a high RF level at a frequency in the fundamental frequency band with the expectation that the RPP indicator will trip. The second test programs a high RF level at a frequency in the HET frequency band with the expectation that the RPP indicator will trip. The third test programs a level below the detector threshold with the expectation that the indicator will not trip.

Pulse Modulator Tests 6-34.

The Pulse Modulator Tests (see Table 6-12) configure the RPP circuitry to its high sensitivity mode as in the RF output tests. The first test programs a high RF level and enables the internal pulse. The internal modulation oscillator sends a steady logic "low" to the pulse modulator; therefore, the pulse modulator will attenuate the RF output, and the RPP indicator will not trip. The second test configures the mod oscillator to send a steady logic high to the pulse modulator; therefore, the pulse modulator will not attenuate the RF output, and the RPP indicator will trip.

Filter Tests 6-35.

The Filter Tests (see Table 6-13) verify the selection and operation of each of the output filter and divider sections. The first group of tests program a frequency within the band of interest and programs the correct filter and divider settings. The ALC loop-leveled indicator should report that the loop is leveled.

The next group of tests program filter settings that do not correspond with the programmed frequency. The ALC loop-leveled indicator should report that the loop is unleveled.

STATUS SIGNALS AND STATUS CODES 6-36.

Table 6-14. lists the major hardware status signals monitored by the software and the corresponding front panel status code.

SOFTWARE DIAGNOSTIC FUNCTIONS 6-37.

The instrument software includes built-in diagnostic functions to aid troubleshooting and alignment.

Digital Control Latch Test 6-38.

Special Function 903, the Latch Test, generates continuous activity on the data and address busses on the analog circuit boards so the activity can be monitored with an oscilloscope.

When the test is initiated, the message “LAtch AA” is displayed, and the bit pattern 10101010 (Hexadecimal AA) is written continuously to each of the decoded module I/O latch positions. The data is written to each address in sequence so that the activity on the address bus is regular. Pressing the STEP ▽ key changes the displayed message to “LAtch 55”, and the bit pattern is changed to 01010101 (Hexadecimal 55). Pressing the STEP △ key changes the pattern back to 10101010. Press any other key to exit.

Instrument Diagnostic State 6-39.

Special Function 909 programs the instrument to a predefined state used by several of the troubleshooting and alignment procedures. First, the instrument preset state (Special Function 01) is programmed to disable most special functions. Then, the diagnostic state is programmed immediately. The significant parameter settings of the diagnostic state are listed in Table 6-15.

Set Internal DACs 6-40.

All internal dac’s can be simultaneously forced to a predetermined setting for troubleshooting and alignment by special function. The settings are described in Table 6-16.

NOTE: The Synthesizer DAC (U7) on the A6 Modulation Oscillator PCA cannot be set to mid scale with Special Function 942.

Display Synthesizer Loop Frequencies 6-41.

The sum loop, coarse loop, and Subsynthesizer frequencies for the programmed RF output frequency can be displayed by the Special Functions in Table 6-17.

Table 6-2. General Self Test Results

CODE	DESCRIPTION
00	No self test failures
301	Self tests aborted

Table 6-3. Digital Test Results

CODE	DESCRIPTION
302	Calibration/compensation memory checksum test failed
303	RAM test failed
304	EPROM test failed
305	Nonvolatile memory test failed
306	IEEE interface test failed

Table 6-4. AM Test Conditions

CODE	AM DEPTH	AMPLITUDE	EXPECTED STATE OF ALC LOOP
307	30.0%	+13.7 dBm	Leveled
308	0.0%	+16.0 dBm	Leveled
309	> 99.9%	> +20.0 dBm	Unleveled

RF Frequency = 1055 MHz
Mod Frequency = 1 kHz
Internal AM = On

Table 6-5. FM Tests

CODE	FM DEV	MOD FREQ	LOW-RATE FM	EXPECTED STATE OF FM LOOP
310	100 kHz	1 kHz	Off	Locked
311	4 MHz	30 Hz	Off	Unlocked
312	4 MHz	63 Hz	Off	Locked
313	20 kHz	1 kHz	Off	Locked
314	10 kHz	1 kHz	Off	Locked
315	60 kHz	30 Hz	On	Locked

RF Frequency = 640 MHz
RF Amplitude = 0 dBm
Mod Frequency = 1 kHz
Internal FM = On

Table 6-6. Phase Modulation Test Conditions

CODE	PM DEV	MOD FREQ	HIGH-RATE ϕM	EXPECTED STATE OF FM LOOP
316	100 rad	1 kHz	Off	Locked
317	10 rad	20 kHz	On	Locked
RF Frequency = 640 MHz RF Amplitude = 0 dBm Mod Frequency = 1 kHz Internal ϕM = On				

Table 6-7. DC FM Tests

CODE	DCFM DAC	EXPECTED STATE OF DCFM HI/LO INDICATOR
319	4095	High
RF Frequency = 640 MHz RF Amplitude = 0 dBm		

Table 6-8. Coarse Loop Tests

CODE	COARSE LOOP FREQUENCY	COARSE STEER DAC	EXPECTED STATE OF COARSE LOOP
320	640 MHz	Normal	Locked
321	768 MHz	Normal	Locked
322	896 MHz	Normal	Locked
323	640 MHz	0	Unlocked

Table 6-9. Subsynthesizer Tests

CODE	RF FREQUENCY	SUBSYNTHESIZER FREQUENCY	EXPECTED STATE OF SUBSYNTHESIZER
324	804.000000 MHz	240 MHz	Locked
325	800.000000 MHz	120 MHz	Unlocked
326	807.999999 MHz	350 MHz	Unlocked

Table 6-10. Sum Loop Tests

CODE	FREQUENCY	SUM STEER DAC	INT FM	FM DEV	MOD FREQ	EXPECTED STATE OF SUM LOOP
327	550 MHz	Normal	Off	-	-	Locked
328	700 MHz	Normal	Off	-	-	Locked
329	830 MHz	Normal	Off	-	-	Locked
330	975 MHz	Normal	Off	-	-	Locked
331	550 MHz	0	Off	-	-	Unlocked
332	800 MHz	Normal	On	4 MHz	50 kHz	Locked
333	800 MHz	Normal	On	4 MHz	63 Hz	Locked

Table 6-11. RF Output Tests

CODE	RF FREQUENCY	AMPLITUDE	EXPECTED STATE OF RPP INDICATOR
334	800 MHz	+16 dBm	Tripped
335	1 MHz	+16 dBm	Tripped
336	800 MHz	+7 dBm	Not tripped

Table 6-12. Pulse Modulator Tests

CODE	RF FREQUENCY	AMPLITUDE	PULSE CONTROL LOGIC LEVEL	EXPECTED STATE OF RPP INDICATOR
337	800 MHz	+16 dBm	Low	Not tripped
338	800 MHz	+16 dBm	High	Tripped

Table 6-13. 6080A Filter Tests

CODE	FREQUENCY	FREQ BAND	EXPECTED STATE OF ALC LOOP
339	20 MHz	15 to 22 MHz	Leveled
340	30 MHz	22 to 32 MHz	Leveled
341	40 MHz	32 to 47 MHz	Leveled
342	60 MHz	47 to 64 MHz	Leveled
343	100 MHz	64 to 128 MHz	Leveled
344	150 MHz	128 to 180 MHz	Leveled
345	200 MHz	180 to 256 MHz	Leveled
346	300 MHz	256 to 350 MHz	Leveled
347	400 MHz	350 to 512 MHz	Leveled
348	550 MHz	512 to 625 MHz	Leveled
349	650 MHz	625 to 730 MHz	Leveled
350	800 MHz	730 to 1056 MHz	Leveled
351	100 MHz	15 to 22 MHz	Unleveled
352	100 MHz	22 to 32 MHz	Unleveled
353	100 MHz	32 to 47 MHz	Unleveled
354	200 MHz	47 to 64 MHz	Unleveled
355	500 MHz	256 to 350 MHz	Unleveled
356	1024 MHz	512 to 730 MHz	Unleveled
Amplitude = 15.0 dBm			

Table 6-14. 6080 Status Signals and Codes

ASSEMBLY	STATUS CODE	SIGNAL	DESCRIPTION
A7 Attenuator/RPP	240	RPTRPL	RPP tripped
A10 Premodulator	241	ALCUNLVL	ALC loop unleveled or AM overmodulation
A4 Subsynthesizer	242	SUBUNLKL	Subsynthesizer unlocked
A2 Coarse Loop	243	CORUNLKL	Coarse loop unlocked
A12 Sum Loop	244	SUMUNLKL	Sum loop unlocked
A12 Sum Loop	245	SUMUNLVL	Sum loop unleveled
A2 Coarse Loop	246	REFUNLKL	Reference loop unlocked
A14 FM loop	247	FMUNLKL	FM loop unlocked or FM overmodulation

Table 6-15. Special Function 909 Diagnostic State Parameter Settings

PARAMETER	SETTINGS
Frequency	300 MHz
Amplitude	-10.0 dBm
AM Depth	30.0 %
FM Deviation	5.00 kHz
Mod Frequency	1.00 kHz
All Modulation	Off

Table 6-16. Special Functions for Setting DACs

CODE	FUNCTION
941	Set all dac's to zero
942	Set all dac's to mid scale
943	Set all dac's to full scale

Table 6-17. Special Functions for Displaying Internal Frequencies

CODE	FUNCTION
945	Display Sum Loop frequency
946	Display Coarse Loop frequency
947	Display Subsynthesizer frequency

Section 6A
Power Supply

POWER SUPPLY BLOCK DIAGRAM 6A-1.

Refer to the Power Supply Block Diagram, Figure 6A-1, to identify the major functional sections of the power supply and for help in following the power and current paths of the power supply.

POWER SUPPLY CIRCUIT DESCRIPTION 6A-2.

Refer to the Power Supply schematic diagram in Section 10 while reading this description. The power supply provides all dc and ac power requirements for the Signal Generator. DC power is supplied to all system circuitry and operates the dc fan. AC power is used for filament heat for the front panel display.

The line voltage selector card, located in the case (rear panel) of the line fused receptacle/filter, accommodates the various line voltages that the instrument operates from. The card can be installed in any one of four configurations to allow selection of one of the following line voltages: 100, 110, 220, or 240V ac.

Line power passes through the line filter and fuse and is then routed to the primary winding of the power transformer. The transformer includes an additional safety device, which serves as a thermal shutoff to break the primary ac supply in case the transformer exceeds its safe operating temperature.

The secondary windings of the transformer are connected to a linear dc power supply assembly that provides the instrument with the supplies shown in Table 6A-1.

The front panel POWER pushbutton switches the instrument between the operate and standby modes. Note that the standby (STBY) mode, indicated by the illuminated yellow LED, does not remove power from the instrument. Two supplies continue to be active in the standby mode: the 23.4V supply and the display filament lines. Additionally, parts of the power supply, including the transformer secondary windings, rectifiers, and filter capacitors, are still energized.

Figure 6A-1 shows bridge rectifier configurations as well as the component designations for the various supplies. Rectifiers in the power supply are used in both a bridge and full-wave center-tapped configurations with capacitor input filters.

The +24V, +23.4V, -5V, 37V, and +30V supplies use conventional three-terminal IC regulators with internal current-limit and temperature protection.

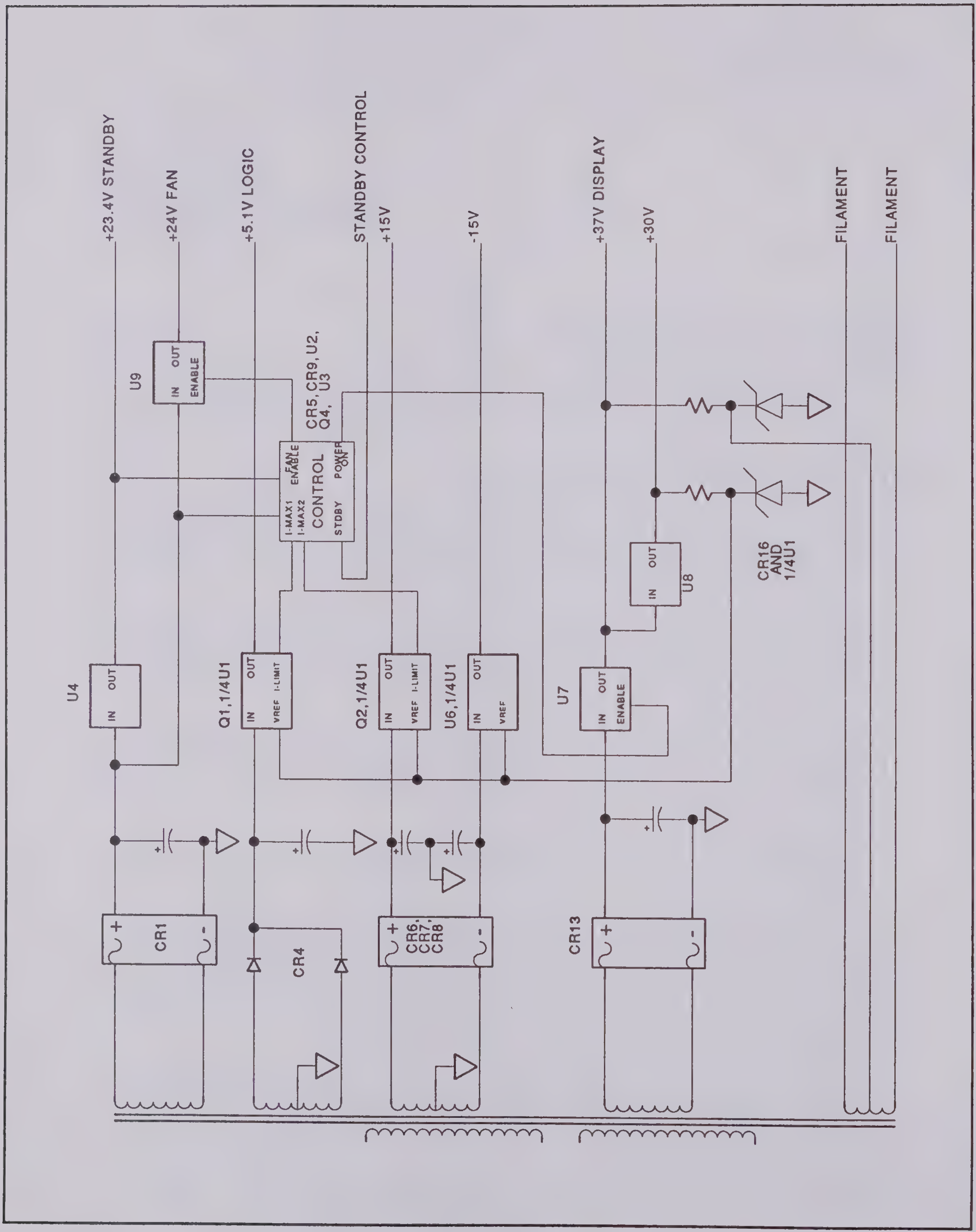

+23.4V STANDBY
+24V FAN
+5.1V LOGIC
STANDBY CONTROL
+15V
-15V
+37V DISPLAY
+30V
FILAMENT
FILAMENT
U9
IN
ENABLE
OUT
CR5, CR9, U2, Q4, U3
FAN ENABLE
I-MAX1
I-MAX2
CONTROL
STDBY
POWER ON
U4
Q1, 1/4U1
VREF
I-LIMIT
Q2, 1/4U1
U6, 1/4U1
U7
U8
CR16 AND 1/4U1
CR1
CR4
CR6, CR7, CR8
CR13

Figure 6A-1. Power Supply Block Diagram

Table 6A-1. Supplies Provided by Power Supply Assembly

VOLTAGE	SUPPLY
+24V dc	Fan and Attenuator
+23.4V dc	Oven and Front Panel (Standby Supply)
+5.1V dc	Logic
+15V dc	Positive Analog
-15V dc	Negative Analog
+37V dc	Front Panel Display
+30V dc	High Voltage Analog
6V ac	Display Filament Lines

The two highest power regulators, +5.1V and +15V are very low noise, low ripple design. They use a high gain, low noise amplifier U1, in a closed loop circuit with high current sense FET transistors Q1 and Q2.

Overcurrent protection is provided to both the +5.1V and +15V supplies via sense FET series-pass element's (Q1 and Q2) internal current mirror, in conjunction with the differential amplifiers (U2). When the load current set by R6 or R18 exceeds the preset limit, zener diodes CR5 or CR9 turn on, triggering the gate of SCR Q4. This sets pin 5 of comparator U3 below its threshold voltage, set by R19 and R22. This sets the adjust terminal of the 37V regulator to -1.3V and turns off the 37V supply. When the 37V supply is turned off, the +30V, +5V reference, the +5.1V, +15V, and -15V supplies are also turned off. The 24V fan supply is not turned off on this current limit. Q4 acts as a memory element that requires resetting after it is turned on. This can be done by turning off the front panel POWER switch.

The +5V reference is adjusted to 5.10V (at TP6) via the supply adjustment potentiometer R41. This adjustment sets up the +5.1V, +15V, and -15V supplies. These supplies track the +5V reference.

The -15V supply is a low-noise, low-ripple design that uses a high-gain, low-noise amplifier (U1) in a closed-loop circuit with a conventional three-terminal IC regulator U6. This circuit provides current limit and temperature protection.

Diodes CR12 and CR14 protect the +15V and -15V regulated supplies from reverse voltages. CR20 protects the +5.1V supply from both reverse voltages and overvoltages.

A +6.2V supply is developed from the +37V supply through resistor R34 and zener diode CR15. The +6.2V supply is then applied to the center tap of the 6V ac filament supply. This provides the necessary grid bias for the front panel displays.

A -5V local supply (U5) is generated on the Power Supply PCA. This supply provides negative voltage to U1 and a -1.3V shut off voltage for U7, U9, and U3. Triac Q3 is a voltage surge protector that protects against line voltage surges as well as overvoltage in case the line power selector card is set incorrectly. When the voltage across the +5.1V secondary winding of the transformer is excessive, CR2 or CR3 conducts current and turns on the gate of Q3. When Q3 conducts, it shorts the secondary winding of the transformer and causes the power line fuse to blow.

To reduce power supply ripple, the common reference terminals of the voltage regulators are connected to an external ground point (P2) on the module section. To prevent damage to the power supply circuitry, all GND lines and the GND SENSE line are grounded to the chassis.

POWER SUPPLY TROUBLESHOOTING 6A-3.

WARNING

TO AVOID ELECTRIC SHOCK, USE EXTREME CAUTION WHEN TROUBLESHOOTING THE POWER SUPPLY. TURNING OFF THE FRONT PANEL POWER SWITCH DOES NOT REMOVE POWER FROM THE PCA. SOME POWER SUPPLY CIRCUITS REMAIN ENERGIZED AS LONG AS THE POWER CORD IS PLUGGED INTO AC LINE POWER.

To access the power supply, remove the rear panel from the instrument and remove the Power Supply PCA from its bracket.

Connect the GND lines and the GND SENSE lines to the controller connector (J4 pins 5,6,7) to reduce ground loops. Connect load resistors that correspond to the load current indicated on the power supply schematic to each of the voltage supply lines.

CAUTION

WHEN OPERATING THE POWER SUPPLY FOR LONGER THAN 5 MINUTES AT A TIME, MAKE SURE THE FAN IS AIMED AT THE POWER DISSIPATORS. FAILURE TO PROVIDE ADEQUATE AIR FLOW MAY DAMAGE POWER SUPPLY COMPONENTS.

Troubleshooting Procedure 6A-4.

Troubleshoot the power supply as described in the following procedure:

1. Set the power supply to the standby mode (front panel yellow LED on).

2. Verify that the two standby supplies are operating within their specified voltage ranges as listed below:

   - TP2, 23.4V supply = 24V (±5%)
   - TP14, -5V supply = -5V (±5%)

   Next verify all other supplies are turned off.

   - TP18, 24V supply = 0V (±0.1V)
   - TP6, +5.1V supply = 0V (±0.1V)
   - TP11, +15V supply = 0V (±0.1V)
   - TP16, -15V supply = 0V (±0.1V)
   - TP20, 37V supply = 0V (±0.1V)
   - TP21, 30V supply = 0V (±0.1V)
   - TP15, +5V reference = 0V (±0.1V)

   a. If either of the 23.4V or -5V supplies are not at the specified voltage, check the unregulated supplies (TP13 and TP1, respectively).

   b. If some of the supplies that are supposed to be off are partially or fully turned on, check the 37V supply (TP20) voltage.

   c. If the 37V supply is partially or fully on, check the standby switching circuit and the comparator operation (U3, Q5, R52).

3. Switch the power supply on by connecting the STANDBY line (J6 pin 4) to GND (J6 pin 7,8).

4. Verify that all supplies are operating and are within the following specified levels:

   - TP18, 24V supply = 24V (±5%)
   - TP2, 23.4V supply = 24V (±5%)
   - TP6, +5.1V supply = 5.1V (±2%)
   - TP11, +15V supply = 15V (±4%)
   - TP16, -15V supply = -15V (±4%)
   - TP14, -5V supply = -5V (±5%)
   - TP20, 37V supply = 37V (±5%)
   - TP21, 30V supply = 30V (±5%)
   - TP15, +5V reference = 5V (±3%)

   a. If all supplies are at the appropriate voltages when in standby, but are not at the appropriate voltages when the power supply is turned on, the shutoff circuit may have failed caused a voltage failure. Verify a second time that the standby supplies are 24V ±5% and -5V ±5%.

   b. If the 24V fan supply is on and the rest of the supplies (except for 23.4 and -5V) are off, check the current limit circuitry (U2, CR5, CR9, Q4). A short of either the +15 or the +5.1V line could cause the current limit to trip and turn all non-standby supplies off (except the fan supply). In this case, verify that the voltage at TP22 is less than 1V, which indicates a current limit trip. To recover from a current limit shutoff, turn the power supply to standby operation (power switch off) for at least 5 seconds.

   c. If only the +5V reference, +5.1V, +15V, and the -15V supplies are in error, check the +5V reference circuitry, since it is likely that the fault is with the reference supply circuitry, U1 and CR16.

POWER SUPPLY ADJUSTMENT PROCEDURE 6A-5.

A single potentiometer (R41) adjusts the voltage output of the three discrete supplies: the +5.1, +15, and -15V. To perform these adjustments, connect a voltmeter to the +5.1V supply (TP6), and adjust R41 for 5.1V (±0.05V). Once the +5.1V supply is adjusted, both the +15 and the -15V supplies should operate at 15V ±0.2V.

Section 6B
Digital Controller

DIGITAL CONTROLLER BLOCK DIAGRAM 6B-1.

The A13 Controller PCA, under the direction of the instrument software, handles the data interface between the front panel, remote interface, and 6080A functions. The controller is located in a top side compartment of the lower module section.

The controller consists of the following functional groups:

- Microprocessor
- Memory
- Memory Control
- Front Panel Interface
- IEEE-488 Interface
- Attenuator Control Interface
- Module I/O Interface
- Status and Control Latches

Refer to Figure 6B-1 to identify the major sections and trace signal paths.

DIGITAL CONTROLLER CIRCUIT DESCRIPTION (A13) 6B-2.

Microprocessor 6B-3.

The software is executed on a 68HC000 16-bit microprocessor. The 8-MHz digital system clock signal is generated by an oscillator made up of gates from U18 and crystal Y1.

Supply voltage monitor TL7705A (U13) generates the active low reset signal to the 68HC000. The reset signal is generated on power-up or when the +5V supply drops below +4.5V. The reset signal remains low for 200 ms.

Memory 6B-4.

The program instructions and constant data are stored in four 128-KB EPROMs, U2-U5. The stack and program variables are stored in two 32-KB static RAMs U6 and U7. Nonvolatile instrument state memory and one half of the redundant calibration/compensation memory are contained in battery-backed CMOS RAM U8. The other half of the redundant calibration/compensation memory is contained in EEPROM U9.

The rear panel CAL|COMP switch protects the calibration/compensation memory from accidental destruction.

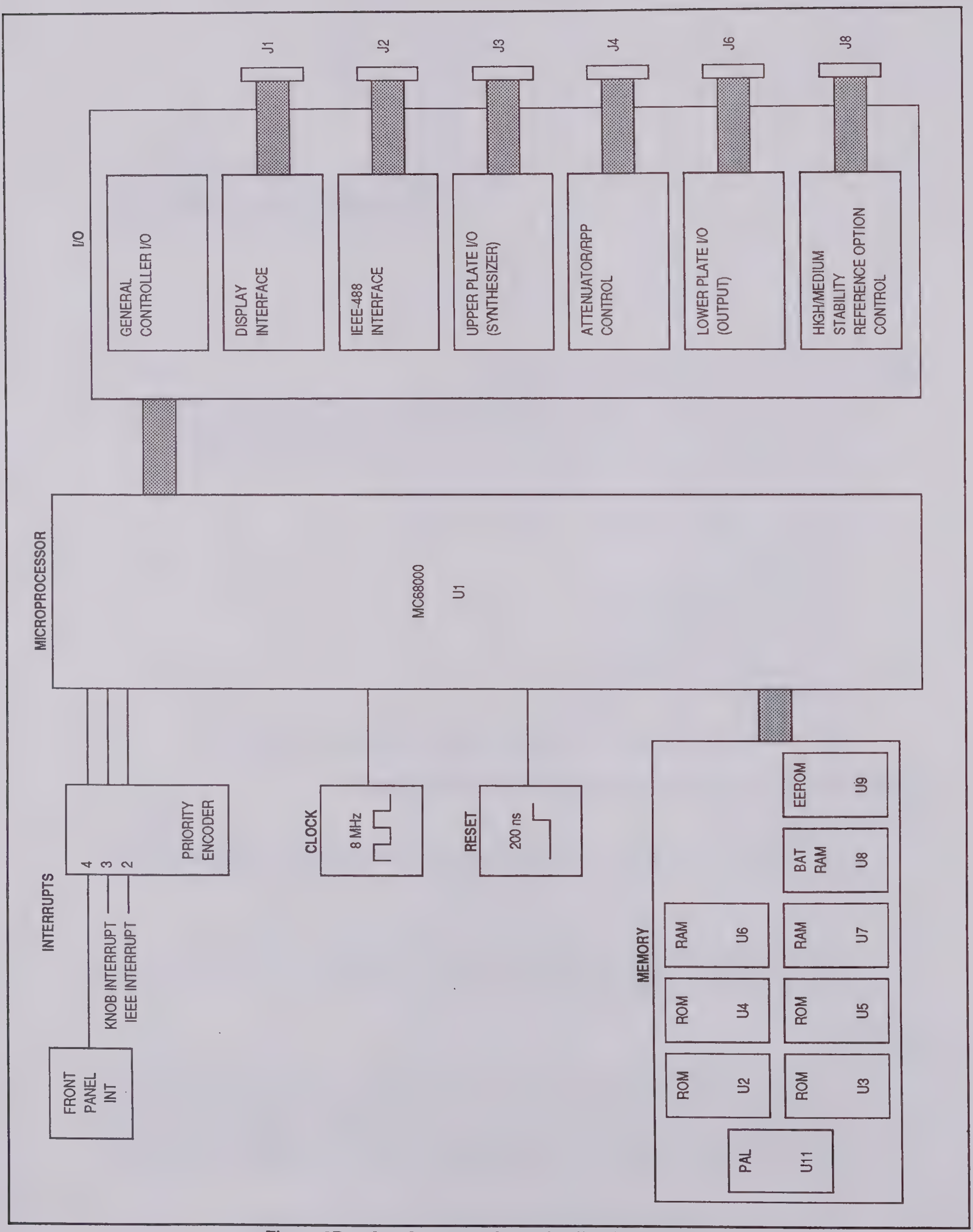

I/O
GENERAL CONTROLLER I/O
DISPLAY INTERFACE
J1
IEEE-488 INTERFACE
J2
UPPER PLATE I/O (SYNTHESIZER)
J3
ATTENUATOR/RPP CONTROL
J4
LOWER PLATE I/O (OUTPUT)
J6
HIGH/MEDIUM STABILITY REFERENCE OPTION CONTROL
J8
MICROPROCESSOR
MC68000
U1
INTERRUPTS
PRIORITY ENCODER
4
3
2
FRONT PANEL INT
KNOB INTERRUPT
IEEE INTERRUPT
CLOCK
8 MHz
RESET
200 ns
MEMORY
EEROM
U9
BAT RAM
U8
RAM
U7
RAM
U6
ROM
U5
ROM
U4
ROM
U3
ROM
U2
PAL
U11

Figure 6B-1. A13 Controller Assembly Block Diagram

Memory Control 6B-5.

Decoder PAL U11 decodes the memory selects and contains additional write-protection logic for calibration/compensation memory and the instrument states stored in the battery-backed RAM. Timing PAL U15 adds one wait state to each memory read or write cycle.

Individual upper-byte and lower-byte read and write enable signals are generated from 68HC000 control signals R/W, UDS, and LDS by U22. Signals RDU and RDL are read enables for the upper-byte and lower-byte respectively. Signals WRU and WRL are write enables for the upper-byte and lower-byte respectively.

Front Panel Interface 6B-6.

Data is transferred to and from the front panel circuitry through tri-state bidirectional data buffer U31. The corresponding address signals are transferred through tri-state buffer U32. These buffers are active when a front panel latch is addressed and the buffer control signal from U43 is low. Otherwise, the buffer is in the high-impedance state. To reduce RF emissions from the Signal Generator, low-pass filters and bypass capacitors are used on all data and select signals to the front panel.

The front panel interrupt rate is determined by the binary dividers U14 and U20. The system clock is divided by 8192 to generate a front panel interrupt every 540 microseconds.

IEEE-488 Interface 6B-7.

All IEEE-488 communications are handled by U28, an NEC μPD7210 talker/listener IC. The 7210 is connected directly to the system address and data bus and communicates with the microprocessor as a memory mapped I/O device.

The active low interrupt signal IEINTL is connected to the level two interrupt on the microprocessor. Tri-state bus drivers U29 and U30 interface the 7210 directly to the IEEE-488 bus.

Attenuator Control Interface 6B-8.

The attenuator control signals are latched by U39. Darlington driver U40 provides the level shifting necessary to control the A7 Relay Driver/RPP PCA.

Module I/O Interface 6B-9.

Control data is transferred to the RF circuitry through two byte-wide unidirectional data buses. Data is transferred to the upper module through J3 and to the lower module through J6.

Select lines BSEL0L, BSEL1L, and BSEL5L, and address lines SAB2, SAB1, and SAB0 are decoded into individual latch enables for the upper module on the A4 Subsynthesizer PCA. Tri-state buffers U24 and U33 provide drive current when active and allow these signals to float when inactive.

Select lines BSEL2L, BSEL3L, and BSEL4L and address lines BAB2, BAB1, and BAB0 are decoded into individual latch enables for the lower module on the A11 Modulation Control PCA. Tri-state buffers U25 and U27 provide drive current when active and allow these signals to float when inactive.

Timing PAL U15 adds additional wait states to each module I/O write cycle to ensure that adequate setup and hold times are provided for every IC on the bus.

Status and Control Latches 6B-10.

Input buffers U35, U36, U37, and U45 read the fault detector signals, hardware status signals, the option status signals, and the status of the REF INT/EXT and CAL|COMP switches. Control and buffer enable data is latched by output latches U34 and U38.

DIGITAL CONTROLLER TROUBLESHOOTING 6B-11.

A properly operating front panel indicates that most of the controller and display circuitry is functional. Therefore, the most obvious symptom of failure in the A13 Controller PCA is a blank front panel. If the front panel is totally blank or unresponsive to keystrokes, refer to Section 6A, Power Supply, and verify that all assemblies are receiving the correct voltages. If all voltages are correct, refer to "Microprocessor Kernel" further on in this section.

If the front panel is operating correctly but the RF output is incorrect, try to determine if the fault is on the controller or on an RF circuit board by programming various functions and checking for status codes.

If the symptoms indicate a digital or control failure, the following paragraphs may help isolate the fault to a particular functional circuit. Refer to the A13 Controller PCA schematic diagram in Section 10.

RF Control 6B-12.

Communication with the RF circuitry in the upper and lower modules is through connectors J3 and J6 respectively. The RF data and control signals to both modules are buffered by tri-state drivers that are active only while data is being transferred and are in the high-impedance state at all other times.

Special Function 903, the latch test, generates continuous activity on the data and address buses so that the activity can be monitored with an oscilloscope. The latch test is described under "Software Diagnostic Functions" in Section 6.

Enter Special Function 903 to initiate the latch test. Use an oscilloscope to inspect the chip select signals at the inputs and outputs of buffers U24 and U25. The first symptom to look for is inactive signals or invalid logic states. If there are no chip select signals present at the inputs of U23, refer to "Address Decoding" later in this section.

If all of the chip select signals are operating correctly, connect an oscilloscope probe to the signal BSEL0L and use the high-to-low transition of the signal to trigger the oscilloscope. Use another probe to inspect the data and address signals buffered by U24, U25, U27, and U33 during the low period of BSEL0L. Look for inactive signals and invalid logic states. Also compare the buffer inputs to their outputs. Press the STEP ▽ key, then the STEP △ key to toggle each of the data signals. In addition, make sure that the buffer control signals are low (active).

If the signals pass the above tests, check the data and address signals at any suspicious latch or dac on the suspect RF circuit board. If a dac problem is suspected, use special functions 941, 942, and 943 to set all dacs to zero, half scale, and full scale respectively.

Microprocessor Kernel 6B-13.

Microprocessor-related problems are difficult to troubleshoot because of the volume of activity at any given time. However, you can systematically verify independent circuit functions and isolate some of the most obvious problems. Read the following paragraphs and check the related circuitry.

Clock 6B-14.

Connect an oscilloscope probe to the clock oscillator output (TP4). There should be a symmetrical 8-MHz square wave with adequate logic levels. If the signal appears abnormal, check the input signal at U18 pin 3 to determine if there is a problem with the oscillator circuit or the ICs connected to the clock output. The square wave should be an inverted version of the same 8-MHz square wave on U18 pin 4 (it may be slightly distorted due to its loading).

Power-On Reset 6B-15.

Connect an oscilloscope probe to the RESET input, U1 pin 18. The signal should generate a low-to-high transition on power-up and remain high during normal operation. Turning the power off and on generates an active low reset pulse approximately 200 ms wide.

If the reset pulse to U1 appears abnormal, compare it to the reset output of the power supply monitor IC, U13 pin 5. If this reset pulse is abnormal, suspect problems with U13, and all ICs connected to the RESETL and RESETH signals.

Also check the HALT input, U1 pin 17; it should look like the RESET input on U1 pin 18.

Unused Microprocessor Inputs 6B-16.

Input signals to U1, BR (pin 13) and BGACK (pin 12) should both be high. If either of these signals is not high, correct the fault before continuing.

Bus Error 6B-17.

The bus error input BERR, U1 pin 22, notifies the microprocessor when a memory cycle cannot be completed as a result of a hardware fault. Normally, the BERR signal should always remain high.

If the BERR signal goes low, verify that U14 pin 1 is clocked by an 800-kHz signal with a 60/40 duty cycle. Also verify that U14 pin 2 is receiving continuous activity from the address strobe signal (AS).

Interrupts 6B-18.

The front panel edit knob interrupt is generated on the A1 Display PCA when the knob is turned. The interrupt signal from the Display PCA connects to U12 pin 13. If the signal is low when the knob is in the rest position, refer to “Edit Knob Interface” further on in this section.

Under normal operation, a front panel interrupt is generated every 540 μs at U21 pin 6. Verify that the divided outputs from U14 and U20 are correct and that a reset signal at U21 pin 1 is generated after each interrupt.

Verify that the IEEE-488 Interface interrupt signal, IEINTL (on pin 12 of U12) is in the inactive (high) state. If IEINTL is active, make sure the microprocessor kernel and buses are operating correctly, since the software must be operating before the IEEE interrupt can be initialized properly. If these are correct, troubleshoot communications with the IEEE-488 interface IC using the diagnostic tests under the heading "I/O Diagnostic Tests" further on in this section.

Microprocessor Bus 6B-19.

The dynamic nature of the microprocessor bus makes it difficult to verify the data transmitted at any given time. However, most common bus faults show recognizable symptoms and can be found with the aid of the address bus diagnostic test.

To initiate the bus diagnostic test, turn off the instrument power and set DIP switches 2, 3, and 4 of S1 to the ON position. Remove U11 from its socket to disable all memory and I/O chip selects, then turn the power on. This test generates predictable activity on the control signals and the address bus.

Look at the bus control signals (AS, R/W, UDS, LDS) with an oscilloscope. Suspect inactive signals or signals that enter invalid logic states. Also compare the inputs and outputs of gated signals.

All the address bus signals should have square waves of varying frequencies. The least significant signal (A1) has the highest frequency, and successively higher order signals have a frequency half that of the previous line. Note that there are small glitches on all of the address signals during the low cycle. These are normal and are not really glitches. The address lines are momentarily tri-stated between bus cycles, and the pull-up resistors pull the signals only part way of the up before the next bus cycle begins.

If the microprocessor bus test does not function as described, suspect the microprocessor kernel and the data bus. Check for data lines shorted together or shorted to the power supply. Also look for ICs that may be driving the data bus.

If the control and address signals appear normal, turn the power off and set the DIP switches to the OFF position and install U11.

Address Decoder 6B-20.

Several levels of address decoding are used to select the memory and I/O devices. Figure 6B-2 shows the levels of decoding.

Decoder PAL U11 generates the major memory segment selects. Verify that all of its address and control inputs are working properly. The signal CMWRL is the write-protection signal for the calibration/compensation memory. Signal CMWRL is connected directly to the rear panel CAL|COMP switch. Signals NVWR and COMPWR are software controlled write-protection signals for the nonvolatile memory and the calibration/compensation memory, respectively.

A chip select for the I/O circuitry is also generated by U11. Two additional levels of decoding generate the individual device selects. If U11 is operating correctly but the decoded chip select is not properly generated, proceed to the following diagnostic tests and perform whichever test is appropriate for the symptoms displayed.

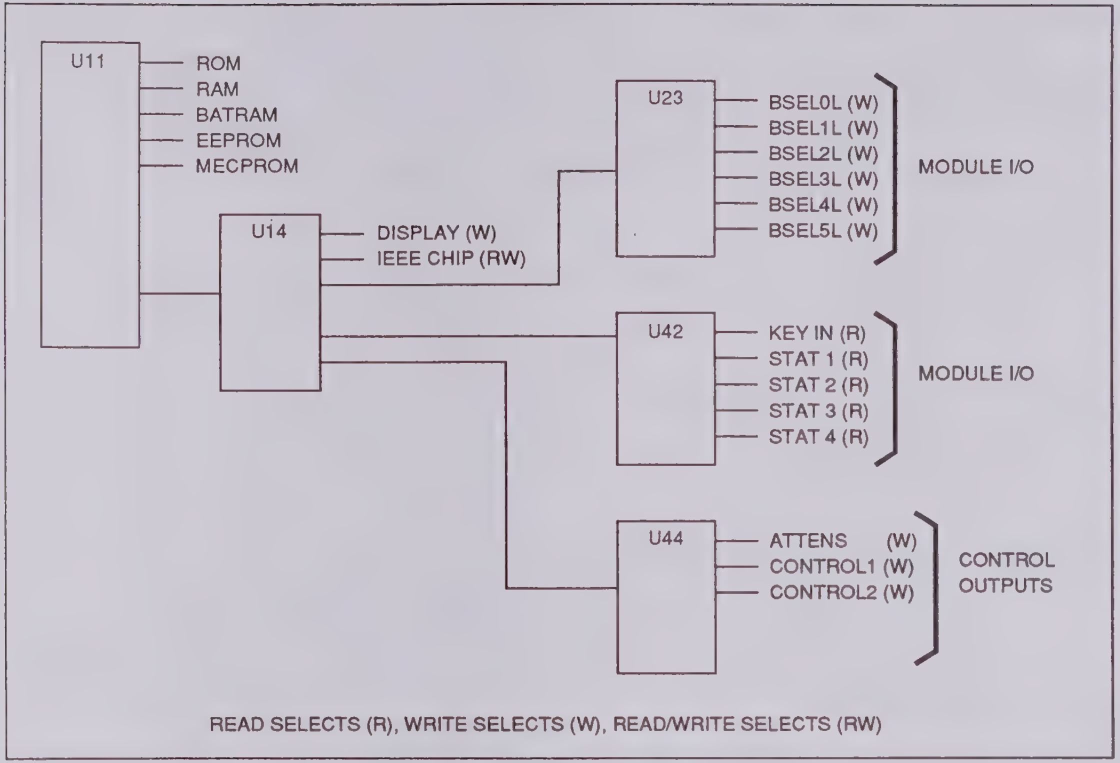

U11
ROM
RAM
BATRAM
EEPROM
MECPROM
U14
DISPLAY (W)
IEEE CHIP (RW)
U23
BSEL0L (W)
BSEL1L (W)
BSEL2L (W)
BSEL3L (W)
BSEL4L (W)
BSEL5L (W)
MODULE I/O
U42
KEY IN (R)
STAT 1 (R)
STAT 2 (R)
STAT 3 (R)
STAT 4 (R)
MODULE I/O
U44
ATTENS (W)
CONTROL1 (W)
CONTROL2 (W)
CONTROL OUTPUTS
READ SELECTS (R), WRITE SELECTS (W), READ/WRITE SELECTS (RW)

Figure 6B-2. Address Decoding

I/O Diagnostic Tests 6B-21.

Initiate a diagnostic routine that continuously writes the data byte 10101010 (binary) to each decoded I/O write location (labeled W or RW in Figure 6B-2). Momentarily ground TP1 on the controller if the data write-select lines to the display latches, the IEEE-488 talker/listener IC (U28), the module I/O control circuitry, or the control outputs are not generated properly. Momentarily grounding TP2 performs the same action but writes the data byte 01010101 (binary) instead.

If the data read selects to IEEE-488 talker/listener IC U28 or the status input buffers are not generated properly, momentarily ground TP3. This initiates a diagnostic routine that continuously reads data from each decoded read position (labeled R or RW in Figure 6B-2). Cycle the instrument power to terminate this diagnostic function.

These diagnostic tests write the data bytes very fast to more easily trigger an oscilloscope. Inspect the various I/O select signals and their relationship to the data and address signals. Normal software activity is halted so instrument power must be cycled to terminate the test.

The display should show an unusual combination of digits and segments since it is displaying an alternating bit pattern rather than the normal display data. Although the module I/O selects are generated by the tests, it may be easier to test the module I/O circuitry using the latch test once the microprocessor circuitry is fully functional.

CALIBRATION/COMPENSATION MEMORY 6B-22.

The integrity of the calibration/compensation data is vital to the performance of the instrument. The use of redundant data storage allows the system to recover even if some of the data has been corrupted.

There are 11 calibration/compensation data segments:

1. Attenuator
2. Coarse Loop Compensation
3. Coarse Loop Steering
4. Output
5. Subsynthesizer
6. Sum Loop Compensation
7. Sum Loop steering
8. AM Calibration
9. FM Calibration
10. RF Level Calibration
11. Reference Oscillator calibration.

Two copies of each data segment are maintained in two separate ICs on the Controller PCA. One copy is stored in EEPROM U9, and the other copy is stored in battery-backed RAM U8. If the power fails while either version is being updated, the other is still valid.

Calibration/Compensation Memory Status 6B-23.

Whenever the self-tests are performed, the checksums are verified for each data segment in EEPROM U9 and in battery-backed RAM U8. In addition, each checksum is compared to the corresponding checksum in the redundant data block. If one checksum is valid and the other is invalid, the valid copy is used. If both copies have invalid checksums, overrange/uncal status code 250 is set, and the STATUS annunciator flashes.

If any of the checksums fail, self-test status code 302 is reported. Special function 04 displays a list of codes that specify which checksums failed. The list can be scrolled by pressing the [STATUS] key. If all checksums are valid, the code 00 is displayed. Refer to Appendix E for a complete list of the checksum status codes.

The most likely failure mode would be a defective EEPROM or battery-backed RAM that would show failures of all the checksum error codes for that IC. Replace the defective IC, and refer to "Repairing Calibration/Compensation Memory Checksum Errors" later in this section.

In addition to checksum error codes, there are codes that indicate the checksums are valid, but a byte-by-byte comparison of the data segments reveals that they are different. This unusual condition is likely to occur only if one of the two calibration/compensation memory ICs have been swapped between controller boards. Although this situation rarely occurs, it is important to detect the condition so that corrective action can be taken. The data comparison codes are included with the checksum status codes in Appendix E.

Repairing Calibration/Compensation Memory Checksum Errors 6B-24.

Special Function 907 attempts to repair all invalid data segments reported by the calibration/compensation memory status command. Special Function 907 can be used to repair an error in an individual data segment or to initialize a new EEPROM or battery-backed RAM following the replacement of a defective part.

NOTE

The rear panel CAL|COMP switch must be set to the "1" position before performing Special Function 907.

If the checksums in both ICs are valid for a given data segment, no transfers are performed. However, if one checksum is valid and the other is invalid, the message "—Sto—" is displayed, and the good data is copied over the bad data. If both checksums are bad, no transfers can be performed. Each redundant data segment pair is checked and updated individually.

This also resolves the situation where a segment in EEPROM and in the battery-backed RAM both have valid checksums but contain different data. The EEPROM data segment is always copied to battery-backed RAM in this situation.

After all transfers are complete, the checksums are verified again and any remaining failures are reported.

Calibration/Compensation Memory Origin Status 6B-25.

Data in the calibration/compensation memory can be generated by:

- The Fluke factory
- The Module Exchange Center (MEC)
- You (by performing the calibration or compensation procedures)

The calibration/compensation data origin code specifies how the particular data segment was generated. A segment's data origin may have a bearing on future actions, so it is desirable to know how each was generated. Refer to Section 7, Compensation Procedures.

Special Function 05 displays the data origin codes. All data segments generated by the Fluke factory display origin code 00. Any data segments generated other ways display the corresponding status code. When there are more than four codes, scroll the list by pressing the STATUS key. Refer to Appendix F for a complete list of origin codes.

FRONT PANEL CIRCUIT DESCRIPTION 6B-26.

The front panel section, mounted in a sheet metal housing, consists of the A1 Display PCA, a switch circuit board, elastomeric switches, and the edit knob. The front panel section also includes the display lens, the AM INPUT connector, the FM/ϕM INPUT connector, and the PULSE INPUT connector.

All front panel control keys, except the POWER on/off button, consist of an elastomeric membrane sandwiched between the switch circuit board and the front panel sheet metal housing. The switch circuit board consists of an 8-by-8 matrix of open switch contact pads. When a key is pressed, a conductive pad on the back of the elastomeric membrane connects a set of contact pads. The software senses which row and column of the matrix is connected when a key is pressed. The two opto-interrupter ICs for the edit knob are the only active components mounted on the Switch PCA.

Display PCA 6B-27.

The A1 Display PCA provides a readout of the programmed modulation, frequency, amplitude parameters, and status information. (Refer to its schematic in Section 10.) Displayed information and the bright digit are controlled by the A13 Controller PCA under the direction of the instrument software. The display is made up of two vacuum-fluorescent displays and their associated control circuitry. The two displays are refreshed as four groups of nine display fields (usually a digit) each. The four groups share the digit (grid) strobes but have individual segment (anode) strobes.

Data Communications 6B-28.

Display data is sent through a byte-wide bidirectional data bus from the Controller PCA and is latched by U1 through U5, and U19. The front panel latch select signals DIG1L, DIG2L, SEG1L, SEG2L, SEG3L, and SEG9L, which are then decoded by U20. These latch select signals determine which latch receives the data. Level-shifting buffer drivers U6 through U10 interface the latches directly to the +37V grids and anodes of the vacuum-fluorescent displays.

Display Filament Voltage 6B-29.

The 6.0V ac filament voltage for the display is derived from a center-tapped winding on the Power Supply PCA transformer (T1). The ac filament voltage is biased at +6.2V above ground by circuitry on the A14 Power Supply PCA to provide a cutoff potential for the displays.

Bright-Digit Effect 6B-30.

The bright-digit effect is achieved by providing three extra refresh cycles (strobes) to the specified digit. Grid current-limiting resistor R3 ensures uniform digit brightness by controlling electron depletion from the display cathode filaments.

Switchboard Interface 6B-31.

The digit strobe data latched by U1 is buffered by open-drain inverters U13 and U15 and strobes the front panel switch matrix. The switch columns are strobed in unison with the display fields. The switch matrix status is read by tri-state buffer U14.

Remote Footswitch (AUX Connector) 6B-32.

The inputs of the rear panel AUX connector accept remotely generated sequence up, sequence down, and bright-digit field (frequency or amplitude) commands. The requests are generated by momentarily grounding the desired signal. The pinout of this connector is provided in Appendix I.

The rear panel control inputs are static due to electromagnetic emission considerations. Gates in U12, U13, U15, and U16 convert the static rear panel inputs into strobed key requests. The software services these key requests in the same manner as the other strobed keys.

Edit Knob Interface 6B-33.

The edit knob interface circuitry receives two input signals (WINDOWL and TRIGGERL) from the opto-interrupters on the A19 Switch PCA.

If the trigger signal makes a high-to-low transition while the window signal is low, the software generates an edit-up request. The software transmits this information to the Controller PCA by setting the knob interrupt signal KNOBINTL low and the knob direction signal KNOBUP high.

If the trigger signal makes a low-to-high transition while the window signal is low, the software generates an edit-down request. The software transmits this information to the Controller PCA by setting the knob interrupt signal KNOBINTL low and the knob direction signal KNOBUP low.

The trigger signal is ignored when the window signal is high.

After servicing the interrupt and reading the directional information, the controller resets the knob circuitry by toggling the reset signal KNOBRSTL.

Display Blanking 6B-34.

Monostable U11 and NOR gate U12 clear the display when new field or segment strobes are not received. This protects the display if the microprocessor stops refreshing.

Operate/Standby Selection 6B-35.

The front panel POWER switch selects the operate or standby modes. The switch is closed in the standby position, which sets the STANDBY signal high and illuminates LED CR1. The switch is open in the operate position, which pulls the STANDBY signal low, and turns off LED CR1.

FRONT PANEL TROUBLESHOOTING 6B-36.

If the display shows signs of activity but has missing or bright digits or segments, the problem is most likely one of the data latches or drivers on the A1 Display PCA. If the display is blank and the controller is operational, check the power supplies (refer to Section 6A, Power Supply).

Use the I/O diagnostic tests described in the A13 Controller troubleshooting text to continuously write data to the display latches. Verify that the correct data is written to each latch and is present at the outputs of the display drivers. The display blanking output of U11 pin 13 should remain high while the data is written.

As the edit knob is rotated, the window and trigger signals should generate transitions on the input signals to U18 resulting in an interrupt at U12 pin 12. If the signals do not change as the knob is turned, suspect the opto-interrupters on the A19 switch PCA or the interconnection with the Switch PCA.

Two special-function service tests are available to test the front panel indicators and keys. Special function 901 checks the front panel displays by lighting all segments. Exit the test by pressing any key.

Special function 902 initiates the key check. As each key is pressed, its identifier code is displayed in the center of the FREQUENCY display field. The key identifier codes are assigned in order from top to bottom and from left to right. This test is exited by a clear entry.

Section 6C
Frequency Synthesis

FREQUENCY FAULT TREE 6C-1.

Refer to Figure 6C-1, Frequency Synthesis Fault Tree, when troubleshooting frequency-related problems.

SUBSYNTHESIZER BLOCK DIAGRAM 6C-2.

The Subsynthesizer Block Diagram (Figure 6C-2) identifies the major functional blocks and signal paths of the Subsynthesizer.

A4 SUBSYNTHESIZER CIRCUIT DESCRIPTION 6C-3.

The A4 Subsynthesizer PCA, in conjunction with the A3 Subsynthesizer VCO PCA generates a 16- to 32-MHz signal in 2-Hz steps. The Subsynthesizer PCA also distributes power, control lines, and programmable dc voltages to the A2 Coarse Loop PCA. Status lines from the Coarse Loop PCA to the A13 Controller PCA are also routed through the Subsynthesizer PCA.

The Subsynthesizer phase-locked loop (PLL) is a fractional divider PLL with a single-sideband (SSB) mixer in the feedback path. The PLL oscillator is located on the A3 Subsynthesizer VCO PCA and operates at a frequency of 160 to 320 MHz. A 10/1 divider on the VCO PCA produces the 16- to 32-MHz signal.

The key signals to the PLL are the 1-MHz reference signal from the 40 MHz reference circuit, the 160- to 320-MHz signal from the vco, and the 10- to 20-kHz signal from the low order digit generator circuit. The fractional division technique provides provides 10 kHz frequency resolution at the vco frequency (160 to 320 MHz).

Single-Sideband Mixer 6C-4.

The SSB mixer, in conjunction with the low order digit generator provides an additional 20-Hz resolution at the vco frequency.

The vco frequency of 160 to 320 MHz is input to J7 (refer to the A4 Subsynthesizer PCA schematic in Section 9) and filtered by C140 through C142, and L70 and L71. Then it is attenuated by R69 through R71 and amplified by U50. Resistors R101 through R103 attenuate the signal again and send it to be amplified by U51. At this point the signal is connected to U52, a quadrature (90-degree phase difference) 3-dB coupler.

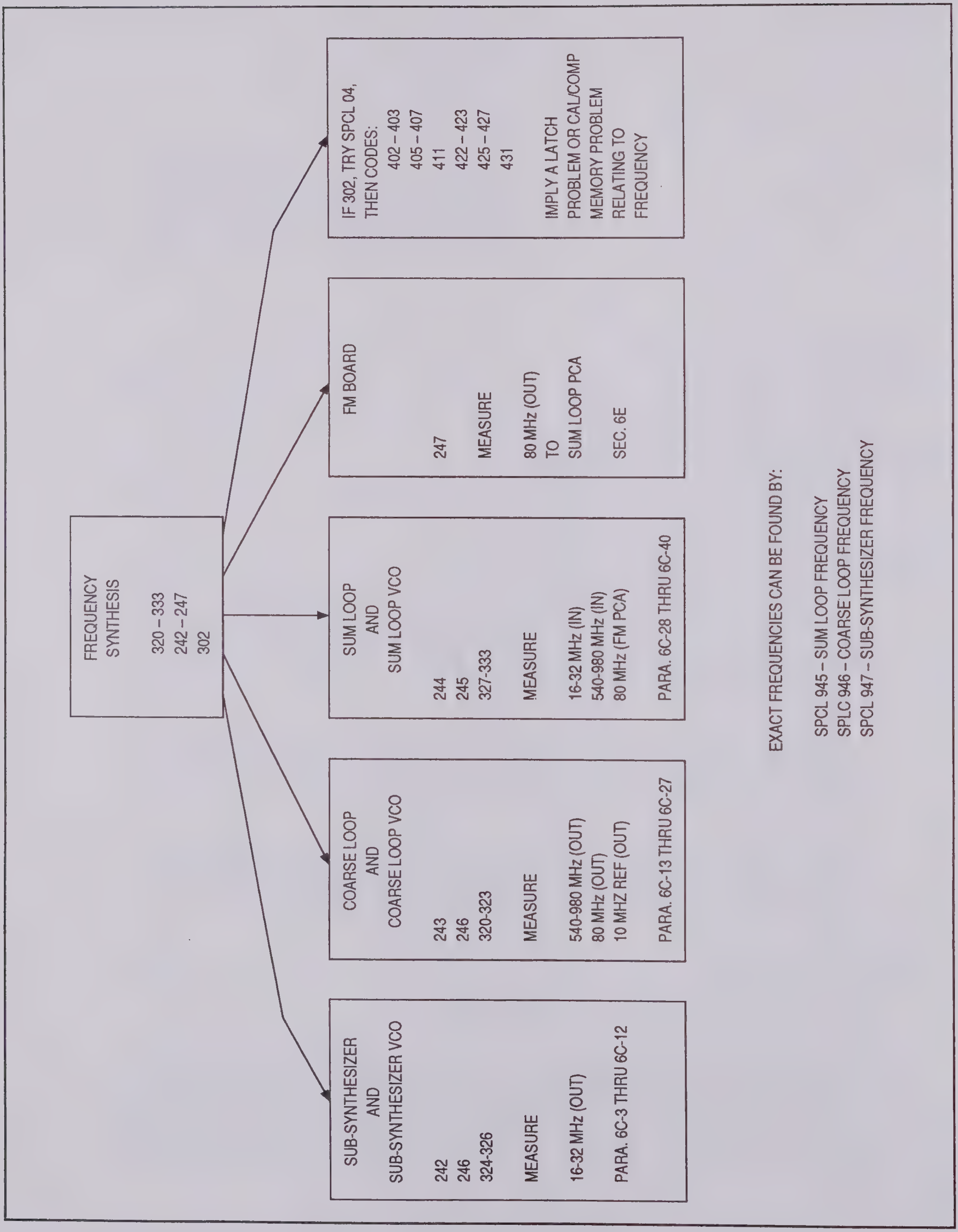

FREQUENCY SYNTHESIS
320 – 333
242 – 247
302
SUB-SYNTHESIZER AND SUB-SYNTHESIZER VCO
242
246
324-326
MEASURE
16-32 MHz (OUT)
PARA. 6C-3 THRU 6C-12
COARSE LOOP AND COARSE LOOP VCO
243
246
320-323
MEASURE
540-980 MHz (OUT)
80 MHz (OUT)
10 MHZ REF (OUT)
PARA. 6C-13 THRU 6C-27
SUM LOOP AND SUM LOOP VCO
244
245
327-333
MEASURE
16-32 MHz (IN)
540-980 MHz (IN)
80 MHz (FM PCA)
PARA. 6C-28 THRU 6C-40
FM BOARD
247
MEASURE
80 MHz (OUT) TO SUM LOOP PCA
SEC. 6E
IF 302, TRY SPCL 04, THEN CODES:
402 – 403
405 – 407
411
422 – 423
425 – 427
431
IMPLY A LATCH PROBLEM OR CAL/COMP MEMORY PROBLEM RELATING TO FREQUENCY
EXACT FREQUENCIES CAN BE FOUND BY:
SPCL 945 – SUM LOOP FREQUENCY
SPLC 946 – COARSE LOOP FREQUENCY
SPCL 947 – SUB-SYNTHESIZER FREQUENCY

Figure 6C-1. Frequency Synthesis Fault Tree

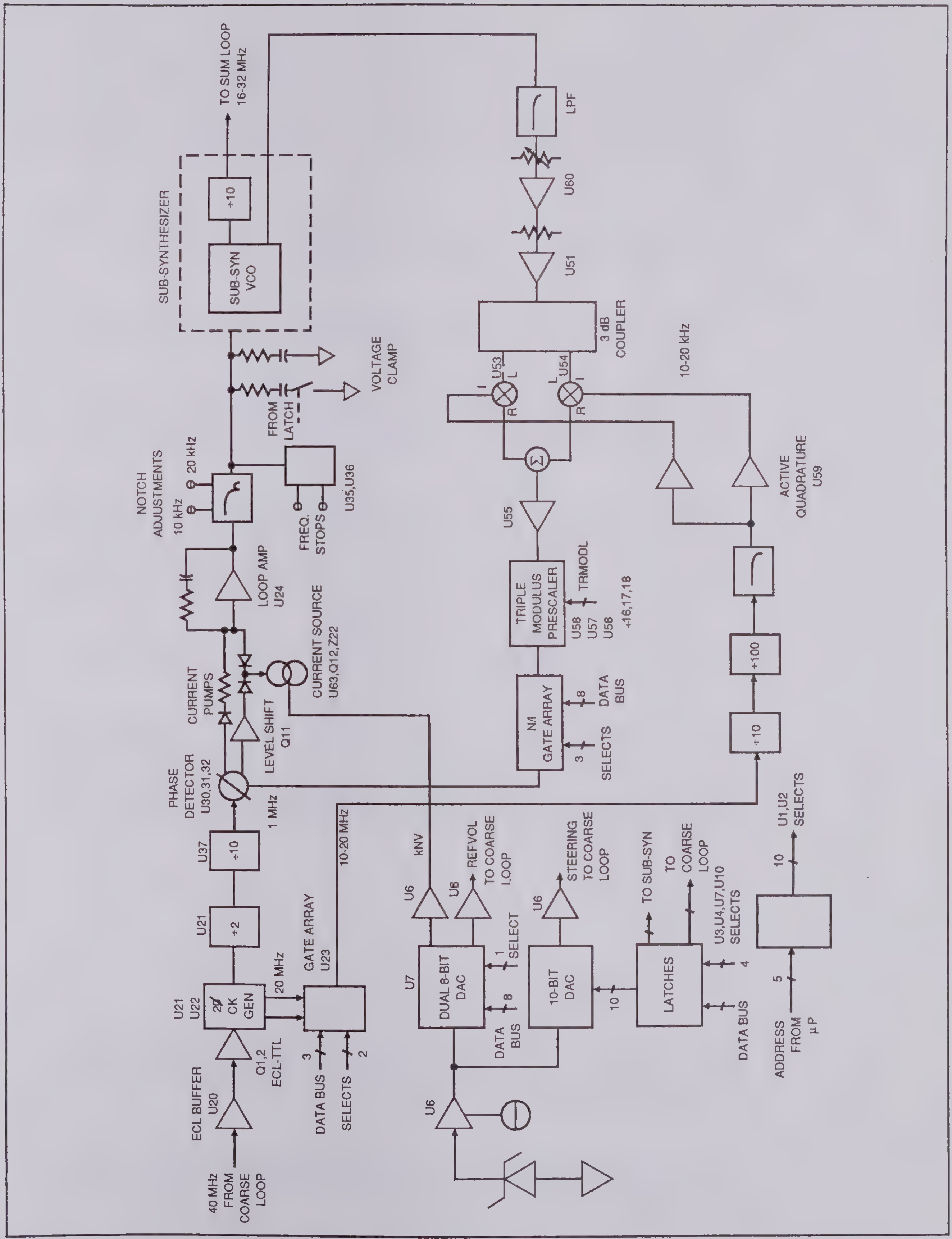

40 MHz FROM COARSE LOOP
ECL BUFFER U20
Q1,2 ECL-TTL
U21 U22
2X CK GEN
20 MHz
GATE ARRAY U23
3
DATA BUS
2
SELECTS
U21
÷2
U37
÷10
1 MHz
PHASE DETECTOR U30,31,32
LEVEL SHIFT Q11
CURRENT PUMPS
CURRENT SOURCE U63,Q12,Z22
LOOP AMP U24
NOTCH ADJUSTMENTS
10 kHz
20 kHz
FREQ. STOPS
U35,U36
FROM LATCH
VOLTAGE CLAMP
SUB-SYNTHESIZER
SUB-SYN VCO
÷10
TO SUM LOOP 16-32 MHz
LPF
U60
U51
3 dB COUPLER
U53
U54
I
L
R
10-20 kHz
Σ
U55
TRIPLE MODULUS PRESCALER
TRMODL
U58
U57
U56
÷16,17,18
N/I GATE ARRAY
8
DATA BUS
3
SELECTS
ACTIVE QUADRATURE U59
÷100
÷10
10-20 MHz
kNV
U6
U8
REFVOL TO COARSE LOOP
U7
DUAL 8-BIT DAC
1
SELECT
8
DATA BUS
U6
STEERING TO COARSE LOOP
10-BIT DAC
10
LATCHES
TO SUB-SYN
TO COARSE LOOP
U3,U4,U7,U10 SELECTS
4
DATA BUS
U1,U2 SELECTS
10
5
ADDRESS FROM μP
U6

Figure 6C-2. Subsynthesizer Block Diagram

The output of U52 and two other audio quadrature signals from U59 are summed in the doubly-balanced mixers U53 and U54 to produce two double-sideband suppressed-carrier signals. Summing the two composite signals in the resistor network R75 and R76 suppresses the upper-sideband component because of the phase relationship of the outputs of the mixers. The predominant remaining signal is the lower-sideband signal.

The lower-sideband signal, spanning 160 to 320 MHz in 10 kHz steps, is amplified by U55 and applied to the N-divider where it is divided to 1 MHz.

N-Divider 6C-5.

The main components of the N-Divider are: triple-modulus prescaler (divide by 16/17/18) U56, U57, and U58, and the N-Divider Custom Gate Array U62.

The triple-modulus prescaler (see Figure 6C-3), consists of divide-by-8/9 U58, divide-by-2 U57A, synchronizing flip-flop U57B, and quad NOR gates U56. If the inputs to U58, E1 through E5 (the 8/9 divider) are low, the prescaler divides by 9, and the total division to the output at pin 7 is 18.

If inputs E1 and E3 are low, the modulus of the 8/9 divider is controlled by the output of the divide-by-2 U57A. Consequently, the prescaler divides by 8 half the time and by 9 the other half, resulting in a divide by 17. U57B synchronizes the changing of the modulus with the clocking of the subsequent stages. The composite prescaler output U18A clocks the N-divider gate array via the ECL-to-TTL converter contained in U58.

The N-divider gate array (Figure 6C-4) contains two 5-bit binary counters (A and N), a BCD two-decade rate multiplier, and latches to interface to the controller. The following paragraphs describe the operation of the A and N counters.

At the beginning of a count cycle, a number is loaded into the A and N counters. The A counter is not at its terminal count, so the output is high, and the mode line (MODE L) is low. This causes the prescaler to divide by 17 (or 18, TRMODL=low). The mode line stays low for 31-A counts, where A is the programmed number. The mode line goes high, and the prescaler divides by 16 (or 17, TRMODL=low) for 31-N counts.

The total division is:

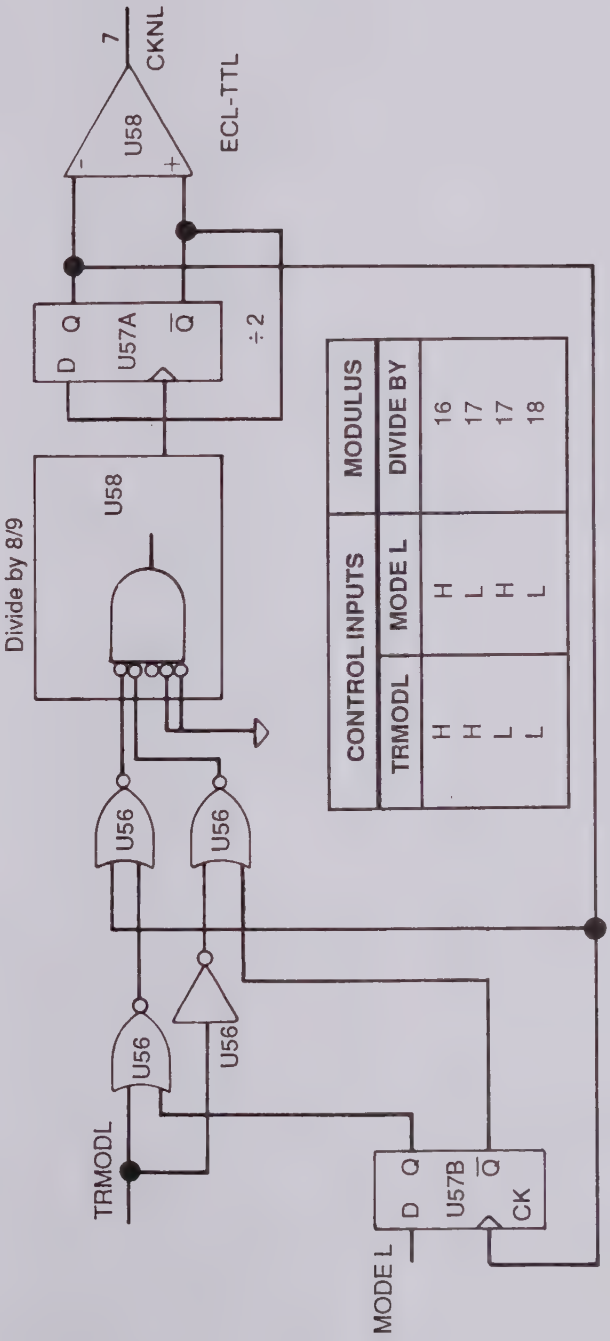
$$(P+1)(31-N) + P*((31-N)-(31-A))$$

or

$$P*(31-N) + (31-A).$$

On the 31st count, the counters are reinitialized. Figure 6C-5 shows the timing of the A counter programmed to 26 and the N counter programmed to 18, a total division of 213. Only the CKNL and MODEL signals shown in Figure 6C-4 are accessible at U62 pins 6 and 22, respectively.

The N-divider gate array includes a two-decade rate multiplier that produces the fractional part of the division. The N-divider gate array rate multiplier produces a pulse train with a programmed number of pulses for a 100-cycle frame of the 1-MHz N-divider output.


7
CKNL
U58
-
+
ECL-TTL
D
Q
U57A
$\overline{Q}$
÷ 2
Divide by 8/9
U58
U56
U56
U56
U56
TRMODL
MODE L
D
Q
U57B
$\overline{Q}$
CK

CONTROL INPUTS		MODULUS
TRMODL	MODE L	DIVIDE BY
H	H	16
H	L	17
L	H	17
L	L	18

Figure 6C-3. Triple-Modulus Prescaler

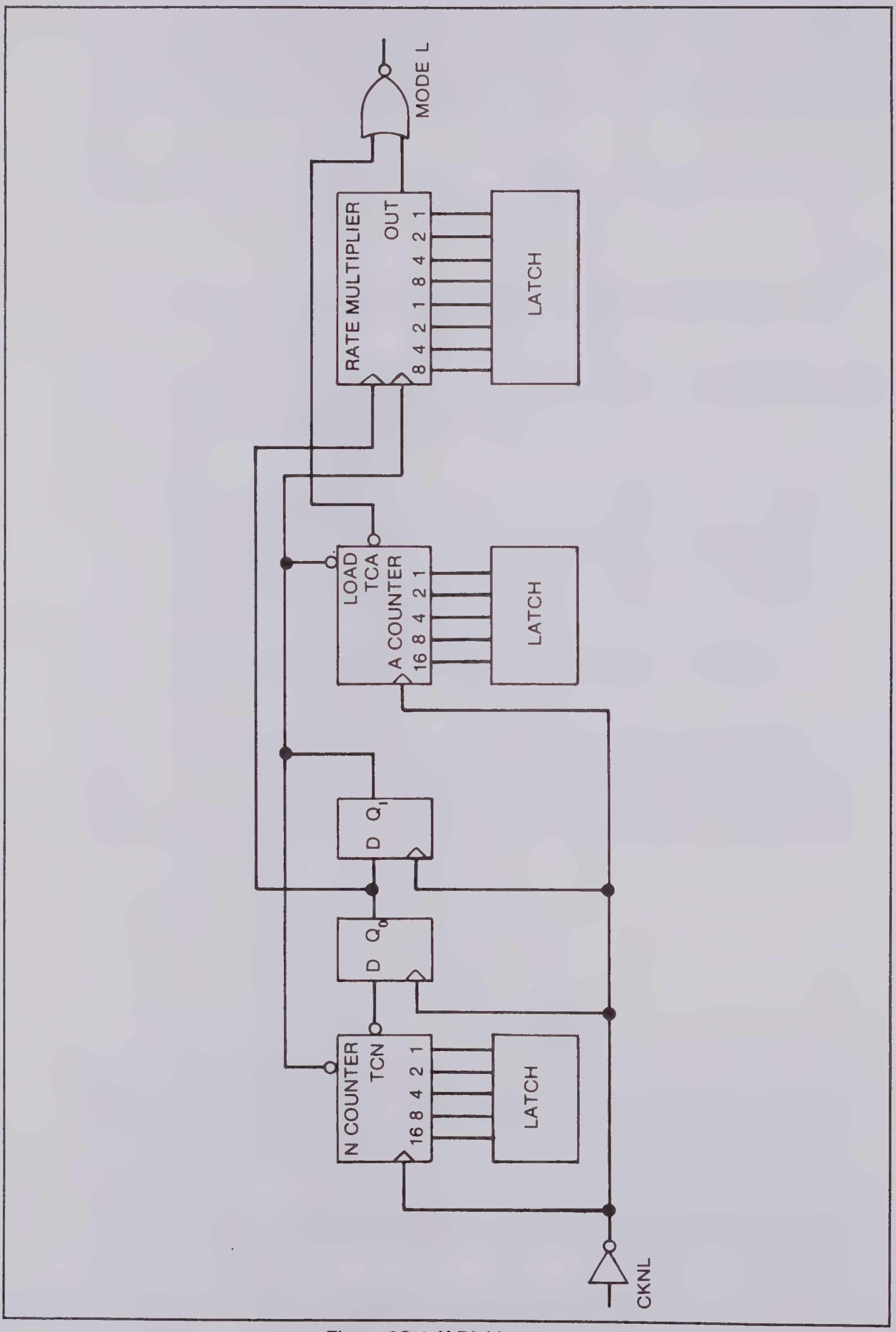

MODE L
RATE MULTIPLIER
OUT
8 4 2 1 8 4 2 1
LATCH
LOAD
TCA
A COUNTER
16 8 4 2 1
LATCH
D
Q_1
D
Q_0
N COUNTER
TCN
16 8 4 2 1
LATCH
CKNL

Figure 6C-4. N-Divider

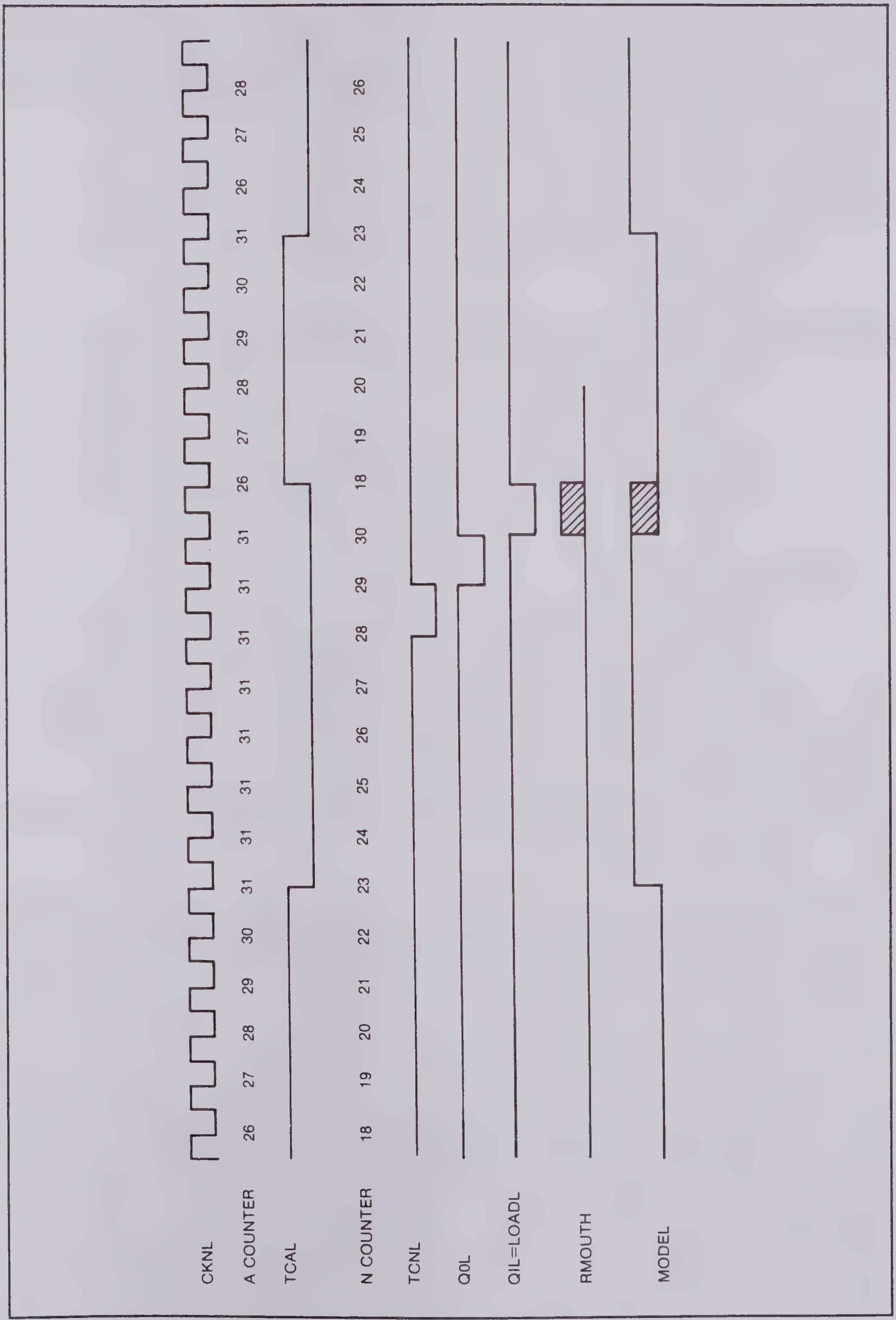

CKNL
A COUNTER
26 27 28 29 30 31 31 31 31 31 31 31 31 26 27 28 29 30 31 26 27 28
TCAL
N COUNTER
18 19 20 21 22 23 24 25 26 27 28 29 30 18 19 20 21 22 23 24 25 26
TCNL
Q0L
QIL=LOADL
RMOUTH
MODEL

Figure 6C-5. N-Divider Timing Diagram

The programmed number ranges between zero and 99, corresponding to 10-kHz steps at the vco frequency. The flip-flops in the rate multiplier are set up on count 29, and on count 30 a pulse may or may not be present, depending on the programming of the rate multiplier. This is represented by the shaded pulse in the timing diagram (Figure 6C-5).

Irregularly spaced rate-multiplier pulses cause the mode line to go low, and the prescaler divides by P+1 at a rate equal to the rate multiplier programming.

A 16/17 dual-modulus prescaler will not allow division from 160 to 320 without holes. For example, 170 is ten frames of 17. Consequently, there is no place to slip in the rate-multiplier pulses. It is not possible to divide by 171.

By using a triple-modulus prescaler, these problems are solved. Continuing with the previous example, 170 is 10 frames of 17 and 0 frames of 18. The deleter allows the prescaler to divide by 18 at a rate equal to the rate-multiplier frequency. Number 171 is 9 frames of 17 and 1 frame of 18. A software algorithm determines whether to operate in the 16/17 mode (TRMODL=1) or 17/18 mode (TRMODL=0).

The frequency at the output of the N-divider gate array is (Fo - Fs - Fd)/N. Since this must be equal to reference frequency, Fr, and Fr is 1 MHz, the vco frequency is Fo = N + Fs + Fd, where Fs is the SSB audio frequency from the low-order digit generator, and Fd is the fractional-division frequency.

Phase Detector 6C-6.

The 1-MHz reference signal from divide-by-10 U37, and the 1-MHz signal from the N-divider U62 are connected to a digital phase-frequency detector made up of U30, U31, and U32. If the N-divider output frequency is less than the reference frequency, TP25 is low, and the voltage at the output of level shifter, Q17, is below ground. CR18 turns off and allows current from U63 to flow through CR18 out of the integrator. This raises the voltage at the output of the integrator, which raises the vco frequency.

Similarly, when the frequency of the N-divider output is higher than the 1-MHz reference, TP24 is high turning on CR16 and allowing current to flow through R97 into the integrator. This lowers the voltage at the output of the integrator, which lowers the vco frequency.

If the phase between the reference and N-divider output slips more than two cycles in either direction, the corresponding phase-detector output is either high or low. This provides twice the integrator current during acquisition as a conventional phase-frequency detector.

R51 provides a small bias current to the integrator to bias the phase detector in the linear region: consequently, the up-pump is always on.

During calibration of the vco, the vco gain coefficient (Kv) is measured at many frequencies across the band, and non-volatile memory stores the compensation data. The instrument software uses this data along with N to control the PLL bandwidth. The PLL bandwidth is controlled by changing the current to the up-pump via KN dac (U7A, U6A), and voltage-to-current converter U62 and Q12.

Loop Amplifier 6C-7.

The loop amplifier-integrator consists of op amp U34, C98, and R44. Capacitors C97 and C102 filter the 1 MHz reference. The output of the integrator is connected to a multi-pole LC filter (R45, C104, C105, C106, C107, L56, L57, and R48) that attenuates the delete rate (10 and 20 kHz), and reference 1 MHz spurs.

Diodes CR12, CR13, CR14, CR15, CR22 and CR23 speed up the loop during switching. Additional lead/lag compensation is provided by C114, C115, R58, and R59. The second lead/lag network is switched by Q10 when the vco frequency is above 230 MHz. This compensates for the wide Kv range of the vco.

Amplifier U35 is a precision clamp that keeps the vco frequency within a specified range. Photoisolator U36 detects clamp activity, which indicates an out-of-lock condition. This signal is sent to the A13 Controller as the SUBUNLKL status.

Low-Order Digits Generator 6C-8.

The low-order digits generator consists of the clock generator (U21, U22, Q1, Q2), gate array U23, the divide-by-1000 (U60, U61), low-pass filter L75, and L76, and active quadrature generator U59. Internal to U23 is a 3 ½ decade-rate multiplier, associated latches, and a divide-by-2.

The 40-MHz reference from the A2 Coarse Loop PCA is converted to ECL in U20 and then converted to TTL in Q1 and Q2. This is followed by a 20-MHz two-phase clock generator U21, U22.

The input frequency to the rate multiplier is 20 MHz. The output frequency can be programmed from zero to 19.995 MHz in 5-kHz steps. This signal is ORd with the other phase of the 20-MHz clock to produce 20 to 39.995 MHz at U23 pin 1. The signal is also divided by 2 in U23, by 10 in U60, and again by 100 in U61 to produce 10 to 19.99975 kHz in 2.5-Hz steps (though not all of this resolution is used.) The TTL signal at TP30 is filtered by L75, L76, C156, C157, C158, C159, and C160. Op amp U59 forms an active quadrature generator to offset the signal at output pins 7 and 14 by 90 degrees. These two signals are the 10- to 20-kHz inputs for the PLL single-sideband mixer.

Dac's and Latches 6C-9.

The control bits for the A2 Coarse Loop PCA are latched by U3, part of U9 and U10. DAC U5 with op amp U6D provides the steering voltage for the A5 Coarse Loop VCO and dac U7B with op amp U6B provides the voltage to tune the reference TXCO.

SUBSYNTHESIZER TROUBLESHOOTING 6C-10.

NOTE

All frequencies mentioned are synthesized; they are exact (coherent with the 10-MHz reference), unless noted as approximate.

Status code 242 indicates that the A4 Subsynthesizer and/or the A3 Subsynthesizer VCO are/is not functioning properly. This status code is triggered when the Subsynthesizer VCO control voltage is out of the normal operating range. Status code 244 indicates the Sum Loop is out of lock, or that a problem exists with the Subsynthesizer and/or Subsynthesizer VCO.

Status code 244, appearing without status code 242, might indicate a marginal break-up condition. To check the Subsynthesizer across the band, move the jumper on the A3 Subsynthesizer VCO from TP1-TP2 to TP1-TP3. This allows the undivided Subsynthesizer VCO frequency to appear at A3-J2.

Connect the A3-J2 output to a spectrum analyzer and program the Signal Generator to 800 MHz. Verify that a stable 160 MHz signal displays on the spectrum analyzer. Step the Signal Generator in 200-kHz steps, while stepping the spectrum analyzer in 4-MHz steps. At each point, verify that the spectrum analyzer dislays a stable signal. If the signal shows evidence of breaking up, troubleshoot the Subsynthesizer and/or Subsynthesizer VCO.

If status code 242 appears, the vco control voltage may be stuck high or low. Measure the dc voltage at TP27 (it is not necessary to remove the module cover), if the dc voltage is around 1.5V, the circuitry that supplies the 1-MHz reference or the phase detector circuit is at fault. If the voltage is around 23V, check the circuitry associated with the phase-locked loop (vco, SSB mixer, and divider).

Table 6C-1 provides signal characteristics as seen at the various test points on the A4 Subsynthesizer PCA. The table lists the range of each signal and the expected value for a typical instrument state. The values in the TYPICAL column apply when the Signal Generator is programmed to 804.001499 MHz. To make the undivided Subsynthesizer VCO signal available for this troubleshooting procedure, move the jumper from TP1-TP2 to TP1-TP3 on the A3 Subsynthesizer VCO.

If the voltage at TP27 is approximately 1.5V, check TP22 for a 1-MHz TTL square wave. If the square-wave signal is missing or the frequency is incorrect, troubleshoot the circuitry previous to TP22. If the frequency is correct, check the phase detector (U30-U32) or loop amplifier (U34 and associated circuitry).

Check for a 10-MHz TTL square wave at U21 pin 9. The input at U21 pin 1, should be a 20-MHz TTL square wave. At U21 pin 3 there should be a 40-MHz TTL signal. There should be a 40-MHz ECL signal at both U20 pins 2 and 14. The A2 Coarse Loop input at J6, the frequency input, should be about 600-mV, p-p at 40-MHz.

If the Subsynthesizer VCO control voltage at TP27 is about 23V, remove the jumper shorting TP40-TP41 and connect a variable power supply to TP41 (be careful not to short to TP40, which could destroy U34). This opens the loop and allows the power supply to directly control the frequency of the Subsynthesizer VCO. Use a spectrum analyzer or counter connected to the undivided Subsynthesizer VCO output (A3-J3) to monitor the frequency. Adjust the power supply so that the frequency tunes from approximately 160 to 320 MHz. If the frequency cannot be adjusted, troubleshoot the A3 Subsynthesizer VCO. Set the frequency to approximately 240 MHz with the variable power supply.

Using a spectrum analyzer, low-impedance probe, and 10X attenuator, measure the level at the output of U51 (a good place to measure this is at the input to coupler U52). Ground the low impedance probe as closely as possible; PCA hold-down screws and the walls of the plate provide good grounds. The measured level should be approximately -10 dBm. If this level is not correct, troubleshoot the RF section (U50, U51, and associated circuitry).

Table 6C-1. Subsynthesizer PCA Test Points

Typical: Front panel frequency set to 804.001499 MHz
Range: Total Subsynthesizer frequency range (160-320 MHz)
Front panel from 800.000000 to 807.999999 MHz

TEST POINT	SIGNAL TYPE	RANGE	TYPICAL	FUNCTION
TP2	Ground			
TP3	TTL	20 MHz, 12.5 ns (AH)	Constant	2-phase clock generator
TP4	TTL	20 MHz, 12.5 ns (AH)	Constant	2-phase clock generator
TP5	TTL	10 to 19.98 MHz	19.98 MHz	Low order digit gate array output
TP6	DC	0 to 10.23V	2.2V	Coarse Loop VCO steering dac output
TP21	TTL	1 MHz, 50 ns (AL)	1 MHz	N-Divider output
TP22	TTL	1 MHz square wave	1 MHz	Reference divider output
TP23	Ground			
TP24	TTL	1 MHz, 10 ns (AH)	1 MHz	Phase detector down output
TP25	TTL	1 MHz, 150 ns (AH)	1 MHz	Phase detector up output high ~2.8V, low ~-0.5V
TP26	Ground			
TP27	DC	2 to 24V	8.6V	Subsynthesizer VCO control voltage
TP30	TTL	10 to 19.98 kHz	19.98 kHz	Low order digits signal
TP31	TTL	1 to 1.998 MHz	1.998 MHz	Intermediate low order digits signal (divide-by-10)
TP32	Ground			
TP33	TTL	9 to 19 MHz	15 MHz	Triple modulus pre-scaler output
TP34	TTL	0 to 1 MHz	10 kHz	Modulus select signal 50 ns (AL)
TP35	DC	0 to 10.23V	1.6V	Subsynthesizer loop gain compensation dac (KN) output
TP36	Input			For calibration of low-pass filter
TP37	Audio	10 to 19.98 kHz 450 mV p-p	19.98 kHz	Active quadrature generator output
TP38	Audio	10 to 19.98 kHz 450 mV p-p	19.98 kHz	Active quadrature generator output
TP39	DC	0 to 10.23V	Varies	Reference oscillator voltage dac output
TP40	DC	2 to 24V	8.6V	Loop amplifier output
TP41	DC	2 to 24V	8.6V	Low-pass filter input TP40-TP41 normally connected together, except when troubleshooting

Next, check the signal at the input to the divider U58 at pin 15 with the low impedance probe. Verify a -15 dBm lower sideband signal as measured on the spectrum analyzer. A problem at this point indicates a failure in the low order digits generator (U21, U22, U23, U60, and U61), active quadrature generator U59, SSB mixer U53, and U54, or divider input amplifier U55.

Program the Signal Generator to 804.000500 MHz. Verify the TTL signal at the output of the triple modulus prescaler, TP33, is approximately 15 MHz. The signal at the output of the N-divider gate array, TP34, should be approximately 1 MHz. This frequency should change as the 1-MHz digit is programmed, since the divide ratio is changing.

To troubleshoot the low-order digit generator, check the signal at TP3 and TP4 for a 25% duty cycle, active high 20-MHz TTL signal. Program the Signal Generator to 800.000000 MHz. The signal at TP5 should be 10-MHz TTL. As you program the unit under test (UUT) to 1 Hz, 10 Hz, and 100 Hz digits, the frequency at TP5 should change by 20 kHz, 200 kHz, and 2 MHz, respectively.

When the UUT is programmed to 800.000499 MHz, the frequency at TP5 should be 19.98 MHz. The outputs of the two divide-by-10, U60 and U61, should be 1.998 MHz and 19.98 kHz, respectively. The output of active quadrature generator U59 at TP37 and TP38 should be about 450 mV p-p, 19.98-kHz sine waves.

Tune the power supply and monitor the frequency at TP21; if the frequency is less than 240 MHz, the frequency at TP21 should be less than 1 MHz. There should be a TTL signal at TP24 that is predominantly low with very narrow pulses going high. There should be a similar signal at TP25, except the "low" voltage is approximately -0.5V and the "high" voltage is +2.8V. The voltage at TP40 should be about 28V.

If the frequency is greater than 240 MHz, the frequency at TP21 should be greater than 1 MHz. The signal levels at TP24 and TP25 should be predominantly high. The voltage at TP40 should be about -2V.

If the signals at TP24 and TP25 are correct, but the voltage at TP40 does not change from approximately -2V to +28V as the frequency at TP21 is adjusted above and below 1 MHz, troubleshoot the following circuits:

- Loop amplifier U34 and associated circuitry
- Current source U63 and associated circuitry
- Switching diodes CR18 and CR19
- KN dac U6
- U7 and associated circuitry.

The loop should lock when you reconnect the shorting jumper between TP40 and TP41. If the loop does not lock, check low-pass filter L56, and L57 (and associated circuitry), clamp circuit U35 and U36 (and associated circuitry), and the lead-lag network. FET Q10 should be on (~+5V on the gate) when the undivided Subsynthesizer frequency is less than 230 MHz, and off (~0V on the gate) when the frequency is greater than 230 MHz. Disconnect CR20 and CR21 to disable the clamp circuit.

To check the various dac's, program the UUT to SPCL 943. This sets all the dac's to full scale. The voltage at the output of the KN dac (TP35), REFVOL dac (TP39) and STEERING dac (TP6) should be approximately 10.23V. When the UUT is programmed to SPCL 942, dac's to half scale, these voltages should be about 5.12V.

SUBSYNTHESIZER ADJUSTMENTS 6C-11.

The following procedures describe the five adjustments on the A4 Subsynthesizer PCA. These adjustments are as follows:

- R5, Steering dac full-scale adjustment
- R99, Lower clamp adjustment
- R98, Upper clamp Adjustment
- R106, SSB mixer LO drive adjustment
- L56, 10-kHz notch adjustment

NOTE

These adjustments are not routine and are required only when you replace the associated components or when you change the adjustment.

Steering DAC Full-Scale Adjustment 6C-12.

TEST EQUIPMENT:

- DVM

REMARKS:

The steering dac full-scale adjustment is normally required only when U5, U6, or associated components have been replaced, or when the adjustment has shifted.

PROCEDURE:

Adjust the steering dac voltage to 10.23V with the coarse loop steering dac set to full scale.

1. Program the UUT to SPCL 909.
2. Program the UUT to SPCL 943. This Special Function programs all dac's to full scale.
3. Connect the dvm to measure voltage between TP6 and ground.
4. Adjust R5 for 10.23V ±0.01V.
5. Program the UUT to SPCL 00. This clears all Special Functions.

Lower Clamp Adjustment, R99 6C-13.

TEST EQUIPMENT:

- Frequency counter

REMARKS:

The lower clamp adjustment, R99, is normally required only when replacing U35, U36, or associated components, when the A3 Subsynthesizer VCO has been repaired or replaced, or when the adjustment has shifted.

PROCEDURE:

Adjust the lower clamp frequency to 15 MHz with the reference to the phase detector disabled.

1. Connect output (J4) of the A3 Subsynthesizer VCO to the frequency counter. Set the frequency counter to measure with 1-kHz resolution.
2. Program the UUT to SPCL 909.
3. Program the UUT to 800 MHz. The frequency counter should read 16.000 MHz.
4. Short TP22 to ground.
5. Adjust R99 for a frequency counter reading of 15.000 MHz ±10 kHz.

Upper Clamp Adjustment, R98 6C-14.

TEST EQUIPMENT:

- Frequency counter

REMARKS:

The upper clamp adjustment, R98, is normally required only when replacing U35, U36, or associated components, when the A3 Subsynthesizer VCO has been repaired or replaced, or when the adjustment has shifted.

PROCEDURE:

Adjust the upper clamp frequency to 32.5 MHz with the N-divider signal to the phase detector disabled.

1. Connect the J4 output of the A3 Subsynthesizer VCO to the frequency counter. Set the frequency counter to measure with 1 kHz resolution.
2. Program the UUT to SPCL 909.
3. Program the UUT to 640 MHz. The frequency counter should read 32.000 MHz.
4. Short TP21 to ground.
5. Adjust R98 for a frequency counter reading of 32.500 MHz ±10 kHz.

SSB Mixer LO Drive Adjustment, R106 6C-15.

TEST EQUIPMENT:

- RF Probe (10X)
- Spectrum analyzer

REMARKS:

The SSB mixer lo drive adjustment, R106, is normally required only when replacing U50, U51, or associated components, when the A3 Subsynthesizer VCO has been repaired or replaced, or when the adjustment has shifted.

PROCEDURE:

Measure the SSB mixer LO Power with a 10X RF probe using a spectrum analyzer. Adjust the SSB mixer LO Power to -10 dBm as displayed on the spectrum analyzer. This corresponds to +10 dBm at the input to the coupler.

1. Program the UUT to SPCL 909.
2. Program the UUT to 800 MHz.
3. Connect the 10X RF probe to the input of the spectrum analyzer. Set the spectrum analyzer to -5 dBm reference level, 160 MHz, 1 MHz span, and 1 dB/div.
4. Touch the probe tip to the input of the coupler, U52, which connects to C147. This is best done on the top of the coupler with the ground connection on the coupler ground plane.
5. Adjust R106 for -10 dBm as displayed on the spectrum analyzer.

10-kHz Notch Adjustment, L56 6C-16.

TEST EQUIPMENT:

- Spectrum analyzer

REMARKS:

The 10 kHz notch adjustment is normally required only when L56, L57, and associated components have been replaced, or when the adjustment has shifted.

PROCEDURE:

A signal from the internal modulation oscillator is injected into the Subsynthesizer phase detector to produce a 10-kHz spur. Adjust L56 to minimize this spur.

1. Program the UUT to SPCL 909.
2. On the A3 Subsynthesizer VCO, move the jumper near J2 from TP1-TP2 to TP1-TP3. Reattach the cover on this side of the module.
3. Program the UUT to 800 MHz, modulation frequency 10 kHz, modulation level 100 mV. Connect the front panel MOD OUTPUT to TP36 on Subsynthesizer PCA.
4. Set spectrum analyzer to center 160 MHz, reference level 5 dBm, frequency span 100 kHz. The signal should be visible in the center of the screen with 10-kHz sidebands.
5. Adjust L56 to minimize these 10-kHz sidebands.
6. On the A3 Subsynthesizer VCO, move the jumper (near J2) back to TP1-TP2.

A3 SUBSYNTHESIZER VCO CIRCUIT DESCRIPTION 6C-17.

The A3 Subsynthesizer VCO PCA is controlled by the A4 Subsynthesizer PCA and produces a signal that is further processed in the A12 Sum Loop PCA. This assembly includes a varactor-tuned oscillator that generates frequencies from 160 to 320 MHz, along with low-pass filters and an ECL divide-by-ten circuit.

Q1 is configured as an oscillator, with a tunable resonant circuit connected between the base and collector to provide positive feedback. This circuit includes printed transmission lines, varactor diodes CR1-CR4, and inductor L1. The frequency tuning voltage at J1-4 is applied to the varactor diodes through RF choke L2, and tunes the oscillator over a 160 to 320 MHz range with voltages from about 2 to 22V.

The oscillator transistor output signal at Q1 emitter is next applied to Q2, configured as a common-base stage that provides isolation. The 0 dBm output of Q2 is applied to monolithic amplifier U1, which boosts the signal level to +13 dBm at its output.

Two switched low-pass filters, including PIN diodes CR5-CR8 and capacitors C13-C22, follow U1 and provide harmonic suppression. Comparator U4 senses tuning voltage VT, and enables the low band filter between CR5 and CR6 for VT less than 7.5V, and enables the high band filter between CR7 and CR8 for VT greater than 7.5V. The 7.5V switching voltage, corresponds to about 230 MHz.

The filtered signal is next applied to resistive splitter R13-R17. One output drives monolithic amplifier U2, which provides isolation and boosts the signal to about +7 dBm. This signal connects to the A4 Subsynthesizer PCA by a through-the-plate coaxial connector at P1. The other splitter output drives ECL divide-by-ten frequency divider U3. The divided output signal from U3 ranges in frequency from 16 to 32 MHz and is filtered by a five-element low-pass filter (L5, L6, C27-C29). The output signal connects by way of a coaxial cable to the A12 Sum Loop PCA at J2.

SUBSYNTHESIZER VCO TROUBLESHOOTING 6C-18.

A problem in the Subsynthesizer VCO can cause uncal status response 242 (Subsynthesizer unlock) and can also cause self-test failure 324. To test the vco independent of the Subsynthesizer PCA, connect a voltage source, such as an external power supply, to the phase lock port at J1 pin 4. This will override the voltage supplied by the Subsynthesizer PCA but will not damage the UUT. Vary the phase lock voltage from 2 to 23V, and observe the signal at connector J2 on a spectrum analyzer. Verify that the frequency varies from about 16 to 32 MHz, and that the level is about +2 dBm. If the signal does not change as described, troubleshoot the vco.

As a first step in troubleshooting, remove the plug-on jumper from TP1 to TP2, and install it to connect TP1 to TP3. This bypasses divider U3, and connects the fundamental oscillator signal to J2. (Remember to plug the jumper into its original position after troubleshooting.) This signal should vary from about 160 to 320 MHz at about +3 dBm over the tuning range. If this signal does not appear as described, troubleshoot the circuitry previous to the input of U3. Measure the dc voltages at various nodes in the circuit to help isolate the failed circuit. Table 6C-2 lists expected approximate dc voltages at various circuit nodes.

Table 6C-2. A3 Subsynthesizer VCO PCA DC Voltages

LOCATION	VOLTS DC
Q1 collector	+8.7
Q2 collector	+7.1
U1 output	+3.9
CR5/CR7/R10 node,V(phaselock) ~<7.5V	+2.3
CR5/CR7/R10 node,V(phaselock) ~>7.5V	-2.3
U2 output	+4.4
U3 pin 2	+3.5

A2 COARSE LOOP CIRCUIT DESCRIPTION 6C-19.

The Coarse Loop PCA generates frequencies from 576 to 960 MHz in 8-MHz steps. It also provides a 40-MHz reference for the Subsynthesizer, a 20-MHz signal for the modulation oscillator, and an 80-MHz signal for the output section. This 80-MHz signal is the local oscillator signal for the heterodyne band and is the reference for the FM circuitry.

The PCA consists of two major blocks: the reference section and the coarse loop. These blocks are described in the following paragraphs.

Reference Section 6C-20.

Refer to the Reference Section Block Diagram (Figure 6C-6) and the Coarse Loop PCA schematic diagram in Section 10 to identify major functional sections and to follow the signal paths of the coarse loop reference section.

The reference section is a phase-locked loop which includes a 40-MHz voltage-controlled crystal oscillator (VCXO), a divide-by-4, by-8, by-20, by-40, a digital phase frequency detector, and associated logic.

The main frequency reference for the instrument is either internal or external. The internal reference is a 10 MHz temperature-controlled crystal oscillator (TCXO), U501, or either the High-Stability (Option -130) or Medium-Stability (Option -132) ovened references. An external reference can be used in place of the internal 10 MHz reference, and can be 1, 2, 5, or 10 MHz.

When the instrument is set to internal reference (EXTREFH=0), the TCXO is turned on by enabling Q501 via open-collector comparator U509C and associated logic circuitry, U502 and U514. The 10-MHz signal from the TCXO is routed through U502 to multiplexer U504B. The output of the multiplexer is connected to the reference clock input of phase detector U503A and U511D.

If the optional high or medium-stability reference is installed (TCXOH=0), the TCXO is disabled. The 10 MHz signal from the optional reference is routed from J8 (REF IN BNC connector) to the phase detector.

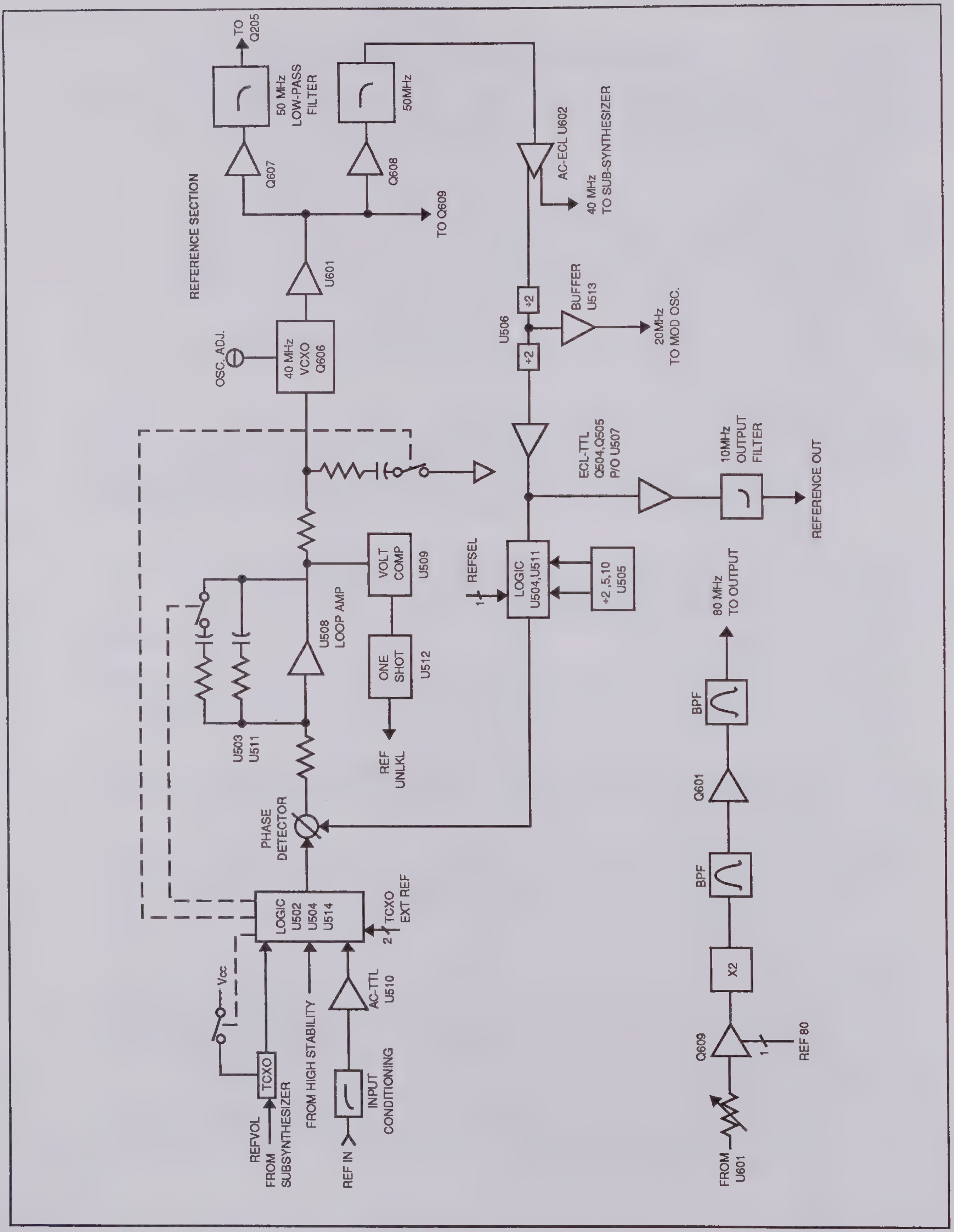

REFERENCE SECTION
TO Q205
50 MHz LOW-PASS FILTER
50MHz
Q607
Q608
TO Q609
AC-ECL U602
40 MHz TO SUB-SYNTHESIZER
U601
OSC. ADJ.
40 MHz VCXO Q606
U506
÷2
÷2
BUFFER U513
20MHz TO MOD OSC.
ECL-TTL Q504,Q505 P/O U507
10MHz OUTPUT FILTER
REFERENCE OUT
VOLT COMP
U509
REFSEL
1
LOGIC U504,U511
÷2 ,5,10 U505
80 MHz TO OUTPUT
U508 LOOP AMP
ONE SHOT
U512
REF UNLKL
U503 U511
PHASE DETECTOR
BPF
Q601
BPF
X2
Q609
1
REF 80
FROM U601
LOGIC U502 U504 U514
2
TCXO EXT REF
Vcc
AC-TTL U510
TCXO
REFVOL FROM SUBSYNTHESIZER
FROM HIGH STABILITY
INPUT CONDITIONING
REF IN

Figure 6C-6 Reference Section Block Diagram

When the instrument is set to external reference (EXTREF=1), the TCXO is turned off. The external signal from J6 is attenuated by R521 through R523, then clipped by CR501 and CR102, and input to a high-pass filter made up of C524 and C525, and L502. High-speed comparator U510 converts the external reference signal to TTL. The output of U510 is input to multiplexer U504B. A portion of the comparator output is fed back to the input to provide hysteresis (R524-R527).

The 40-MHz voltage-controlled crystal oscillator (VCXO) consists of four parts: the 40-MHz third-overtone crystal Y601, a grounded base stage made up of Q606 and associated components, a low-Q tuned circuit to ensure the crystal operates at the third overtone made up of L601, C604 and C605, and R602, and varactors CR603 through CR605.

This oscillator can be tuned approximately ±1 kHz. Feedback is from collector to emitter. The output from the collector-tuned circuit is lightly coupled by C607 to buffer amplifier U601. The output of the buffer is connected to the 80-MHz section (R606, R617, C610) and another pair of grounded base stages Q607 and Q608. The outputs of these buffers are filtered by a low-pass filter made up of C616, C617, L604, C622, C623, and L605. The output of Q608 is converted to ECL in U602, while the other output drives the main loop phase detector buffer amplifier Q205.

One output of U602 provides the 40-MHz reference for the A4 Subsynthesizer via J16. The same output is also clocked into U506A, divided by 2, and buffered by U513. The 20-MHz square wave is output to bandpass filter R536, L510, and C545 before being sent to the A6 Modulation Oscillator via J8.

A second divide-by-2 counter (U506B) divides the 20 MHz to 10 MHz. This ECL signal is converted to TTL by Q504 and Q505 and buffered by U507C. Two inverters in parallel (U507A,B) drive a low-pass filter consisting of C518, C519, C550, and L501. This filter outputs a 10-MHz sine wave, which is the reference out for the instrument (J7).

When in internal reference, the 10-MHz signal from U507C is routed through multiplexer U504A to the CK input of phase frequency detector U503B, and U511D. When in external reference (10 MHz), divider U505 is disabled and the signal from U507C is routed through multiplexer U504C and logic circuit U511A,B to the R input of the phase frequency detector.

When Special Function 761 is enabled, the 10-MHz signal is divided to 1 MHz, 2 MHz, or 5 MHz by U505, depending on how the switches in SW502 are set. The output of the divider is also routed to the phase frequency detector.

Phase frequency detector U503 and U511D compares the phase/frequency of the divided 40-MHz VCXO (V input) with either the 10-MHz TCXO, the high or medium stability optional reference, or an external reference. The phase detector operates at 10 MHz, except when an external reference of 1, 2, or 5 MHz is used. In these cases, it operates at the reference frequency.

The output of this phase detector operates in the differential voltage mode. If the frequency/phase of the V input (U503B pin 11) is greater than the R input (U503A pin 3), there will be a net positive voltage from U503A pin 6 to U503B pin 8. The loop amplifier/integrator (U508 and associated components), which drives a lead-lag network made up of R532, R530, C546, and Q502, integrates the phase detector voltage and causes the voltage on the control line to varactors CR603 through CR605 to drop until the two frequencies match and the loop is locked. Consequently, if the frequency/phase of the R input is greater than the V input, the net voltage will be negative, and the control voltage will rise until the loop is locked.

A small phase offset is set (R512) to keep the phase detector in its linear region. The bandwidth of this reference loop is changed by switching in various lead-lag networks (R505, R510, R530, R532, C530, C547, C549, C546). When in internal TCXO or external 10 or 5 MHz, Q506 and Q502 are on and the loop bandwidth is approximately 30 Hz. When the external reference is 1 or 2 MHz, Q506 is on and Q502 is off. Turning off Q502 increases the gain by five times, but since the division factor is five times greater, the overall loop gain remains approximately constant. When the medium or high stability optional internal reference is active, both Q502 and Q510 are off and the loop bandwith is approximately 500 Hz.

The loop control voltage (U508 pin 6) is sensed by two comparators U509A,B. If the voltage is less than approximately 1.2V and more than approximately 11V or if the voltage is pulsing, the loop is unlocked. One-shot U512 converts these pulses into a logic signal. This is combined with the low and high voltage detector to produce REFUNLKL, which is sent to the controller.

The 40 MHz from buffer U601 is amplified by Q609 and doubled to 80 MHz by full-wave rectifier T601, CR601, and CR602. The 80 MHz is filtered by L611, L612, C643, and C644. Then the 80 MHz is amplified by Q610, and filtered again by C649, C50, L613, and L615. This 80-MHz signal is sent to the output section via J5. When in the dc FM mode and not in the heterodyne band, this signal is turned off by Q611 via the REF80H signal.

Coarse Loop 6C-21.

Refer to the Coarse Loop Block Diagram (Figure 6C-7) and the Coarse Loop PCA schematic diagram in Section 10 to identify the major functional sections and follow the signal paths of the coarse loop.

The coarse loop consists of two interlocking loops: the main phase-locked loop and the discriminator loop around the vco. (The discriminator loop reduces the phase noise of the vco.)

A 576- to 960-MHz signal from the A5 Coarse Loop VCO is attenuated, amplified by U401, attenuated again, and amplified a second time by U405. This signal drives divide-by-4 prescaler U301. The 144- to 240-MHz output of the prescaler is amplified to ECL levels by U311 and is input to the N-divider.

The main N-divider consists of two parts: a programmable divide by ¾/5/6/7 (made up of U302, U303, U308, and U310), and a programmable 5-bit rate multiplier (made up of U304, U305, U306, and U307). The divide by ¾/5/6/7 is a ring counter with different feedback paths selected to change the division. It is programmed with the CF0/CF1 bits to a steady-state value of N = 3, 4, 5, or 6. A toggle line (TP2) allows the divider to be programmed to one more than its steady-state value (N+1).

The rate multiplier generates a sequence of 0 to 19 pulses within a 40-MHz frame. The output of the rate multiplier drives the TP2 toggle line. Consequently, the divider divides by N part of the frame and N+1 for the remainder of the frame. Fractional division with a 2-MHz step size is obtained depending on the programming of the rate multiplier. Because of the divide-by-4 prescaler, this corresponds to a 8-MHz step at the Coarse Loop VCO frequency.

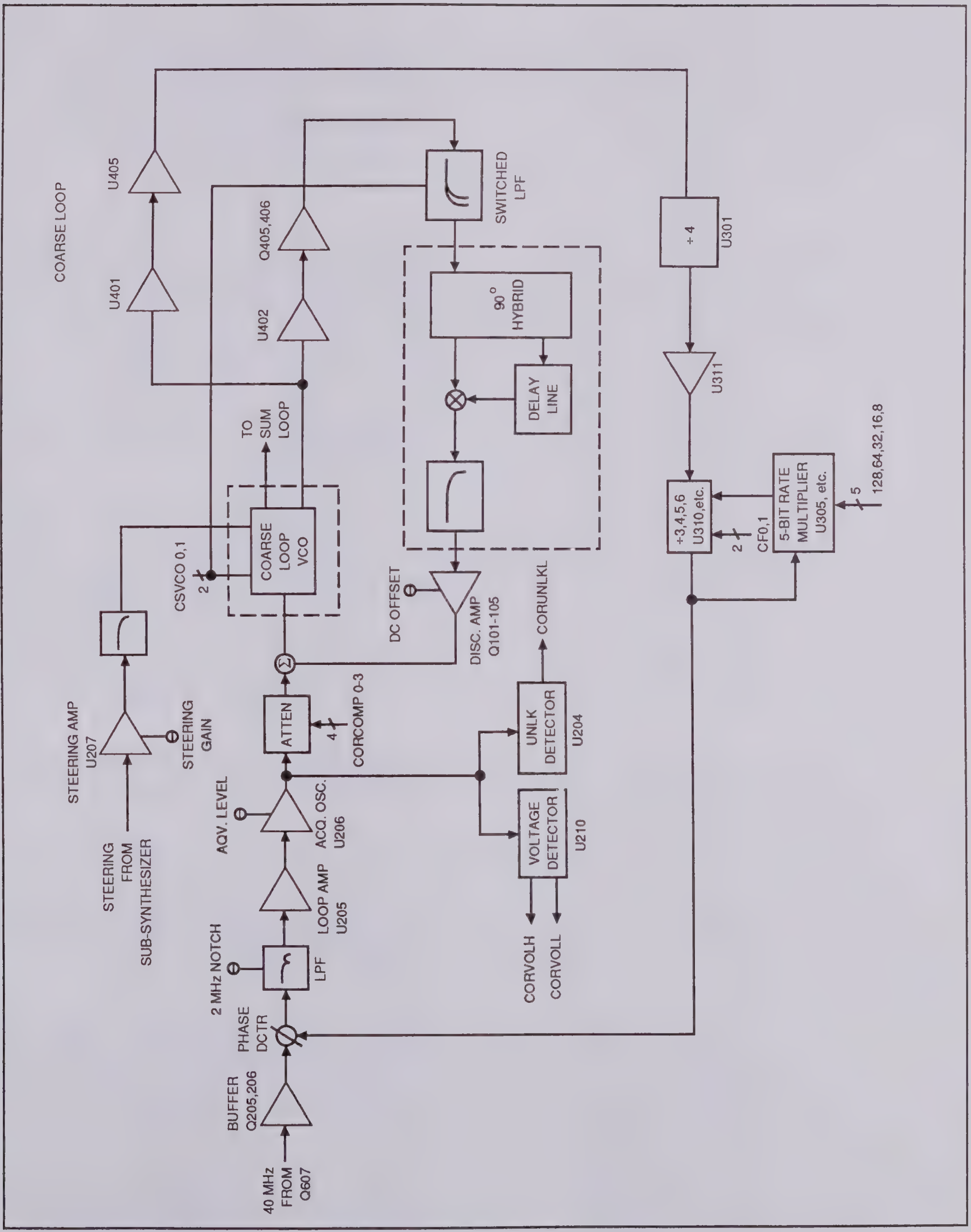

COARSE LOOP
U405
U401
Q405,406
U402
SWITCHED LPF
90° HYBRID
DELAY LINE
÷ 4
U301
U311
TO SUM LOOP
COARSE LOOP VCO
CSVCO 0,1
2
DC OFFSET
DISC. AMP Q101-105
CORUNLKL
÷3,4,5,6 U310,etc.
2
CF0,1
5-BIT RATE MULTIPLIER U305, etc.
5
128,64,32,16,8
STEERING AMP U207
STEERING GAIN
STEERING FROM SUB-SYNTHESIZER
ATTEN
4
CORCOMP 0-3
AQV. LEVEL
ACQ. OSC. U206
UNLK DETECTOR U204
VOLTAGE DETECTOR U210
LOOP AMP U205
CORVOLH
CORVOLL
2 MHz NOTCH
LPF
PHASE DCTR
BUFFER Q205,206
40 MHz FROM Q607

Figure 6C-7. A5 Coarse Loop Block Diagram

The outputs of N-divider U308D are connected to mixer phase detector U203. The 40 MHz from the reference section is buffered in a common base stage Q205 and amplified by Q206 to provide a second input to the phase detector. The output of the phase detector is input to the low-pass filter, C212 through CR216 and L204 and L205, with notches at 2 and 4 MHz to suppress the rate multiplier spurs. A lead-lag network made up of R210, R211, and C211 provides proper high-frequency termination for the mixer.

The output of the low-pass filter is connected to loop amplifier U205. This amplifier provides lead-lag compensation for the phase-locked loop. The output of this stage is fed into the acquisition oscillator state U206. This is set up as a Wien bridge oscillator consisting of R225 through R228, C228 and C229 at a frequency of approximately 100 Hz. Since the phase detector is not a phase/frequency detector, the beat frequency at the output of the phase detector must be small in order for the loop to lock. When the loop is unlocked, the Wien bridge oscillator is oscillating, and the vco frequency is slowly swept about its steered frequency. This causes the beat frequency to be slowly swept close to 0. When the loop locks, there is enough gain around the loop so the oscillation condition for the Wien bridge is no longer met and it stops oscillating. One-shot U204 trips when the Wien bridge oscillates to indicate an out-of-lock condition. This signal (CORUNLKL) is sent to the controller.

The output of the acquisition oscillator U206 is fed into a programmable lead-lag network made up of R229 through R237, C231 through C235, and Q201 through Q204. Since the tuning slope of the vco, in MHz/V, is not constant, this network is programmed to reduce the magnitude of the change. The output of this network is connected to the phase-lock port of the A5 Coarse Loop VCO via J4. This network forms part of the compensation of the discriminator loop. Comparator U208 converts the TTL programming input to 0/10V to drive the FETs. Comparator U210 monitors the phase-lock voltage and generates signals when the voltage exceeds -5V (CORVOLH) or +5V (CORVOLL). This voltage is used for the Coarse Loop VCO compensation.

A 500-Hz active Bessel filter, U207, amplifies and filters the steering voltage from the A4 Subsynthesizer PCA, input via J1-16. The same signal is then sent to the A5 Coarse Loop VCO via J15.

The discriminator circuit senses the frequency noise of the vco and generates a correction signal to reduce the noise. A portion of the RF output from the Coarse Loop VCO (P2) is amplified by U402 and fed into the two-stage limiting power amplifier Q405 and Q406. The output of the amplifier is filtered by C422 through C426, CR402, and CR403. This filter switches at 712 MHz, the same point as a vco band change. Op amp U209 drives PIN diode switches CR402 and CR403.

The output power from the filter is approximately +20 dBm to the 90-degree power splitter on the A25 Discriminator Board. The outputs of the power splitter are connected to the LO input of the mixer U404 and to the delay cable. The other end of the delay cable is connected to the RF input of the mixer. The delay cable is trimmed, so as the coarse loop steps in 8-MHz increments, the phase is such that the IF output is approximately 0V dc.

A filter made up of C418 through C421, L403, L404, R419, and R420 is connected to the IF port. This filter provides both UHF and HF terminations for the mixer. The output of the filter is ac-coupled by C101 and R106 to low noise amplifier Q101 through Q106. The output of this amplifier is resistively summed at R123 and R125 with the phase lock voltage from U206. Diodes CR101 and CR102 limit the output of the discriminator amplifier while in the acquisition mode. To ensure stability, the gain of the low noise amplifier is rolled off by C104 and R119.

COARSE LOOP TROUBLESHOOTING 6C-22.

The A2 Coarse Loop consists of two sections: the reference section and the main coarse loop. These sections are described in the following paragraphs.

Reference Section 6C-23.

A status code 246 indicates a problem in the reference section. This code is displayed when the Signal Generator is set to external reference but no reference is supplied. It is also displayed if the reference is the wrong frequency or is outside the lock range specification. If the unit is set to internal reference and the high or medium stability option is installed, check to see that the 10-MHz output from the option is correct.

If the voltage at TP19 measures approximately -13V, it indicates a problem with the internal TCXO, the internal/external reference circuitry, or the phase detector/loop amplifier. If the voltage measures approximately 13V, it indicates a problem in the 40-MHz oscillator, buffers, dividers, or phase detector/loop amplifier.

Use a 10MΩ, 8 pF probe and make a ground connection, less than 1 inch of lead length, at the probe tip. Voltages measured with an oscilloscope are approximate. Because the reference loop is not locked, frequencies given here are not exact and will typically be slightly higher than indicated. Check the oscillator for 40 MHz 1.4V p-p at TP4.

To check the reference circuitry, proceed as follows:

1. Check the junctions of L605 and C624, L604 and C625, and C617 and C625 for a 630 mV p-p signal.
2. Check U602 pin 2 for a 40-MHz ECL signal.
3. Check TP17, which connects to the A4 Subsynthesizer, for a 700 mV p-p signal.
4. Check the output of the first divide-by-2, U506 pin 15, for a 20-MHz ECL square wave.
5. At TP17 following buffer U513, which supplies the A6 Modulation Oscillator, check for a 20 MHz, 1.2V p-p signal.
6. At U506 pins 2 and 3 check for a 10-MHz ECL square wave.
7. At the collector of Q505, check for a 10-MHz TTL signal.
8. At J7, the 10 MHZ OUT connector, check for a 10-MHz 5V p-p sine wave.
9. If the voltage at TP19 is approximately -13V when in internal reference, first check the internal TCXO. There should be a 10-MHz TTL signal at U502 pin 12 and U503 pin 3. Power to the TCXO is supplied from Q501 at TP18.

NOTE

If the optional medium or high stability reference is installed, no power should be supplied to the TCXO and there should be a 10 MHz TTL signal at J8 and at pin 3 of U503.

10. If the instrument is set to internal or external 10-MHz reference, REFSEL should be a logic high. There should be a 10-MHz TTL signal at the phase detector input, U503 pin 11.

11. If the instrument is set to the 1-MHz, 2-MHz, 5-MHz external reference mode (SPCL 761), REFSEL should be a logic low. The signal at U503 pin 11 is 1, 2, or 5 MHz (configured for 5 MHz at the factory), depending on the setting of SW502. Refer to the alignment section for information on how to set this switch.

12. To check the external reference, connect a 10-MHz source, +4 dBm signal to the REF IN connector. There should be a 1V p-p sine wave at J6. There should be a 10-MHz TTL signal at U510 pins 9 and 11 and eventually at U503 pin 5. The logic control for the reference section is summarized in Table 6C-3.

13. You should observe 10-MHz signals at U503 pins 3 and 11. To check the phase detector, remove the jumper between TP20 and TP21. Connect a variable power supply to TP21. Monitor the frequency at U503 pin 11. As you adjust the power supply from about 1 to 10V, the frequency at TP11 should increase and decrease around 10 MHz by about ±200-500 Hz. The voltage at TP19 should range between -13 and +13V. Reconnect the jumper between TP20-TP21.

14. The final check is the out-of-lock circuitry, which consists of U509, U512, and U515. When the control voltage is between 1 to 11V, the signal at J2-2 should be a TTL high.

Table 6C-3. Reference Section Logic Control Line Summary

STATE	EXTREFH	TCXOH	REFSEL	Q502	Q506
External 10 MHz	1	Y	1	On(+5V)	on(+15V)
External 5 MHz	1	Y	0	On	On
External 2 MHz	1	Y	0	Off(0V)	On
External 1 MHz	1	Y	0	Off	On
Internal TCXO	0	1	X*	On	On
Internal HI/MED ref	0	0	X	Off	Off

X = 1 if using 10 MHz external reference; 0 if using SPCL 761 (1, 2, or 5, MHz external reference).
Y = 1 if using standard TCXO; 0 if using high or medium stability option.

To troubleshoot the 80-MHz doubler section, proceed as follows:

1. Check the bias voltages. The voltage should be about 8.8V at the junction of R648, C652, and T601. The voltage at the collector of Q610 should be about 8.1V.
2. Check for the collector of Q609 for an ac voltage of 40 MHz, 2.7V p-p.
3. Check the output of the doubler CR601 and CR602 for an 80-MHz full-wave rectified signal of 1.2V p-p.
4. Check for an 80-MHz 0.8V p-p sine wave at J5.

Main Loop 6C-24.

Status code 243 indicates that the coarse loop is out of lock. Status codes 244 or 245, which indicate the sum loop is out of lock, could be caused by a marginal lock condition in the coarse loop.

When any of these codes are present, check the coarse loop steering circuit first, as follows:

1. Program the coarse loop to 640 MHz by setting the UUT to 544 MHz.
2. Connect the output of the Coarse Loop VCO, A2-J8, to a spectrum analyzer.
3. Ground the phase lock port, TP7 and disable the search oscillator by moving the jumper from TP13 to TP28-TP13.
4. There should be a signal at 640 MHz ±2 MHz. If the signal is absent or it is far off frequency, either the Coarse Loop VCO or the vco steering voltage circuit has failed.
5. Program the UUT with SPCL 943 and measure the dc voltage at TP8, the vco steering port. This special function programs the steering dac to full scale, and should result in a reading of 24V. If the Coarse Loop VCO seems to function properly, the Coarse Loop PCA is probably at fault.
6. Using a 500Ω, 10X probe connected to the spectrum analyzer, compare the levels in the RF section with those in Table 6C-4. These levels are as measured on the spectrum analyzer. The actual level is 20 dB higher.

NOTE

The levels in Table 6C-4 are approximate and can vary as much as ±3 dB.

Table 6C-4. Coarse Loop RF Levels

CONNECTION POINT	LEVEL
P2	-14 dBm
U401 output	-18 dBm
U405 output	-16 dBm
U402 output	-16 dBm

7. At the output of the divide-by-4 amplifier, use a 500Ω, 10X probe to check for a 160 MHz, -16 dBm signal.

8. The N-divider programs the coarse loop in 8-MHz steps. The output of the N-divider, TP1, should be approximately 40 MHz, ECL level. There should not be any signal at TP2 for coarse loop frequencies of 640 MHz, 800 MHz, and 960 MHz.

9. If the rate multiplier divider (U305 and related circuitry) is working correctly, there should be a 2-MHz ECL signal at U305 pin 14. The programming to the rate multiplier (128-, 64-, 32-, 16-, and 8-MHz bits) is active low. There are 20 steps in the rate multiplier programming. The logic states for the N-divider are given in Table 6C-5.

10. If the N-divider is functional, check the mixer amplifier Q205 and Q206.

11. Check the collector bias at C273 for approximately 8V.

12. Check for a 40-MHz 1.2V p-p signal at TP5.

13. Check the output of the filter, TP11, for a 500-mV p-p slightly triangular signal. The frequency is below 125 kHz, and its exact value is a function of how close the programmed RF output signal is to 640 MHz.

14. Re-enable the search oscillator by removing the ground from TP28-TP13 and grounding TP11. There should be a 100 Hz 10V p-p sine wave (~0V dc) at TP6.

15. Program the UUT to SPCL 943. This programs the dac's to full scale, which turns Q201 through Q204 on. There should be a 100-Hz 650 mV p-p sine wave at TP7.

16. Clear the UUT. Remove the jumper between TP7 and ground. The loop should be locked. If the loop still does not lock, ground TP9. If the loop locks, the problem is in the delay line discriminator section. If the loop is locked and status code 243 is still present, check the unlock detector, U204.

If the phase noise of the UUT is beyond specified limits, the problem could be in the discriminator section. Check it as follows:

1. Measure the dc voltage at TP1 on the A25 Discriminator PCA. It should be ±200 mV as the RF frequency is changed.

2. If the voltage is nearly zero, remove the semi-rigid cable connected to J10, and measure the power with the spectrum analyzer. The power should be between +9 and +14 dBm depending on the frequency.

3. If there is no power or if the power is low, use the spectrum analyzer with 500Ω 10X probe to compare the RF power amplifier levels at Q404 and Q405 with those listed in Table 6C-6. The actual levels are 20 dB higher. The levels in Table 6C-6 are approximate and can vary as much as ±3 dB.

4. The Q404 and Q405 collector bias voltages should be 10.4V and 5.1V.

Table 6C-5. N-Divider Logic States

FRONT PANEL FREQUENCY (MHz)	COARSE LOOP FREQUENCY (MHz)	LOGIC STATE						
		CF1	CF0	128	64	32	16	8
15.00	576	0	0	1	0	0	1	1
15.25	584	0	0	1	0	0	1	0
15.50	592	0	0	1	0	0	0	1
15.75	600	0	0	1	0	0	0	0
512	608	0	0	0	1	1	1	1
520	616	0	0	0	1	1	1	0
528	624	0	0	0	1	1	0	1
536	632	0	0	0	1	1	0	0
544	640	0	1	1	1	1	1	1
552	648	0	1	1	1	1	1	0
560	656	0	1	1	1	1	0	1
568	664	0	1	1	1	1	0	0
576	672	0	1	1	1	0	1	1
584	680	0	1	1	1	0	1	0
592	688	0	1	1	1	0	0	1
600	696	0	1	1	1	0	0	0
608	704	0	1	1	0	1	1	1
616	712	0	1	1	0	1	1	0
624	720	0	1	1	0	1	0	1
632	728	0	1	1	0	1	0	0
640	736	0	1	1	0	0	1	1
648	744	0	1	1	0	0	1	0
656	752	0	1	1	0	0	0	1
664	760	0	1	1	0	0	0	0
672	768	0	1	0	1	1	1	1
680	776	0	1	0	1	1	1	0
688	784	0	1	0	1	1	0	1
696	792	0	1	0	1	1	0	0
704	800	1	0	1	1	1	1	1
896	808	1	0	1	1	1	1	0
904	816	1	0	1	1	1	0	1
912	824	1	0	1	1	1	0	0
920	832	1	0	1	1	0	1	1
928	840	1	0	1	1	0	1	0
936	848	1	0	1	1	0	0	1
944	856	1	0	1	1	0	0	0
952	864	1	1	1	0	1	1	1
960	872	1	0	1	0	1	1	0
968	880	1	0	1	0	1	0	1
976	888	1	0	1	0	1	0	0
984	896	1	0	1	0	0	1	1
992	904	1	0	1	0	0	1	0
1000	912	1	0	1	0	0	0	1
1008	920	1	0	1	0	0	0	0
1016	928	1	0	0	1	1	1	1
1024	936	1	0	0	1	1	1	0
1032	944	1	0	0	1	1	0	1
1040	952	1	0	0	1	1	0	0
1048	960	1	1	1	1	1	1	1

Table 6C-6. Discriminator RF Section Levels

FRONT PANEL FREQUENCY	COARSE LOOP FREQUENCY	Q404-C	Q405-C	C421	A25-J9
544 MHz	640 MHz	-9 dBm	+3 dBm	+3 dBm	+3 dBm
704 MHz	800 MHz	-11 dBm	-3 dBm	0 dBm	-6 dBm
1048 MHz	960 MHz	-9 dBm	-2 dBm	-2 dBm	-5 dBM

5. If the power is correct at the collector of Q405 but low at C421, the problem is probably in the switched low-pass filter. If the power is correct at C421 but low at the cable connecting to J10, the problem is probably in the coupler or delay line. If the power is correct at the output of the delay line and the dc voltage at the output of the mixer is nearly zero, the problem is probably a defective mixer. Problems with the delay line assembly necessitate replacing the whole assembly, including the cable.

To check the discriminator amplifier, which consists of Q101 through Q105, proceed as follows:

1. Remove the end of the resistor that connects to J3 on the A25 Discriminator PCA.
2. Connect the resistor to the UUT front panel MOD OUTPUT.
3. Program the UUT to MOD FREQ 1 kHz and MOD LEVEL 4 mV. There should be a 500-mV p-p 1 kHz signal at TP9.

COARSE LOOP PCA ADJUSTMENTS 6C-25.

Refer to Table 6C-7 for information about the test points for the A2 Coarse Loop PCA. The following procedures cover the five adjustments on the A2 Coarse Loop PCA:

- R102, Discriminator video amplifier offset
- R221, Steering gain adjustment
- R227, Acquisition oscillator level adjustment
- L601, 40-MHz oscillator adjustment
- L612 and L613, 80-MHz filter tuning
- R617, 80-MHz level adjustment
- L205, 2-MHz notch adjustment
- SW502, Alternate reference frequency selection

NOTE

These adjustments are not routine and are required only when you replace the associated components or when the adjustment has been changed or has shifted. An exception is SW502, the alternate reference frequency selection, which you may need to change whenever required by your external reference applications.

Table 6C-7. A2 Coarse Loop PCA Test Points

TEST POINT	SIGNAL TYPE	RANGE	TYPICAL	SIGNAL DESCRIPTION
TP1	ECL	40 MHz	800 mV p-p	N-divider Output
TP2	ECL	0 to 16 MHz	2 MHz 25 ns AH	Rate Multiplier Output
TP3	RF-ECL	120 to 240 MHz	162 MHz,+5 dBm*	Divide-by-4 Prescaler Output
TP4	ac	40 MHz	1V p-p	40-MHz Oscillator Output
TP5	ac	40 MHz	1.2V p-p	40-MHz Reference Amplifier Output
TP6	dc	+/-1V	Varies	Loop Amplifier/Acquisition Oscillator Output
TP7	dc	+/-0.1V	Varies	VCO Phase-Lock Port
TP8	dc	2 to 22V	11V	VCO Steering Port
TP9	dc	+/-50 mV	Varies	Discriminator Loop Amplifier Output
TP10				Input for Test
TP11	dc	+/-50 mV	Varies	Low-Pass Filter Output
TP12	Ground			
TP13	Shorting	-	-	Disables Acquisition Oscillator Connection
TP14	Ground			
TP15	TTL	10 MHz	150 ns AL	Reference Loop Phase Detector Output
TP16	ac	20 MHz	1V p-p	20-MHz Reference to Modulation Oscillator
TP17	ac	40 MHz	800 mV p-p	40-MHz Reference to Subsynthesizer
TP18	dc	12.7 +/-0.2V 0.8 +/-0.2V	Constant Constant	On when internal TXCO Off when external or high/medium stability option
TP19	dc	1 to 11V	5.6V	Reference Loop Amplifier Output
TP20	Shorting Connection			Opens reference loop for troubleshooting

* As measured with 500 ohm 10X RF probe (TEK 6156). Actual level as displayed on spectrum analyzer will be approximately 20 dB lower.

Discriminator Video Amplifier Offset Adjustment, R102 6C-26.

TEST EQUIPMENT:

- DVM

REMARKS:

Discriminator video amplifier offset adjustment is normally required only when Q102 or any associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

The output of the discriminator video amplifier (TP9) is adjusted to 0V dc.

1. Program the UUT to SPCL 909.
2. Connect the dvm to measure voltage between TP9 and ground.
3. Adjust R102 for 0V ±10 mV.

Steering Gain Adjustment, R221 6C-27.

TEST EQUIPMENT:

- DVM

REMARKS:

The steering gain adjustment is normally required only when U207 or any associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

The Coarse Loop VCO steering voltage is adjusted to 24V with the Coarse Loop VCO steering dac set to full scale.

1. Program the UUT to SPCL 909.
2. Program the UUT to SPCL 943. This Special Function programs all dac's to full scale.
3. Connect the dvm to measure the voltage between TP8 and ground (TP14).
4. Adjust R221 for 24.00V ±.01V.
5. Program the UUT for SPCL 00. This clears all Special Functions.

Acquisition Oscillator Level Adjustment, R227 6C-28.

TEST EQUIPMENT:

- DVM

REMARKS:

The acquisition oscillator level adjustment is normally required only when U206 or any associated components have been replaced, or when the adjustment has shifted.

PROCEDURE:

Acquisition oscillator level at TP6 is adjusted for 3.54V rms with the phase-locked loop disabled.

1. Connect TP11 to ground (TP13) with a clip lead.
2. Connect the DVM to measure the ac voltage between TP6 and ground.
3. Adjust R227 for 3.54V rms ±0.10V.

40-MHz Oscillator Adjustment, L601 6C-29.

TEST Equipment:

- Frequency counter
- DVM

REMARKS:

The 40-MHz oscillator adjustment is normally required only when Q606 or any associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

The 40-MHz oscillator is adjusted to 40 MHz with the crystal removed from the circuit.

1. Program the UUT to SPCL 909, and select internal reference.
2. Connect counter external reference OUT to UUT 10 MHZ IN. Set UUT to EXT REF.
3. Move the jumper from TP22-TP24 to TP22-TP23, and move the jumper from TP26-TP27 to TP25-TP26. This removes the crystal from the circuit.
4. Connect the frequency counter to TP4. Set for 1-kHz resolution.
5. Adjust L601 for 40 MHz ±10 kHz.
6. Replace the jumpers to original positions.

7. Set the frequency counter for 1-Hz resolution. Verify the frequency is 40 MHz ±1 count on the frequency counter.

8. Measure voltage at TP19. It should be between 4.5 and 7.5V dc.

80-MHz Filter Tuning, L612 and L613 6C-30.

TEST EQUIPMENT:

- Spectrum analyzer

REMARKS:

Tuning the 80-MHz filter is normally required only when components in the doubler section, Q609, Q610 and related components, have been replaced, or when the adjustment has shifted.

PROCEDURE:

The 80-MHz output from the coarse loop is adjusted for the maximum level.

1. Program the UUT to SPCL 909.

2. Remove the cable and connect the spectrum analyzer to A2-J5. Set the spectrum analyzer to 80 MHz, 1-MHz span, and 10-dBM reference level.

3. Adjust L612 for the maximum level.

4. Adjust L613 for the maximum level.

5. Repeat steps 3 and 4 until the level no longer increases.

6. Reinstall the cable.

80-MHz Level Adjustment, R617 6C-31.

TEST EQUIPMENT:

- Spectrum analyzer

REMARKS:

The 80-MHz level adjustment is normally required only when Q606, Q609, Q610, U601 and associated components have been replaced, or when the adjustment has been changed or has shifted. This adjustment should be done after L612 and L613 have been adjusted.

PROCEDURE:

The 80-MHz level from A2-J5 is adjusted to 4 dBm.

1. Program UUT to SPCL 909.

2. Remove the cable from A2-J15. Connect A2-J15 to the spectrum analyzer. Set the spectrum analyzer to 80 MHz, 1 MHz-span and 10-dBm reference level.

3. Adjust R617 for 4 dBm ±0.2.
4. Reconnect the cable to A2-J15.

2-MHz Notch Adjustment, L205 6C-32.

TEST EQUIPMENT:

- Spectrum analyzer

REMARKS:

The 2-MHz notch adjustment is normally required only if L205 and associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

The 2-MHz signal at the output of the acquisition oscillator is minimized.

1. Program the UUT to SPCL 909.
2. Program the UUT to 15.25 MHz.
3. Connect the spectrum analyzer to TP6 with clip leads. Set the spectrum analyzer to center 2 MHz, 100-kHz span, and ref level -20 dB.
4. As L205 is adjusted inward, a signal should become visible on the spectrum analyzer. Adjust L205 to minimize this signal.

Alternate Reference Frequency Selection 6C-33.

REMARKS:

The unit is configured at the factory to accept a 5-MHz external reference when the unit is in alternate reference frequency mode, SPCL 761. You can change the alternate reference from 5 MHz to 1 or 2 MHz by changing the position of switch SW502.

PROCEDURE:

1. On the synthesizer module bottom cover, remove the metal hole plug labeled A2S502.
2. Set the switches as shown in Table 6C-8.

Table 6C-8. Setting SW502 for Alternate Reference Frequency

REFERENCE FREQUENCY	SW502 Switch Segments					
	1	2	3	4	5	6
5 MHz	ON	ON	OFF	OFF	ON	OFF
2 MHz	OFF	OFF	ON	ON	OFF	OFF
1 MHz	OFF	ON	OFF	ON	OFF	ON

A5 COARSE LOOP VCO CIRCUIT DESCRIPTION 6C-34.

The A5 Coarse Loop VCO PCA is controlled by the A2 Coarse Loop PCA and produces a signal that is further processed in the A12 Sum Loop PCA. This assembly includes three varactor-tuned oscillator circuits that cover the frequency range 576 to 960 MHz, programmed by binary control signals CSVCO0H and CSVCO1H, as listed in Table 6C-9.

The three oscillator circuits are designed similarly but have different element values and printed transmission line lengths to cover the three bands. Because the three circuits operate the same, the following discussion specifies only the reference designators for the band 1 oscillator. Refer to the A5 Coarse Loop VCO schematic diagram in Section 10 to locate corresponding elements for the other two oscillators. (Components for each band are identified on the schematic.)

Band 1 oscillator uses a common-base transistor, Q3, configured for negative resistance at the emitter. The emitter is coupled to a resonator that consists of a printed transmission line in series with varactor diodes CR5 and CR6, and low loss porcelain capacitors C5 and C6. Two tuning voltage lines connect to the varactor cathodes and anodes via RF chokes L6 and L3, respectively. The cathodes connect to the vco steering port, J6. The anodes connect to the vco phase lock port, J5. These ports are used by the A2 Coarse Loop PCA to control the operating frequency. The voltage across the varactors, measured between J6 and J5, varies approximately linearly with frequency in each band, from about 2V to 20V.

The +13 dBm nominal signal at the oscillator transistor collector is applied to an 8-dB attenuator R13 through R15 that provides isolation, and then to a low-pass filter consisting of C41, C42, and printed lines that attenuates harmonics to less than -20 dBc. PIN diode CR9 has low RF resistance and passes the oscillator signal when the oscillator is on and goes to a high impedance when the oscillator is off.

Band control signals CSVCO0H and CSVCO1H are decoded by U3 and Q4 through Q8. This circuit applies bias current only to the selected oscillator transistor so that only one oscillator is activated per band.

PIN diodes CR7 through CR9 connect the active oscillator to a resistive signal splitter, R21 and R22, which drives monolithic 11 dB amplifiers U1 and U2. The +7 dBm output of U1 connects to the A2 Coarse Loop PCA at J7 by a through-the-plate coaxial connector, and the output of U2, also at +7 dBm, connects to the A12 Sum Loop PCA at J8 by a coaxial cable.

Table 6C-9. Coarse Loop VCO Binary Band Control Signals

BAND	FREQUENCY RANGE (MHz)	CSVCO0H	CSVCO1H
1	576 to 704	0	0
2	712 to 824	0	1
3	832 to 968	1	1

COARSE LOOP VCO TROUBLESHOOTING 6C-35.

The Coarse Loop VCO PCA, controlled by the Coarse Loop PCA, generates the coarse loop signal that is further processed in the A12 Sum Loop PCA. A problem with the Coarse Loop VCO can cause Coarse Loop Unlock status code 243 to appear. Self-test error codes 320 through 323 can also be triggered by a failed A9 Sum Loop VCO. To determine if a failure is due to the Coarse Loop VCO rather than another assembly, perform the following tests:

1. Ground J5, the phase-lock port of the vco with a clip lead and measure the dc voltage at J6 with the UUT programmed to SPCL 943 (all dac's to full scale). The reading should be 24.00V.

2. Program the UUT to SPCL 942 (all dac's to half scale). The reading should be 12.00V. This tests the vco steering voltage circuit.

3. With J5 still grounded, examine the output at connector J8 with a spectrum analyzer as the frequency is stepped in 8 MHz increments from 512 MHz to 1056 MHz. The frequency should always be within about 2 MHz of expected coarse loop frequency, and the level should be approximately +5 dBm. (The expected coarse-loop frequency can be displayed by entering SPCL 946.) If the signal is good, the problem is likely in another PCA. If the signal is incorrect only over a frequency band corresponding to one of the vco bands, the associated vco circuit is likely at fault.

4. Measure dc voltages at various circuit nodes with the UUT programmed to 600 MHz, 700 MHz, and 1000 MHz to enable each of the three bands. Compare your readings with Table 6C-10. These measurements should help isolate the problem circuit.

SUM LOOP BLOCK DIAGRAM 6C-36.

Refer to the Sum Loop Block Diagram (see Figure 6C-8) to identify major functional sections and to follow the signal paths of the sum loop.

Table 6C-10. A5 Coarse Loop VCO PCA Expected DC Voltages

LOCATION	VOLTS DC
ON bias transistor collector (Q4, Q5, or Q6, depends on band)	-14.3
OFF bias transistor collectors	0
ON oscillator transistor collector (Q1, Q2 or Q3, depends on band)	+8.3
OFF oscillator transistor collectors	+9.6
U1, U2 outputs	+4.4
CR7, CR8, CR9 node	+9.9

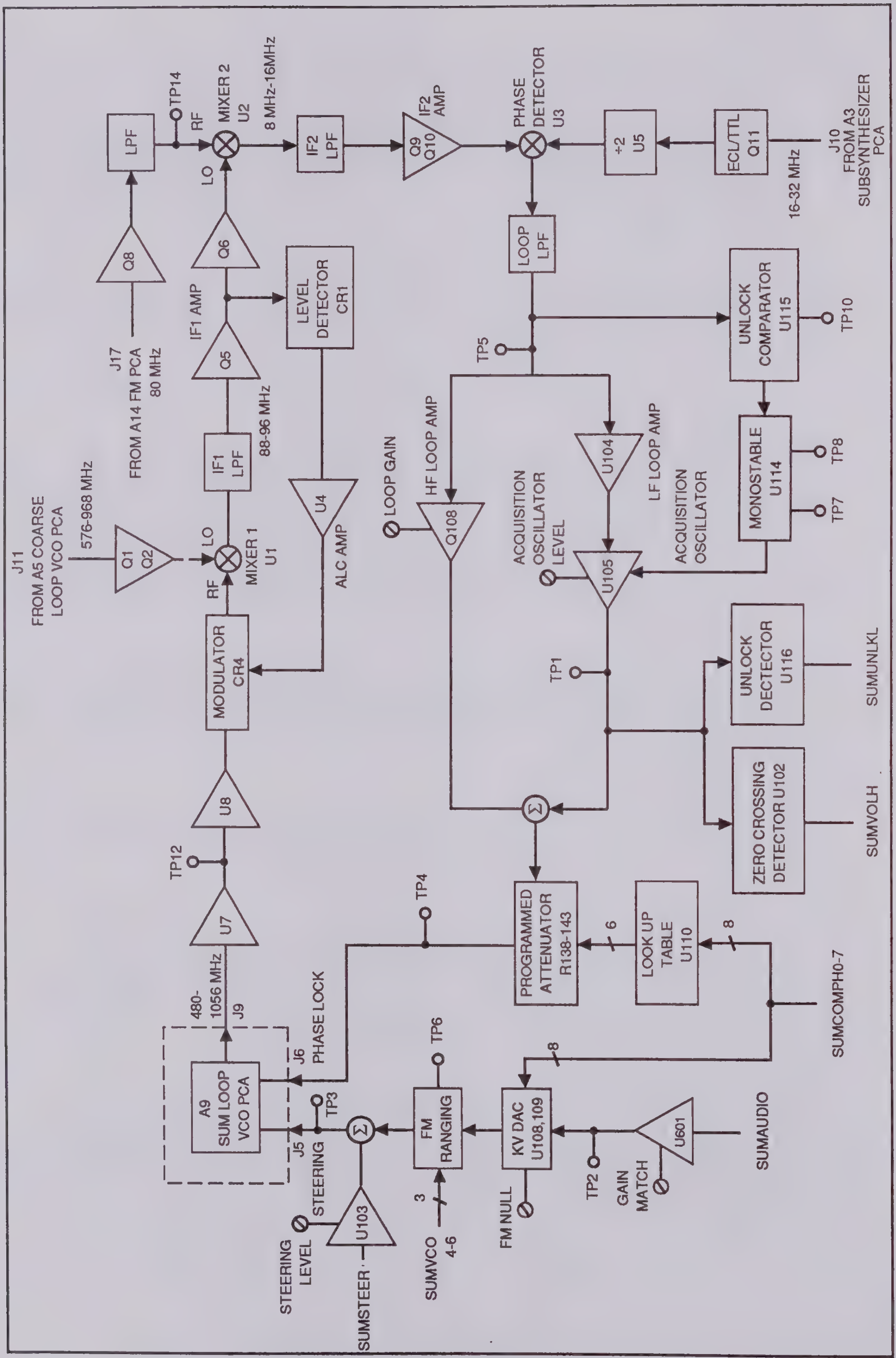

J11
FROM A5 COARSE
LOOP VCO PCA
576-968 MHz
Q1
Q2
LO
MIXER 1
U1
RF
MODULATOR
CR4
U8
TP12
U7
480-
1056 MHz
J9
A9
SUM LOOP
VCO PCA
J6
PHASE LOCK
J5
STEERING
TP3
STEERING
LEVEL
U103
SUMSTEER
FM
RANGING
TP6
3
SUMVCO
4-6
KV DAC
U108,109
FM NULL
8
TP2
GAIN
MATCH
U601
SUMAUDIO
J17
FROM A14 FM PCA
80 MHz
Q8
LPF
TP14
RF
MIXER 2
U2
8 MHz-16MHz
LO
Q6
IF1 AMP
Q5
IF1
LPF
88-96 MHz
LEVEL
DETECTOR
CR1
U4
ALC AMP
IF2
LPF
Q9
Q10
IF2
AMP
PHASE
DETECTOR
U3
÷2
U5
ECL/TTL
Q11
16-32 MHz
J10
FROM A3
SUBSYNTHESIZER
PCA
LOOP
LPF
TP5
UNLOCK
COMPARATOR
U115
TP10
LOOP GAIN
HF LOOP AMP
Q108
U104
LF LOOP AMP
ACQUISITION
OSCILLATOR
LEVEL
ACQUISITION
OSCILLATOR
U105
MONOSTABLE
U114
TP8
TP7
TP1
UNLOCK
DECTECTOR
U116
SUMUNLKL
ZERO CROSSING
DETECTOR U102
SUMVOLH
Σ
Σ
TP4
PROGRAMMED
ATTENUATOR
R138-143
6
LOOK UP
TABLE
U110
8
SUMCOMPH0-7

Figure 6C-8. Sum Loop Block Diagram

A12 SUM LOOP CIRCUIT DESCRIPTION 6C-37.

The A12 Sum Loop PCA generates the fundamental frequency band, 480 to 1056 MHz, by combining signal frequencies from the FM, the Subsynthesizer, and the Coarse Loop PCAs. The sum loop was designed for spurious Signal Generation of less than -100 dBc, and for low phase noise contribution. The relation between sum loop output frequency and the input frequencies follows.

For f(sum) <760 MHz:

f(sum) = f(coarse) - f(fm) - f(subsynth)

For f(sum) >=760 MHz:

f(sum) = f(coarse) + f(fm) + f(subsynth)

The A12 Sum Loop PCA includes a phase-locked loop (PLL) circuit that steers the frequency of the A9 Sum Loop VCO PCA to the correct value, according to the above equations. The loop includes an RF section (with two stages of heterodyne frequency downconversion), a phase detector circuit, and an audio section. The audio section contains the loop amplifier, acquisition circuits, and vco coarse steering circuits. The following paragraphs discuss these PLL sections.

The output signal from the A9 Sum Loop VCO PCA is coupled into the output section where the signal is further processed to generate the instrument RF OUTPUT signal.

RF Section 6C-38.

The RF section contains the RF amplifiers, mixers, and filters required to process the Sum Loop VCO signal through three successive stages of frequency downconversion. The first stage subtracts the coarse loop frequency from the Sum Loop VCO frequency to generate a first IF signal, referred to as the IF1 signal. The second stage subtracts the FM PCA signal from the IF1 signal to generate a second signal, IF2. The third stage includes a mixer phase detector that compares the IF2 signal to the subsynthesizer signal and generates the audio frequency phase-locked signal that is further processed in the audio section.

Frequency ranges for these signals are given in Table 6C-11. Note that when FM is on, the programmed deviation appears in the Sum Loop VCO signal, the IF1 signal, and the FM PCA signal.

Table 6C-11. Sum Loop Frequencies

SIGNAL	FREQUENCY RANGE (MHz)
Sum Loop VCO	480 to 1056
Coarse Loop	576 to 960
IF1	88 to 96
FM PCA	80
IF2	8 to 16
Subsynthesizer	8 to 16

The Sum Loop VCO signal at J9 is applied to buffer amplifiers U7 and U8. PIN diode CR4 follows U8 and acts as an adjustable attenuator to control the level at the RF port of double balanced mixer U1. A low-pass filter including C81 and C82 precedes U1 RF port and attenuates high order harmonics in the RF signal. The LO port of U1 is driven by a two-stage amplifier that includes Q1 and Q2. This amplifier accepts the +7 dBm signal from the Coarse Loop VCO at J11 and produces +20 dBm of drive power at the LO port of U1.

U1 generates the IF1 signal at the IF port. This signal is filtered by a 10-element, 100-MHz low-pass filter with input at L3 and output at C27. The filter is located within a channel in an aluminum cover piece to improve high frequency attenuation. This cover also shields the IF1 amplifiers and the IF2 low-pass filter.

The -14 dBm IF1 signal at the filter output is amplified by Q5, configured for 21-dB gain. Q5 drives level detector diode CR1 at +7 dBm. CR1, U4 and associated components form a level control loop that holds RF level constant at CR1 by adjusting modulator PIN diode CR4 bias current. This action also holds the signal level at U1 RF port to a constant value. Accurate RF port level control is necessary to control mixer intermod spurs and noise floor.

The leveled IF1 signal at CR1 is next applied to a 6-dB attenuator (R25-R27) and then to Q6, which is configured as a 20-dB amplifier. Q6 drives the LO port of double balanced mixer U2 with about +20 dBm. The 80-MHz signal from the A14 FM PCA is applied to the RF port of U2 and coupled via a capacitor at J17. Q8 and associated components buffer and low-pass filter this signal, which is then applied to U2 at a -8 dBm level.

U2 generates the IF2 signal at the IF port. This signal is filtered by a nine-element, 20-MHz low-pass filter with input at L9 and output at L23. Like the IF1 filter, this filter is located within a channel in an aluminum cover piece to improve high frequency attenuation. The -14 dBm signal at the filter output drives the IF2 amplifier, which includes Q9 and Q10 and is configured for 21-dB gain. Q10 drives the RF port of mixer U3 with +7 dBm, which is used as a phase detector. The IF2 low-pass filter also provides a dc path for +15V power for the IF2 amplifier.

The A3 Subsynthesizer PCA inputs a 16- to 32-MHz signal to J10. This ECL-level signal is converted to TTL by Q11 and related circuitry. The TTL signal then drives U5, a D-type flip-flop configured to divide the input frequency in half. The resulting 8- to 16-MHz Q and Q (compliment) outputs of U5 drive the LO port of U3.

The IF output of U3 drives the loop filter, a 13-element low-pass type with input at R56 and output at L26. This filter allows audio frequency components to pass with minimum phase shift while adequately attenuating RF mixer products. The loop filter output voltage is proportional to the phase difference between the RF and LO ports of U3. This signal drives the audio section, described in the following paragraphs.

Audio Section 6C-39.

The Audio Section contains the circuits required to acquire and maintain phase lock. Inputs to this section include the phase detector voltage, Sum Loop VCO coarse steering voltage (SUMSTEER), FM modulation signal (SUMAUDIO), FM range switching signals (SUMVCO4-6), and Sum Loop VCO Kv information (SUMCOMPH0-7). Audio Section outputs include Sum Loop VCO steering port and phase-lock port voltages, and a phase-locked status indicator for the controller.

LOOP AMPLIFIER 6C-40.

The loop amplifier consists of a low frequency path and a high frequency path connected in parallel and driven by the phase detector voltage at the loop filter output (L26). This configuration minimizes noise and phase shift at frequencies around the unity loop gain frequency of 500 kHz.

The low frequency path operates from dc to about 30 kHz, and includes op amps U104, U105, and associated components. U105 is also configured as a Wien bridge-type acquisition oscillator. When the sum loop is unlocked, U105 oscillates at either 800 Hz or 14 kHz. The oscillation depends on switching FETs Q106 and Q107, which switch capacitors C127 and C131. Potentiometer R132 sets the amplitude of oscillation. U105 stops oscillating and acts as a gain-of-3 amplifier when phase lock is obtained, due to loop dynamics.

The high frequency path operates for frequencies greater than about 30 kHz, and includes Q108 and associated components. Q108 is a low-noise, high-ft transistor configured as an emitter follower. An RC circuit sums the outputs of the two paths, with C137 and C138 providing high-pass and low-pass characteristics, respectively. R167 provides loop gain adjustment.

The summing node, at TP4, is connected to the J6 Sum Loop VCO phase-lock port, and to ground through six switchable resistors, R138-R143. These switched resistors adjust loop amplifier gain to compensate for Sum Loop VCO Kv variations. Note that Kv is the slope of the frequency vs the tuning voltage function.

The switched resistors are programmed by U110, a PROM containing a look-up table. The input to U110, SUMCOMP bits 0-7, is a binary number proportional to 1/Kv. The six-bit output of U110, functionally related to the SUMCOMP number, drives the programmed resistors to compensate for Kv variation with Sum Loop VCO RF frequency.

ACQUISITION CIRCUITS 6C-41.

The acquisition circuit includes a two-frequency acquisition oscillator, an unlock detecting comparator, a loop disabling circuit, and a dual monostable multivibrator.

When the loop is properly phase locked, the phase detector voltage at TP5 stays close to 0V, because the loop forces equal frequency and nearly equal phase for the phase detector inputs. If the loop was opened, for instance by shorting the vco phase lock port at TP4, the phase detector would generate a beat frequency triangle wave signal of about 300 mV amplitude. Thus, the presence of a voltage above a threshold level indicates loop unlock. High speed comparator U115 trips and activates a two-stage acquisition sequence when the phase detector voltage exceeds 190 mV, indicating loop unlock.

The output of U115 is applied to the 1A input of U114, a dual monostable multivibrator, and trips one-shot A upon unlock detection. One-shot A is configured for a 10-ms output pulse and drives comparators U102A and U102B, which disable the low and high frequency paths of the loop amplifier, respectively, during the 10-ms pulse. U102A turns off Q109, and U102B turns off bias current to Q108, effectively open circuiting the loop amplifier.

This disabling action of opening the loop allows time for all the frequency inputs to the Sum Loop PCA to settle to proper values following a change in instrument RF frequency, prior to sum loop phase-lock acquisition. The trailing edge of the one-shot A pulse triggers one-shot B, at the 2B input.

One-shot B is configured for a 0.5-ms pulse and drives comparator U102C, which switches acquisition oscillator U105 to the 14-kHz mode. This acquisition frequency results in optimum lock-on behavior. During the 0.5-ms pulse, unlock comparator U115 is disabled to allow acquisition to occur. If Sum Loop PCA inputs are correct, acquisition occurs during the 0.5-ms pulse, and U105 stops oscillating, due to changes in loop dynamics. After the 0.5-ms one-shot B pulse, U105 is set to the 800-Hz mode to improve closed-loop dynamics, but does not oscillate if the lock was obtained.

U102D is a zero crossing comparator that senses the polarity at TP1, the low frequency loop amplifier output, and generates the SUMVOLH signal. The controller uses this signal during the Sum Loop VCO calibration routine.

Monostable multivibrator U116 is triggered by the acquisition oscillation at U105. This occurs when the sum loop is unlocked, and generates the SUMUNLKL signal. The signal informs the controller that the sum loop is not locked.

SUM LOOP VCO STEERING CIRCUIT 6C-42.

The Sum Loop VCO has two ports for frequency tuning: the steering port at J5 and the phase-locked port at J6. A coarse tuning voltage, generated at the steering port, tunes the Sum Loop VCO frequency to the desired value, within about ±2 MHz. The phase-locked port is driven by the loop amplifier with enough voltage to compensate for any error in the steering port, and sets the Sum Loop VCO frequency to the correct phase-locked value. The following paragraphs describe the circuit that drives the steering port.

The SUMSTEER signal is generated in a 12-bit dac on the A11 Modulation Control PCA. The dac is programmed by data stored in the controller. Note that this data is obtained and stored during the Sum Loop VCO compensation procedure, and is unique to a given vco.

The SUMSTEER signal is input at J7-14. This signal, an RF frequency-dependent dc voltage, is proportional to the required steering port voltage. The signal is low-pass filtered and amplified by U103 and associated components. Resistor R112 adjusts the gain of the circuit. Depending on the RF frequency, the dc voltage at steering port TP3 varies from 0 to 26V.

The 80-MHz FM source for the Signal Generator is output by the A14 FM PCA. The Sum Loop VCO is phase locked to this 80-MHz input signal, and any frequency modulation on the signal is transferred to the Sum Loop VCO. However, at high levels of FM deviation, the required voltage swing at the vco phase-lock port would require a phase detector output greater than possible, and thus the sum loop would lose lock.

This problem is avoided by applying an ac signal at the vco steering port that provides nearly the correct deviation in the Sum Loop VCO during high deviation FM operation. Thus, the loop must generate only a small error voltage at the vco phase-lock port to maintain lock, and the phase detector output stays acceptably small.

The SUMAUDIO signal at J8-1, from the A14 FM PCA, is an ac frequency-modulating signal with amplitude proportional to FM deviation. This signal is buffered by op amp U106, which is configured for unity gain. The signal can be switched via U107 for inverting or non-inverting operation. These two modes are required to properly phase the cancellation signal, depending on fundamental frequency band. For f(fund) <760 MHz, U106 inverts, while for f(fund) >=760 MHz, U106 is non-inverting. R121 provides gain equalization for the two modes.

The buffered signal at TP2 is next applied to dac U109, which is programmed by SUMCOMP bits 0-7. These eight bits encode a number proportional to Sum Loop VCO 1/Kv. Note that Kv is the slope of the frequency vs the tuning voltage function. Thus, dac U109 scales the signal to account for vco tuning voltage sensitivity variations with RF frequency. R116 adjusts the gain for dac U109.

The dac output at U108 pin 6 is next applied to a switched RC network, which includes R105-108 and related components. The switched RC network is programmed by fm range-switching bits SUMVCO4-6 depending on FM deviation range. This network scales the signal to the appropriate level. The vco steering port TP3, outputs the desired ac cancellation signal. Noise contribution at the vco steering port is reduced by C105, which is switched to ground by Q101 when the cancellation circuit is not active.

SUM LOOP TROUBLESHOOTING 6C-43.

Since the primary function of the sum loop is to combine various signal frequencies into the desired fundamental band frequency, sum loop problems generally cause frequency errors at the UUT output. To troubleshoot, check for sum loop fault status codes 244 and 245. The implications of these errors and suggested troubleshooting sequences in response to the codes are described below. To aid in understanding these circuits, read the detailed circuit descriptions for the A12 Sum Loop and A9 Sum Loop VCO assemblies earlier in this section before you troubleshoot.

Status code 244 indicates that the sum loop is not properly phase locked, and is triggered by the free-running loop acquisition oscillator. This fault can be caused by a problem with the input signals to the sum loop, or by a problem in the A12 Sum Loop PCA or the A9 Sum Loop VCO PCA. The sum loop can be unlocked by a faulty input signal from the Coarse Loop, the Subsynthesizer, or the FM assembly.

To begin troubleshooting sum loop problems, proceed as follows:

1. Check for fault status codes that indicate incorrect operation of the Subsynthesizer PCA, the Coarse Loop PCA, and the FM PCA. Repair any indicated assemblies and recheck for Status Code 244.

2. If the code still appears, check that the three input signals listed in Table 6C-12 are the correct frequency and level. Measure the FM signal using a 500Ω probe with the spectrum analyzer. Detach the coarse loop and subsynthesizer cables from the Sum Loop PCA and connect them directly to the spectrum analyzer. Display the coarse loop and subsynthesizer frequencies by entering SPCL 946 and SPCL 947, respectively, for any UUT frequency.

Table 6C-12. Preliminary Sum Loop Troubleshooting Checks

SIGNAL DESCRIPTION	TEST LOCATION	FREQUENCY	LEVEL
Coarse Loop	Cable W14	Use SPCL 946	+7 dBm
FM	TP14	80 MHz	-13 dBm
Subsynthesizer	Cable W13	See equations below or use SPCL 947	+3 dBm
For f(sum) <760 MHz, f in MHz: f(subsynth) = 2*(f(coarse) -80 -f(sum)) For f(sum) >=760 MHz, f in MHz: f(subsynth) = 2*(f(sum) -80 -f(coarse))			

If the signals in Table 6C-12 are the correct frequency and level, first verify that the Sum Loop VCO is functional as follows:

1. Ground TP4, the phase-lock port, and measure the Sum Loop VCO signal at TP12 using a 500Ω probe with a spectrum analyzer.

2. The measured frequency should be within 2 MHz of the expected sum loop frequency. If the signal is absent or is far off frequency, either the Sum Loop VCO or the vco steering voltage circuit is faulty.

3. Check the steering voltage circuit by programming the UUT with SPCL 943. Measure the dc voltage at TP3, the vco steering port. This special function programs the steering dac to full scale and should result in a reading of 26.00V. If the Sum Loop VCO is functioning properly, troubleshoot the Sum Loop PCA.

Proceed as follows to troubleshoot the Sum Loop PCA:

1. Keep the phase-lock port TP4 shorted to ground and measure the signal at the phase detector output, TP5, with an oscilloscope.

2. This signal should be a 0.56V p-p triangle wave with a frequency of less than 2 MHz. An incorrect signal indicates a fault in the phase detector or the RF circuitry preceding it.

3. Check the RF circuits to isolate a problem by measuring signal levels and frequencies at various points with a 500Ω probe and a spectrum analyzer. Table 6C-13 lists expected frequencies and approximate levels in a suggested test sequence, and Table 6C-14 contains dc bias voltage information for circuits in the RF section. When checking signal levels, short TP4 to ground, and ground the 500Ω probe as closely as possible to each test point. The PCA hold-down screws and the walls of the plate provide good grounds.

An appropriate signal at TP5, with TP4 shorted to ground, indicates a problem in the audio section rather than in the RF circuits. To check the loop amplifier/acquisition oscillator, proceed as follows:

1. Short TP5 to ground and measure the waveform at TP1 with an oscilloscope. The waveform at TP1 should be about a 800 Hz, 14V p-p sine wave.

Table 6C-13. A12 Sum Loop PCA RF Circuitry Test Information

LOCATION	CIRCUIT	FREQUENCY	LEVEL**
J11	U1 LO amplifier	f(coarse)	-14 dBm
Q2 collector	U1 LO amplifier	f(coarse)	-1 dBm
J9	U1 RF amplifier	f(sum) +/-2 MHz	-34 dBm
TP12	U1 RF amplifier	f(sum) +/-2 MHz	-24 dBm
Q5 base	IF1 amplifier	f(IF1)*	-35 dBm
R25/R26 node	IF1 amplifier	f(IF1)*	-15 dBm
Q6 collector	IF1 amplifier	f(IF1)*	-5 dBm
R17/R45 node	FM amplifier	80 MHz	-26 dBm
TP14	FM amplifier	80 MHz	-13 dBm
Q9 base	IF2 amplifier	f(sub-syn)/2 +/-2 MHz	-37 dBm
Q10 collector	IF2 amplifier	f(sub-syn)/2 +/-2 MHz	-18 dBm
J10	ECL/TTL buffer	f(sub-synth)	-18 dBm
R57/C60 node	U3 LO driver	f(sub-synth)/2	-26 dBm
* f(IF1) = (f(sub-synth)/2 + 80) +/-2 MHz ** Levels are approximate and are measured using a 500-ohm probe with a spectrum analyzer.			

Table 6C-14. A12 Sum Loop PCA RF Section DC Bias Voltages

LOCATION	CIRCUIT	VOLTS DC
Q1 collector	U1 LO amplifier	+9.8
Q2 collector	U1 LO amplifier	+4.9
U7 output	U1 RF amplifier	+4.7
U8 output	U1 RF amplifier	+4.7
Q5 collector	IF1 amplifier	+9.5
Q6 collector	IF1 amplifier	+3.5
Q8 collector	FM amplifier	+9.8
Q9 collector	IF2 amplifier	+6.4
Q10 collector	IF2 amplifier	+8.5
Q11 collector	ECL/TTL buffer	+1.0

2. With both TP5 and TP8 shorted to ground, measure the TP1 waveform for an approximate 13.6 kHz, 8V p-p sine wave. Failure of this test indicates a problem somewhere between TP5 and TP1.

To check the programmable attenuator for proper operation, proceed as follows:

1. Connect TP7 and TP9 to ground.

2. Program the UUT to SPCL 943 (dac's set to full scale), and measure the resistance from TP4 to ground for a reading of about 240Ω.

3. Program the UUT to SPCL 941 (dac's set to zero) for a resistance reading of about 29.5Ω. Failure of this test indicates a problem somewhere between TP1 and TP4.

Status Code 245 indicates an unleveled condition in the leveling loop that controls the signal amplitude at the RF input of mixer U1. A fault code displays when the modulator control voltage at J16 exceeds about 10V. This fault condition can be caused by either a level problem in the RF path (including the Sum Loop VCO and sum loop circuits between J9 and CR1), or by improper signal frequencies within the sum loop.

Table 6C-15 presents the nominal characteristics of the signals at the various test points on the A12 Sum Loop PCA. This table lists the normal range of the signals, along with specific values for the instrument diagnostic state.

Table 6C-15. A12 Sum Loop PCA Test Points

TEST POINT	SIGNAL TYPE	RANGE	TYPICAL FOR SPCL 909	SIGNAL DESCRIPTION
TP1	dc+audio	+/-4V	0V	Loop amp low frequency output
TP2	audio	0 to 3.0V rms	0V	SUMAUDIO buffer amplifier output
TP3	dc+audio	0 to 26.0V	15V	Sum Loop VCO steering voltage
TP4	dc+audio	+/-.8V	0V	Sum Loop VCO phase lock voltage
TP5	dc+audio	+/-150 mV	0V	Phase detector voltage
TP6	N/A	This test point is an input for sum loop test and alignment.		
TP7	TTL	TTL high, low	TTL high	Loop disabling one-shot output signal
TP8	TTL	TTL high, low	TTL high	Acquisition oscillator switching signal
TP9	dc+audio	+/-4V	0V	Filtered loop amp LF output
TP10	N/A	This test point is shorted to ground for sum loop test and alignment.		
TP11	N/A	This test point is shorted to ground for sum loop test and alignment.		
TP12	RF*	-20 to -28 dBm 480-1056 MHz	-24 dBm 600 MHz	Buffered Sum Loop VCO signal
TP14	RF*	-13 dBm 80 MHz	-13 dBm 80 MHz	Buffered FM oscillator signal
TP15	ground	n/a		
* RF Levels are approximate and are measured using a 500Ω probe with a spectrum analyzer.				

SUM LOOP ASSEMBLY ADJUSTMENTS 6C-44.

The following procedures cover the five potentiometer adjustments on the A12 Sum Loop PCA listed below:

- R112, Steering level adjustment
- R121, Buffer gain match adjustment
- R116, FM null adjustment
- R167, Loop gain adjustment
- R132, Acquisition oscillator level adjustment

NOTE

These adjustments are not routine and are required only when you replace the associated components or when you change the adjustment.

Steering Level Adjustment, R112 6C-45.

TEST EQUIPMENT:

- DVM

REMARKS:

The Steering Level Adjustment is normally required only when U103 or any associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

Adjust the Sum Loop VCO steering voltage to +26V dc with the Sum Loop VCO steering dac set to full scale.

1. Program the UUT to SPCL 909.

2. Program the UUT to SPCL 943 to program all dac's to full scale.

3. Connect the dvm to measure the voltage between TP3 and TP15 (ground).

4. Adjust R112 for +26.00V ±.02V.

5. Program the UUT for SPCL 00. This clears all Special Functions.

Buffer Gain Match Adjustment, R121 6C-46.

TEST EQUIPMENT:

- DVM

REMARKS:

The buffer gain match adjustment is normally required only when U106 or any associated components have been replaced or when the adjustment has shifted.

PROCEDURE:

Adjust the SUMAUDIO buffer amplifier for equal gain in the inverting and non-inverting modes.

1. Program the UUT to SPCL 909, 800 MHz, 4 MHz FM deviation, and 1 kHz mod frequency. Turn INT FM on.
2. Connect the dvm to measure the ac voltage between TP2 and TP15 (ground).
3. Note the dvm reading.
4. Program the UUT to 700 MHz.
5. Adjust R121 for a dvm reading equal to that noted in step 3, ±5 mV.

FM Null Adjustment, R116 6C-47.

TEST EQUIPMENT:

- Oscilloscope

REMARKS:

Perform the FM null adjustment under the following conditions:

- If the A12 Sum Loop PCA has been replaced or the A14 FM PCA has been replaced or repaired.
- If U108, U109, or any associated components have been replaced or the adjustment has been changed or has shifted.

PROCEDURE:

With the UUT programmed for INT FM on, and 4-MHz FM deviation at 168-kHz mod frequency, adjust the ac error voltage at TP5 (the phase-detector output), for a minimum peak-to-peak value.

1. Program the UUT to SPCL 909, 700 MHz, 4-MHz deviation, and 168-kHz mod frequency. Turn INT FM on.
2. Set the oscilloscope for 50 mV/division vertical, 2 μs/division horizontal, and ac coupling.
3. Connect the oscilloscope probe to monitor the signal at TP5, using TP15 for the ground connection.
4. Adjust R116 for a minimum peak-to-peak voltage. The waveform should be less than 150 mV p-p.

Loop Gain Adjustment, R167 6C-48.

TEST EQUIPMENT:

- High-frequency synthesized signal generator (HFSSG)
- Wideband ac voltmeter (WBVM)

REMARKS:

- The Loop Gain Adjustment is normally required only when U3, Q108, or any associated components are replaced or when the adjustment has shifted.
- The upper plate cover of the lower module must be installed prior to this adjustment.

PROCEDURE:

An 800-kHz signal is applied to the Sum Loop VCO steering port through TP6. Then adjust the loop gain via R167 until the ac voltages at the Sum Loop VCO steering and phase lock ports are equal.

1. Access R167, TP3, TP4, and TP6 by removing the appropriate plate cover access plugs.
2. Program the UUT to SPCL 909, 548 MHz, 150-kHz FM deviation. Turn EXT AC FM on.
3. Program the HFSSG to 800 kHz, -21.0 dBm.
4. Connect the HFSSG output to TP6 via a BNC to clip lead adapter. Connect the ground clip to the plate cover adjacent to TP6.
5. Connect the WBVM to measure the ac voltage between TP3 and the plate cover adjacent to TP3 (ground).
6. Program the WBVM for dB relative. The reading should be 0 dB.
7. Connect the WBVM to measure the ac voltage between TP4 and the plate cover.
8. Adjust R167 for an indication of 0.0 dB ±.1 dB.
9. Replace the access plugs.

Acquisition Oscillator Level Adjustment, R132 6C-49.

TEST EQUIPMENT:

- DVM

REMARKS:

The acquisition oscillator level adjustment is normally required only when U105 or any associated components are replaced or when the adjustment has been changed or has shifted.

PROCEDURE:

Adjust the acquisition oscillator level at TP1 for 2.82V rms with the phase-locked loop disabled.

1. Connect TP5 to TP15 with a clip lead. Connect TP8 to TP15 with a clip lead.
2. Connect the dvm to measure the ac voltage between TP1 and TP15 (ground).
3. Adjust R132 for an indication of 2.83V rms ±.05V.

A9 SUM LOOP VCO CIRCUIT DESCRIPTION 6C-50.

The A9 Sum Loop VCO PCA produces the fundamental band signal that when further processed in the Output Section, becomes the Signal Generator output. The A12 Sum Loop PCA controls this assembly, which includes four varactor-tuned oscillator circuits that cover the frequency range 480 MHz to 1056 MHz. They are programmed by binary control signals SUMVCO0H and SUMVCO1H as shown in Table 6C-16.

Table 6C-16. Sum Loop VCO Binary Control Signals

BAND	FREQUENCY RANGE (MHz)	SUMVCO0H	SUMVCO1H
1	480 to 624.999999	0	1
2	625 to 759.999999	0	0
3	760 to 894.999999	1	0
4	895 to 1056	1	1

The four oscillator circuits are designed similarly but have different element values and printed transmission line lengths to cover the four bands. Because the four circuits operate the same, the following discussion specifies only the reference designators for the band 1 oscillator. Refer to the A9 Sum Loop VCO PCA schematic in Section 9 to locate corresponding elements for the other three oscillators. (The components for each band are identified on the schematic.)

The band 1 oscillator uses common-base transistor Q4 configured for negative resistance at the emitter. The emitter is coupled to a resonator that consists of a printed transmission line in series with varactor diodes CR7 and CR8 and low loss porcelain capacitors C7 and C8. Two tuning voltage lines connect to the varactor cathodes and anodes via RF chokes L8 and L4, respectively. The cathode lines connect to the vco steering port, J5. The anode lines connect to the vco phase lock port, J6. These ports are used by the A12 Sum Loop PCA to control the operating frequency. The voltage across the varactors, measured between J6 and J5, varies approximately linearly with frequency in each band from about +2V to +20V.

The +13 dBm nominal signal at the oscillator transistor collector is applied to an 8-dB attenuator that provides isolation (R18-R20), and then to a low-pass filter that attenuates harmonics to less than -20 dBc (C51, C52, and printed lines). PIN diode CR12 has low RF resistance and passes the oscillator signal when the oscillator is on, and goes to a high impedance when the oscillator is off.

Band control signals SUMVCO0H and SUMVCO1H are decoded by U5 and Q5 through Q10. This circuit applies bias current only to the selected oscillator transistor. Thus, only one oscillator is activated per band.

PIN diodes CR9 through CR12 connect the active oscillator to a resistive signal splitter consisting of R22, R23, and R50. The first signal splitter output goes to series-connected monolithic 11-dB amplifiers U1 and U2. A -12 dB pad (R26-R28) is located between U1 and U2. Two amplifiers are required for adequate isolation between the Sum Loop and the Premodulator assemblies. The output of U2, at about +7 dBm, is connected to the A10 Premodulator PCA by a plug-in capacitor at J7.

The second signal splitter output goes to an identically configured circuit including amplifiers U3 and U4. Following U4 is a low-pass filter including C69 and C70 that attenuates high frequency harmonics. The filtered output from U4 is connected to the A12 Sum Loop PCA at P1 by a through-the-plate composition resistor. This component behaves as a distributed RC low-pass filter at very high frequencies, and improves sum loop spurious performance.

SUM LOOP VCO TROUBLESHOOTING 6C-51.

The Sum Loop VCO PCA, along with the A12 Sum Loop PCA, generates the fundamental frequency band. A failure of the Sum Loop VCO can cause Sum Loop Unlock status code 244, or Sum Loop Unlevel status code 245 to appear. A failure of the Sum Loop VCO can trigger self-test error codes 327 through 333. To determine whether the Sum Loop VCO or another assembly has failed, perform the following tests.

1. Ground the phase lock port of the vco with a clip lead (J6, Sum Loop VCO or TP4, Sum Loop).

2. Measure the dc voltage at J5 with the Signal Generator programmed to SPCL 943 (all dac's to full scale). The reading should be +26.00V.

3. Program the UUT to SPCL 942 (all dac's to half scale). The reading should be +13.00V. This tests the vco steering voltage circuit.

4. With J6 still grounded, examine the generator output with a spectrum analyzer while stepping the frequency from 512 to 1056 MHz. The frequency must be within about 2 MHz of programmed frequency.

Bypass the output section by examining the signal at vco output J7 with a 500Ω probe (ground the probe nearby). The level should be about -14 dBm. If the signal is correct, the problem is likely in another PCA. If the signal is incorrect over a frequency band corresponding to one of the vco bands, troubleshoot the associated vco circuit.

The dc voltages can be measured at various circuit nodes with the UUT programmed to frequencies corresponding to the four vco bands. Enable each of the four bands with UUT frequencies of 600 MHz, 700 MHz, 800 MHz, and 900 MHz. Table 6C-17 lists the voltage levels of the Sum Loop PCA.

Table 6C-17. A9 Sum Loop VCO PCA Expected DC Voltages

LOCATION	VOLTS DC
ON bias transistor collector (Q5, Q6, Q7 or Q8, depends on band)	-14.4
OFF bias transistor collectors	0
ON oscillator transistor collector (Q1, Q2, Q3 or Q5, depends on band)	7.8
OFF oscillator transistor collectors	9.4
U1,2,3,4 outputs	4.5
CR9, CR10, CR11, CR12 node	9.7

SUM LOOP VCO ASSEMBLY ADJUSTMENT 6C-52.

The following procedure covers the R23 amplifier gain adjustment on the A9 Sum Loop VCO PCA.

NOTE

This adjustment is not routine and is required only when you replace the associated components, when you change an adjustment, or when either the A12 Sum Loop PCA or the A9 Sum Loop VCO PCA is replaced.

TEST EQUIPMENT:

DVM

REMARKS:

The R23 Amplifier Gain Adjustment should be performed when the following components are replaced:

- A9 Sum Loop VCO: U3, U4, Q1, Q2, Q3, Q4
- A12 Sum Loop PCA: U7, U8, CR4, U1

PROCEDURE:

Adjust the sum loop modulator voltage to 3.0V dc maximum over the Sum Loop VCO frequency range.

1. Program the UUT to RCL 98, 720 MHz.
2. Connect the DVM to measure the dc voltage between J12 on the A10 Premodulator PCA and ground.
3. Adjust R23 for 3.00V ±0.10V.
4. Step the UUT frequency from 520 MHz to 1050 MHz in 10 MHz steps. Note the frequency where the voltage is greatest. Program the UUT to this frequency.
5. Adjust R23 for 3.00V ±0.10V.
6. Step the UUT frequency from 520 MHz to 1050 MHz in 10 MHz steps. Verify that the voltage is between 1.00V and 3.10V for each frequency.

Section 6D

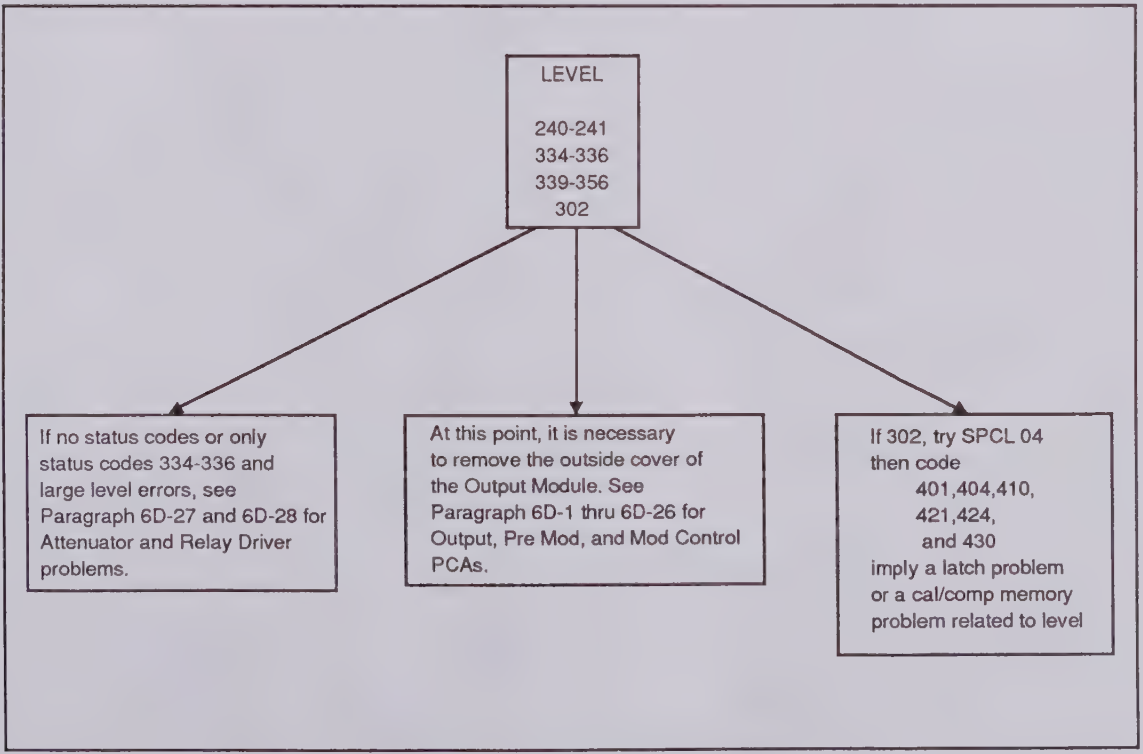
RF Level/AM

RF LEVEL FAULT TREE 6D-1.

Refer to the RF Level Fault Tree (Figure 6D-1) when troubleshooting RF level and AM problems.

RF LEVEL BLOCK DIAGRAMS 6D-2.

Figure 6D-2 is a block diagram of the A8 Output and A11 Modulation Control assemblies. Figure 6D-3 is a block diagram of the A10 Premodulator assembly. Refer to these block diagrams to identify the major functional sections and to follow the signal paths for the next discussion.



If no status codes or only status codes 334-336 and large level errors, see Paragraph 6D-27 and 6D-28 for Attenuator and Relay Driver problems.

At this point, it is necessary to remove the outside cover of the Output Module. See Paragraph 6D-1 thru 6D-26 for Output, Pre Mod, and Mod Control PCAs.

If 302, try SPCL 04 then code 401,404,410, 421,424, and 430 imply a latch problem or a cal/comp memory problem related to level

Figure 6D-1. RF Level Fault Tree

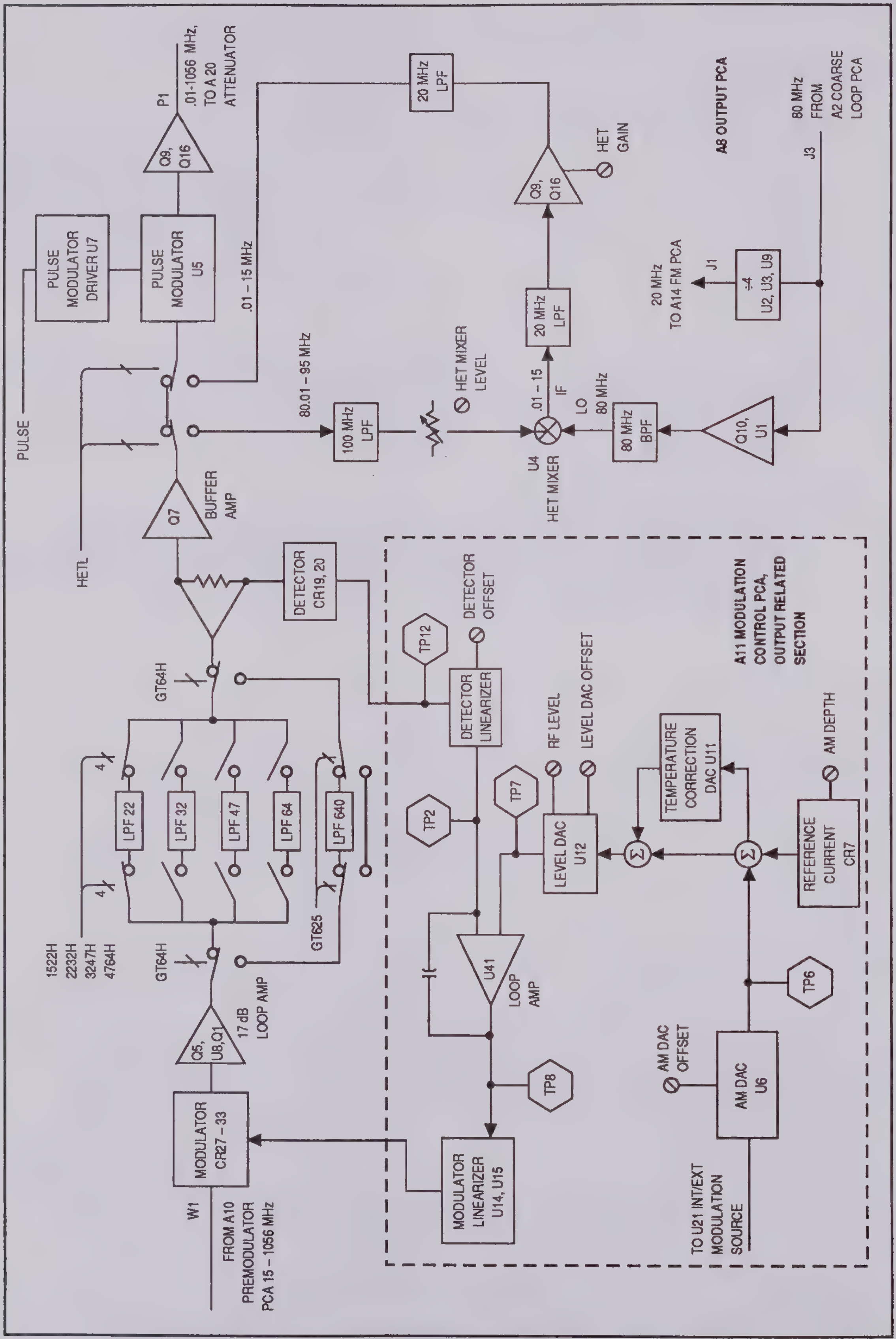

PULSE
PULSE MODULATOR DRIVER U7
PULSE MODULATOR U5
Q9, Q16
P1
.01-1056 MHz, TO A20 ATTENUATOR
20 MHz LPF
.01 – 15 MHz
HETL
Q7
BUFFER AMP
80.01 – 95 MHz
100 MHz LPF
HET MIXER LEVEL
.01 – 15
IF
LO
80 MHz
U4
HET MIXER
20 MHz LPF
Q9, Q16
HET GAIN
80 MHz BPF
Q10, U1
J3
80 MHz FROM A2 COARSE LOOP PCA
A8 OUTPUT PCA
÷4 U2, U3, U9
J1
20 MHz TO A14 FM PCA
DETECTOR CR19, 20
TP12
DETECTOR OFFSET
DETECTOR LINEARIZER
GT64H
GT64H
1522H
2232H
3247H
4764H
4
4
LPF 22
LPF 32
LPF 47
LPF 64
LPF 640
GT625
TP2
TP7
RF LEVEL
LEVEL DAC OFFSET
LEVEL DAC U12
Σ
Σ
TEMPERATURE CORRECTION DAC U11
REFERENCE CURRENT CR7
AM DEPTH
A11 MODULATION CONTROL PCA, OUTPUT RELATED SECTION
Q5, U8,Q1
17 dB LOOP AMP
U41
LOOP AMP
TP8
TP6
AM DAC OFFSET
AM DAC U6
MODULATOR CR27 – 33
W1
FROM A10 PREMODULATOR PCA 15 – 1056 MHz
MODULATOR LINEARIZER U14, U15
TO U21 INT/EXT MODULATION SOURCE

Figure 6D-2. A8 Output and A11 Modulation Control Block Diagram

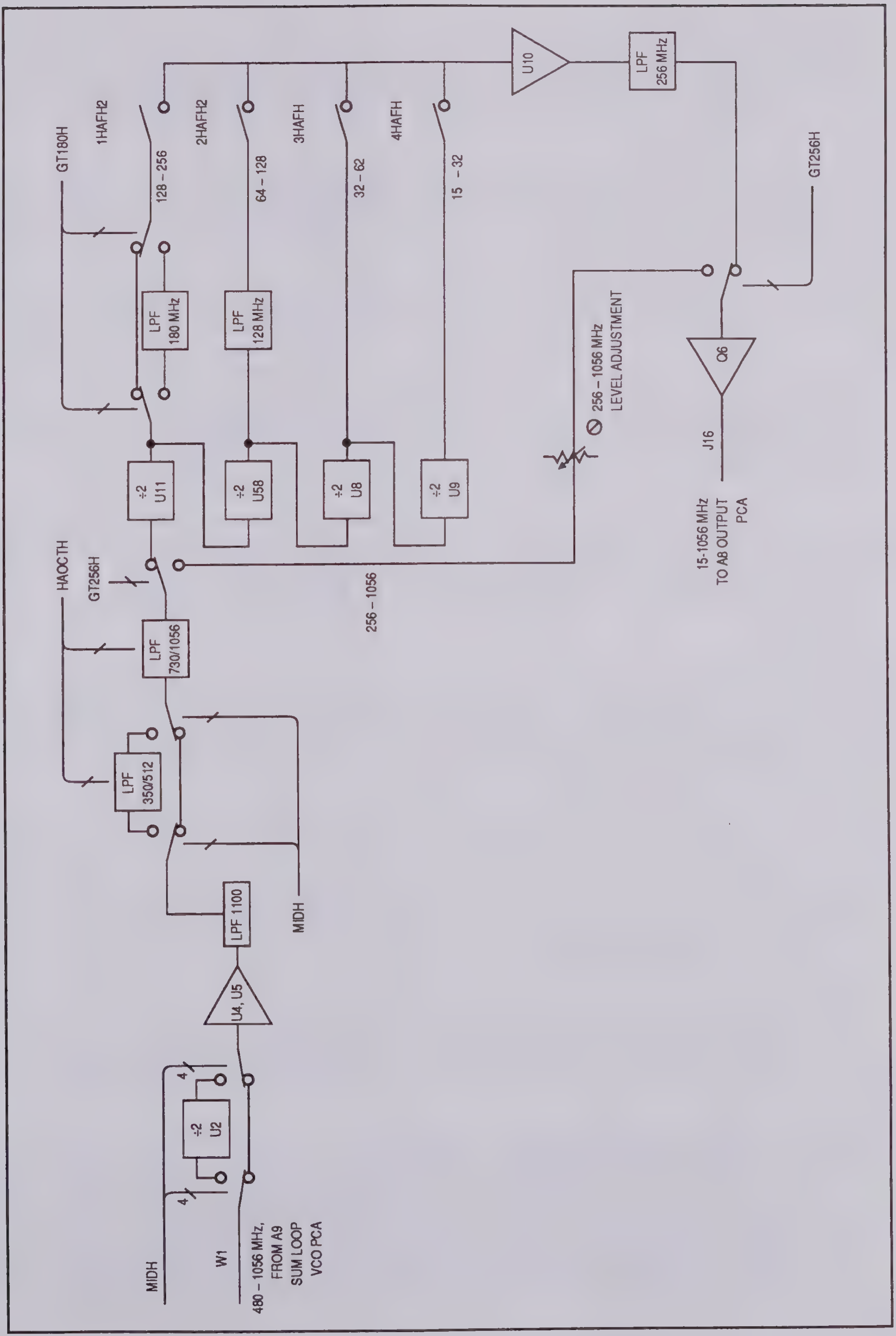

GT180H
1HAFH2
128 - 256
2HAFH2
64 - 128
3HAFH
32 - 62
4HAFH
15 - 32
U10
LPF 256 MHz
GT256H
LPF 180 MHz
LPF 128 MHz
256 – 1056 MHz LEVEL ADJUSTMENT
Q6
J16
÷2 U11
÷2 U58
÷2 U8
÷2 U9
15-1056 MHz TO A8 OUTPUT PCA
HAOCTH
GT256H
256 – 1056
LPF 730/1056
LPF 350/512
LPF 1100
MIDH
U4, U5
÷2 U2
4
4
MIDH
W1
480 – 1056 MHz, FROM A9 SUM LOOP VCO PCA

Figure 6D-3. A10 Premodulator PCA Block Diagram

RF LEVEL CIRCUIT DESCRIPTION 6D-3.

The Output Assembly consists of the circuits on the A11 Modulation Control PCA, the A10 Premodulator PCA, and the A8 Output PCA. They are interrelated and are described in this section as a unit.

The A11 Modulation Control PCA distributes dc power and control signals to the Output PCA, the Premodulator PCA, the FM PCA, and the Sum Loop PCA. It also controls and distributes internal and external modulation signals for AM, FM, ϕM, and pulse modulation.

The A10 Premodulator PCA receives a 480- to 1056-MHz RF signal from the A9 Sum Loop VCO. The Premodulator PCA uses divide-by-two circuits and switches to develop a 15- to 1056-MHz RF signal. This signal is applied to the Output PCA.

The A8 Output PCA contains the level/am modulator and the pulse modulator circuits. It generates a detected voltage for the leveling loop, develops the 0.01- to 14.999999-MHz het band signal, and provides the final amplification of the 0.01- to 1056-MHz output signal.

The A20 Attenuator/RPP Assembly receives a 0.01- to 1056-MHz RF signal from the Output Assembly. Refer to "Attenuator/Reverse Power Protection (RPP)" in Section 6D for details about the A20 assembly. The Attenuator/RPP provides 0 to 138-dB of attenuation in 6-dB steps and provides protection for the output circuits.

RF Path 6D-4.

The A9 Sum Loop VCO PCA inputs a 480- to 1056-MHz signal to J5 on the A10 Premodulator PCA. The logic signal (MIDH) controls a circuit that includes CR1 through CR 4, which acts as a double-pole, double-throw (dpdt) switch. The diode circuitry switches the RF signal directly to amplifier U4, or through divide-by-two circuit U2, and then to U4.

Both RF signal paths use frequency-shaping networks to flatten the frequency response. The input frequency to U4 is 240 to 1056 MHz. The signal is then further amplified by U5. The output of U5 is first low-pass filtered at 1100 MHz, then filtered again by the switched filter that is controlled by logic signals HAOCTH and MIDH. This filter removes harmonics with low-pass filters switched at 350 MHz, 512 MHz, and 730 MHz. The particular filter in place depends on the logic state of HAOCTH and MIDH, which control CR9-CR19.

The 240- to 1056-MHz signal goes to the circuitry that includes CR22, CR23, CR31, and CR32, which act as a DPDT switch. The switch circuitry is controlled by logic signal GT256H. This DPDT switch directs the RF signal to amplifier Q6, or to the divider chain beginning with U11.

From this point, the output of U11 splits: one output provides 128- to 256-MHz to a switched filter for reducing harmonics, and a second output provides an input signal to the third divider, U58. The 128- to 256-MHz output passes through a low-pass filter (selected by logic signal GT180H) for frequencies below 180 MHz. Frequencies greater than 180 MHz are filtered by the 260 MHz low-pass filter between U10 and CR31. When a frequency in this band is selected, logic signal 1HAFH2 is high, which turns on CR71. The signal is level-adjusted by the network between CR25, CR27, and CR71.

U58 has two outputs. One output provides 64 to 128 MHz to an output filter consisting of T2 and the low pass filter following it. The second output provides these same frequencies to the fourth divider, U8. U58 is activated when D1HAFL is high, which provides dc bias, and when D2HAFH is low, which activates the divider.

U8 provides a 32- to 64-MHz output. U8 and its output are selected by logic signals D3HAF and 3HAFH. The fifth divider, U9, generates 15 to 32 MHz. U9 and its output are selected by logic signals D4HAFL and 4HAFH. Low-pass filters on the A8 Output PCA following the modulator filter the 15- to 64-MHz range for harmonic suppression. Diodes CR71, CR28, CR29, or CR30 select the appropriate band, then U10 amplifies it. When a frequency from 15 to 256 MHz is selected, it passes through CR31 to amplifier Q6. Q6 provides 6 dB of gain and buffering for the 15- to 1056-MHz signal input to the Output PCA at J16.

The amplitude modulator on the Output PCA consists of PIN diodes CR27 through CR33 and associated components. The modulator receives the 15- to 1056-MHz signal from the Premodulator PCA through W1. The modulator is a voltage-controlled variable attenuator that provides AM and output level control. Modulator control voltage is determined by the leveling-loop circuitry, which is described later in this section.

Q5, U8, Q1, and associated components follow the modulator in the signal path and form a three-stage, 17-dB gain, 15- to 1056-MHz amplifier. This gain stage is followed by a 4-band switched filter to remove harmonics in the 15- to 27-MHz, 27- to 32-MHz, 32- to 47-MHz, and 47- to 64-MHz frequency bands.

Circuitry turns on CR4 to direct signals below 64 MHz to the filter bank. The appropriate filter is selected by CR6-CR13, and the result is returned to the signal path by CR16. Signals above 64 MHz proceed to this point via a high frequency, switched filter consisting of CR14, CR15, C38, C39, and circuit traces. This filter passes frequencies below 625 MHz to further reduce harmonics. The 64- to 1056-MHz signal is recombined with the 15- to 64-MHz signal at C180. This signal then drives a 3-dB power splitter that consists of resistors R63, R30, R31, and R32 and the associated transmission lines.

One power-splitter output drives the leveling loop detector diode CR20. The other output goes to a 5.5-dB pad followed by a 7 dB amplifier, Q7 and associated components. The het band switch follows the buffer amp and consists of PIN diodes CR18, CR21-CR24 and biasing components. In the 15- to 1056-MHz position, the signal passes through diodes CR21-CR24 to the pulse modulator, U5. A buffer amplifier consisting of Q9 and associated circuitry, follows the pulse modulator and provides 8.5 dB of gain. This amplifier is then followed by the 6-dB final amplifier, which is composed of Q16 and associated components. The final amplifier provides at least +20 dBm output at low distortion.

For het band operation (0.01 to 15 MHz), the signal from the power splitter is routed through CR18 to the het band circuitry. The RF signal passes through a 95 MHz low-pass filter, then an adjustable attenuator (R70 through R75), and then to the RF port of a doubly-balanced mixer. The signal frequency at the mixer RF port varies from 80.01 to 95 MHz. The 80 MHz local oscillator (LO) signal for the mixer comes from the A2 Coarse Loop PCA through J3 and is amplified by U1. This signal is then amplified by class C amplifier Q10, which is followed by a band-pass filter and 3 dB pad to provide +18 dBm at the mixer LO port.

The mixer 0.01- to 15-MHz output signal passes through a diplexing low-pass filter (C99 through C104, and R76) that suppresses unwanted mixer spurious products while maintaining a 50Ω load at the mixer IF port. A two-stage IF amplifier Q13, Q14, and associated components amplifies the filtered IF signal by a (nominal) gain of 20 dB. The signal is filtered to remove remaining LO and RF signals before being recombined at CR24 with the main signal path. Q3 switches off the +5V power supply for the LO amplifier to prevent spurious signals from being introduced when the instrument operates in the 15- to 1056-MHz bands.

Leveling Loop 6D-5.

The leveling loop controls the 15- to 1056-MHz signal level at detector diode CR20 and buffer amplifier Q7 on the A8 Output PCA. The leveled RF signal is proportional to the leveling-loop control voltage that appears at TP7 on the A11 Modulation Control PCA.

Schottky detector diode CR20 generates a temperature-dependent dc voltage. This is a non-linear function of the applied RF voltage, thus temperature compensation and linearization are necessary. The detector diode signal is low-pass filtered by L34 and C34 and is offset by the voltage across temperature-compensating diode CR19. A current source circuit formed by Q1, Q2, and associated components on the Modulation Control PCA provides bias current for CR20 and CR19.

The offset detector diode voltage at U7 pin 3 on the Modulation Control PCA is linearized by amplifier U7 and its associated feedback components. Potentiometer R28 provides an adjustment for best detector linearity at low RF levels. Thus, the voltage at U7 pin 6 (TP2) is proportional to the RF signal level at detector diode CR20 (Output PCA).

The voltage is then applied to U41 pin 2, the loop-integrator/summing amplifier. The leveling-loop control voltage (plus any AM) is applied to U41 pin 3. U41 drives the leveling/am modulator through U14 and U15 and circuits that compensate for modulator non-linearity. An additional linearizing network consisting of R35, R36, CR5, and CR6 acts on the control signal. Amplitude modulation is achieved by summing an appropriately scaled modulation signal with the dc leveling loop control voltage.

The amplitude modulator on the Output PCA consists of PIN diodes CR27 through CR33 and associated components. The bias current through these PIN diodes attenuates the output. This current is provided by the modulator-linearizer circuit on the Modulation Control PCA. U14 and associated components provide modulator series diode current, while U15 and associated components provide shunt diode current.

Modulator attenuation is approximately proportional to the modulator control voltage on TP8. Proportionality is required to maintain constant leveling-loop bandwidth as modulator attenuation varies. Minimum attenuation is obtained with a modulator control voltage of 10V, while maximum attenuation is obtained with 0V.

Comparator U10 and associated components form an unleveled indicator circuit. The comparator senses the modulator control voltage at TP8. This voltage is normally less than +11V, and the comparator output is high. If the modulator control voltage exceeds +11V, the modulator attenuation is at a minimum, and the leveling loop becomes inoperative (unleveled). This condition could be due to a fault or some abnormal operation such as overmodulation. In this case, the comparator output (UNLVLL) goes low. The Controller PCA senses this low and causes the front panel STATUS indicator to flash and displays unleveled status code 241 if interrogated.

Level Control 6D-6.

The level-control circuit sets the instrument output level. This audio signal processing circuit receives inputs from the internal and external modulation signals, a dc reference voltage, and the digital control commands. The circuit outputs the leveling-loop control voltage that provides vernier level control and amplitude modulation control of the Signal Generator output. The A11 Controller PCA provides digitally encoded level, modulation depth, and temperature-compensation information.

External AM signals are cabled to J13, pin 1 on the Modulation Control PCA. This point is monitored by an ac peak-detecting voltmeter composed of comparator U16 and U17 and associated components. A similar circuit monitors external FM signals. Both circuits share a common reference circuit, R70 through R74 and CR12. These components provide voltages of 1.02 at U16 pin 8 and 0.98V at U16 pin 10. When these voltages are exceeded, these comparators trip and trigger monostable multivibrators U17A and U17B to provide indication to the controller that the peak ac voltage is not 1V.

Analog switch U5 selects the internal or external dc- or ac-coupled modulating signal, or selects no modulation. The selected signal is buffered by U21 and is applied to U6 pin 19, a multiplying 12-bit dac. U6, with amplifier U8A, acts as a digitally programmed variable attenuator that controls AM depth. Op amp U8B sums the AM signal (at TP6) with a dc-reference current provided by CR7. The output at U8B pin 8 is the 1+AM signal. This signal, with additional scaling, is the basis for level and AM depth. AM depth adjustment is provided by potentiometer R10, and AM dac offset is provided by R8.

The instrument RF output amplitude is temperature compensated in a manner. The 1+AM signal is applied to the reference input of U11, an 8-bit multiplying dac, and to one input of summing op amp U8D. The dac output, at U8C pin 1, is the 1+AM signal scaled by a factor that is generated from stored constants. This voltage is applied to a resistor/thermistor network that includes R15, R16, R18, and RT17. This signal, the temperature-compensated 1+AM signal, is output on U8D pin 14.

This 1+AM signal is applied to the reference input of level dac U12. This 14-bit multiplying dac, with op amp U4, generates the leveling-loop control voltage (at TP7). The leveling-loop control voltage is the temperature compensated 1+AM signal multiplied by a factor proportional to the 14-bit level control number provided by the Controller PCA. The Signal Generator RF output level adjustment is provided by potentiometer R20, and dac offset voltage adjustment is provided by potentiometer R23.

RF LEVEL TROUBLESHOOTING 6D-7.

If the Signal Generator level is inaccurate or if an unleveled condition exists, the Output assembly (A8, A10, and A11), or the A20 Attenuator/RPP Assembly is probably at fault. If an unleveled condition exists, check the RF circuitry prior to the detector, the detector circuitry, or the dc part of the leveling-loop circuitry. Refer to the heading "Unleveled Condition" later in this section.

If there is no unleveled condition, the problem is likely in the circuitry following the detector. This circuitry includes the buffer amp Q7, the heterodyne circuit, the pulse modulator, the output amplifiers Q9 and Q16, and the A20 Attenuator/RPP Assembly. If the level problem exists only below 15 MHz, troubleshoot the heterodyne circuitry. If the level problem exists only in a specific frequency band, check premodulator operation and switched filter operation controlling that band as shown in Table 6D-1. If the problem is not frequency dependent and if the level is accurate above +7 dBm but inaccurate below +7 dBm, check the Attenuator/RPP Assembly.

If the level problem is not in a particular frequency band, troubleshoot at a low frequency where an oscilloscope is useful. Select SPCL 01 to place the instrument into a known state, set the frequency to 88 MHz, and the amplitude to +13 dBm. Verify the voltage at TP8 on the Modulation Control PCA is +1.3 ±0.5V dc. If this voltage is correct, the problem is localized to the Output PCA following the detector diode CR20 or the Attenuator/RPP assembly. The appropriate signal levels following this point are:

- R121, 0.9V p-p
- Q7 base, 0.4V p-p
- Q7 collector, 0.85V p-p
- CR23 cathode, 0.82V p-p at 88 MHz
- Q9 base, 0.6V p-p
- Q9 collector, 1.5V p-p
- Q16 collector, 3.0V p-p

These voltages are approximate and are as measured with a 10-MΩ, 8-pF oscilloscope probe using a ground connection with less than 1 inch of lead length. Make the ground connection at the probe tip.

Unleveled Condition 6D-8.

If the problem exists in a specific frequency band (or bands) and other bands work properly, check band control signals and band switches. See Table 6D-1 for band control signal state definitions and Table 6D-2 to determine PIN diode states for various frequency bands. A specific band (or bands) problem will most likely involve a divider, a switch, a filter, or a control signal.

If all of the frequency bands are affected, the leveling loop or associated controls and inputs are probably at fault. First, check the signal at the output connector (J16) of the Premodulator PCA. As the instrument frequency is incremented from 15 to 1056 MHz, verify that a corresponding signal is present at J16. The levels typically range from +6 dBm at 15 MHz, and to +4 dBm at 1056 MHz with a low of about 2.5 dBm at 256 MHz. High harmonic levels will be seen in the frequencies below 64 MHz. Lack of a proper signal here might involve U4, U5, or Q6 on the Premodulator PCA. Also check the input signal to the Premodulator PCA (at J5) from the Sum Loop VCO (A9). These levels should be approximately +7 dBm.

Table 6D-1. Band, Filter, and Frequency Programming Logic Signals

FREQUENCY (MHz)	F1522	F2232	F3247	F4764	GT64	GT180	GT256	GT625	1HAF	2HAF	3HAF	4HAF	MID	HAOCT	HET
0.01 to 14.999999	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1
15 to 21.999999	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0
22 to 31.999999	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0
32 to 46.999999	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0
47 to 63.999999	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0
64 to 127.999999	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0
128 to 179.999999	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0
180 to 255.999999	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0
256 to 349.999999	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0
350 to 511.999999	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0
512 to 624.999999	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0
625 to 729.999999	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
730 to 1056.000000	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0

Table 6D-2. Frequency Band Logic States

FREQUENCY BAND (MHz)	CIRCUIT BOARD	PIN DIODES TURNED“ON”
0.01 to 15	Output, A8	CR18, CR24
15 to 22	Output, A8	CR6, CR10, CR4, CR16
22 to 32	Output, A8	CR7, CR11, CR4, CR16
32 to 47	Output, A8	CR8, CR12, CR4, CR16
47 to 64	Output, A8	CR9, CR13, CR4, CR16
64 to 128	Premodulator, A10	CR28, CR22, CR31
128 to 180	Premodulator, A10	CR26, CR27, CR71, CR22, CR31
180 to 256	Premodulator, A10	CR24, CR25, CR71, CR22, CR31
256 to 350	Premodulator, A10	CR9, CR10, CR14, CR15, CR16
350 to 512	Premodulator, A10	CR9, CR10, CR17, CR18, CR19
512 to 730	Premodulator, A10	CR11, CR12, CR13, CR17, CR18, CR19
730 to 1056	Premodulator, A10	CR11, CR12, CR13, CR14, CR15, CR16
0.01 to 625	Output, A8	CR15
625 to 1056	Output, A8	CR145

If the Premodulator PCA output appears to be correct, the problem is on the A11 Modulation Control PCA, the A8 Output PCA (between the input, W1, and the detector diode, CR20), or possibly on the A13 Controller PCA.

With the instrument programmed for SPCL 01, frequency set to 88 MHz, and level set to 13 dBm, the voltage at TP7 (leveling-loop control voltage) should be approximately +1.7V dc. With the RF output programmed off, the voltage at TP7 should be 0V. If these voltages are not correct, look at the Modulation Control PCA circuitry associated with U21, U6, U8, U9, U11, U12, U4, or check inputs from the controller.

With the instrument programmed as in the preceding paragraph, the voltage at TP8 should be +1.3 ±0.5V dc. In the unleveled state, the voltage at TP8 should be greater than +11V dc. If the instrument is working properly, signal levels between the modulator and the detector are typically as noted in Table 6D-3.

A high voltage at TP8 will cause the ac voltages to be high unless this part of the circuitry is defective. Investigate any dc voltage discrepancies that may indicate the source of the problem.

If high ac voltages are measured, the unleveled problem is most likely with the detector diode, CR20, on the Output PCA, or with U7 or U41 and associated circuitry on the Modulation Control PCA.

Output Assembly Test Point Signal Information 6D-9.

Table 6D-4 presents the nominal characteristics of the signals at the various test points on the Modulation Control PCA. The table shows the range of the signal and the expected value for the instrument preset state (SPCL 01).

RF LEVEL ADJUSTMENTS 6D-10.

The Output Section adjustments listed below are covered in the following paragraphs:

- Modulation Control PCA, A11
    - R23, level dac offset adjustment
    - R8, AM dac offset adjustment
    - R28, detector offset/linearity adjustment
    - R10, AM depth adjustment
    - R20, RF level adjustment
    - R71, external modulation level indicator adjustment
    - R99, sum loop steer gain adjustment
- Premodulator PCA, A10
    - R51, C7, AM bandwidth adjustment
- Output PCA, A8
    - R96, Q16 bias adjustment
    - R1, Q9 bias adjustment
    - R72, het mixer level adjustment
    - R10, het gain adjustment
    - C201, gain flatness adjustment

Potentiometers R82, R101, and R102 are related to FM performance and are discussed under "Alignment of FM PCA (A14)" in Section 6E.

You can make adjustments in any order unless it is noted that the adjustment interacts with another adjustment. Adjustments that are interdependent must be performed in sequence. If more than one adjustment is necessary, perform the adjustments in the sequence presented.

Table 6D-3. Modulator/Detector Nominal Voltages

LOCATION	VOLTS DC	VOLTS AC @ 88 MHz
CR31 cathode	-15V	180 mV p-p
CR28 anode	-12V	1.2V p-p
Q5 collector	+7.5V	270 mV p-p
U8 output	+5.5V	600 mV p-p
Q1 collector	+9.5V	1.25V p-p
CR5 anode	+.7V	1.25V p-p
CR14 cathode	+.7V	1.2V p-p
CR17 anode	+.7V	1.15V p-p
NOTE: Measured with a 10 MΩ, 8 pF oscilloscope probe with a short ground lead		

Table 6D-4. A11 Modulation Control PCA Test Points

TYPICAL TEST POINT	SIGNAL TYPE	RANGE	FOR SPCL 01	SIGNAL DESCRIPTION
TP1	dc	0.98 +/-5 mV	0.980V	Ext. AM/FM level indicator reference
TP2	dc+audio	+14V to 0V	2.6V	Detector Linearizer output
TP3*	N/A			
TP4	Not Used			
TP5	dc+audio	0.2 to 4V	0.3V (on)	Pulse Modulator to Output PCA
TP6	dc+audio	0 to 2.8V	0.0V dc	AM input scaled by % AM
TP7	dc+audio	0.04 to 3.0V dc nominal	1.0V dc	Leveling loop control voltage.
TP8	dc+audio	+14V dc nominal	1.0V dc	Modulator control voltage.
* This test point is an input for factory test of ALC loop.				

Mod Control PCA Level DAC Offset Adjustment, R23 6D-11.

TEST EQUIPMENT:

- DVM

REMARKS:

The level dac offset adjustment is normally required only when U4 or any associated components are replaced.

CAUTION

This adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

With the RF OUTPUT set to OFF, adjust the level dac offset, R23 for 0 ±0.5 mV at TP7.

1. Access R23 by removing both the bottom instrument cover and the bottom module cover.
2. Program the unit under test (UUT) to SPCL 01, and program the RF OUTPUT to OFF.
3. Connect the DVM to measure the voltage between TP7 and ground on the module plate.
4. Adjust R23 for an indication of 0 mV ±0.5 mV.
5. Program the UUT RF OUTPUT to ON.
6. Reinstall the module plate cover and instrument cover when the adjustments are complete.

Mod Control PCA AM DAC Offset Adjustment, R8 6D-12.

TEST EQUIPMENT:

- DVM

REMARKS:

The AM dac offset adjustment is normally required only when U8 or any associated components are replaced.

CAUTION

This adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

With AM off, adjust the AM dac offset, R8 for 0 ±0.5 mV at TP6.

1. Access R8 by removing both the bottom instrument cover and the module plate cover.
2. Program the UUT to SPCL 01.
3. Connect the DVM to measure the voltage between TP6 and ground on the module plate.
4. Adjust R8 for an indication of 0 mV ±0.5 mV.
5. Reinstall the module plate cover and the instrument cover when the adjustments are complete.

Mod Control PCA Detector Offset Adjustment, R28 6D-13.

The detector offset adjustment sets the detector offset voltage. The adjustment also affects AM depth adjustment, R10. Repeat Section 6D-14 after this adjustment.

TEST EQUIPMENT:

- Power meter
- Power sensor (high level)

REMARKS:

Operate the UUT at room temperature for at least one hour with the module plate cover in place before continuing with this adjustment procedure.

Perform this adjustment when components in the detector or detector linearizer circuits have been replaced. If the detector offset is adjusted, perform the AM depth adjustment.

CAUTION

The detector offset adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

While operating in fixed range, adjust the detector offset adjustment, R28 to provide a 23-dB change in output power for a 24-dB change in the level dac.

1. Access R28 by removing the instrument bottom cover.
2. Program the UUT to SPCL 01, 350 MHz and +12 dBm.
3. Program the UUT to SPCL 51. This Special Function enables amplitude fixed range.

4. Remove the detector offset adjustment access screw from the bottom module plate cover.

5. Zero the power meter.

6. Connect the power sensor to the UUT RF OUTPUT connector.

7. Note the power meter reading.

8. Use the EDIT knob to program the UUT for -12 dBm. Be certain to use the EDIT knob to change the amplitude for this step or the special function will be automatically cleared.

9. Adjust the detector offset adjustment, R28, for a power meter reading 23 dB ±0.1 dB below the reading obtained in step 7. Program the UUT to +12 dBm.

10. Repeat steps 7 through 9 until the difference between the power measurements is 23 ±0.1 dB. This adjustment should require three or fewer iterations.

11. Use the EDIT knob to program the UUT to +17 dBm. Note the power meter reading.

12. Use the EDIT knob to program the UUT for +2 dBm. Verify that the power meter reading is 15 dB ±0.2 dB below the previous reading.

13. Program the UUT for SPCL 50. This disables amplitude fixed range.

14. Disconnect the power sensor from the UUT, and reinstall the detector offset adjustment access screw.

Mod Control PCA AM Depth Adjustment, R10 6D-14.

TEST EQUIPMENT:

- DVM
- Modulation Analyzer
- Low-Frequency Synthesized Signal Generator (LFSSG)

REMARKS:

The UUT must be operated at room temperature for at least one hour with the module plate covers in place before continuing with this adjustment procedure.

CAUTION

The AM depth adjustment directly affects the output level and should not be made indiscriminately.

The AM depth adjustment is normally required only when components in the AM signal processing circuits have been replaced. If this adjustment is made, repeat both the adjustment described under “Mod Control PCA Detector Offset Adjustment, R28” and the adjustment described under “Mod Control PCA RF Level Adjustment, R20”.

PROCEDURE:

Adjust the AM depth adjustment, R10, for 90% AM depth as measured with the modulation analyzer when the UUT is programmed to 90% AM.

1. Remove the AM depth adjustment access screw from the bottom module plate cover.
2. Connect the output of the LFSSG to the UUT MOD IN connector and to the DVM using a BNC tee connector.
3. Program the UUT to SPCL 01, 350 MHz, +4 dBm, and EXT AM AT 90% AM DEPTH.
4. Program the LFSSG for 1 kHz and 0.7071V rms as measured by the DVM.
5. Connect the UUT RF OUTPUT connector to the modulation analyzer input.
6. Program the modulation analyzer to measure AM + Peak, in a 0.05 to 15 kHz bandwidth.
7. Alternately measure +PEAK and -PEAK, and adjust the AM depth adjustment, R10, until the readings are symmetrical about 90%.
8. Reinstall the AM depth adjustment access screw.

Mod Control PCA RF Level Adjustment, R20 6D-15.

TEST EQUIPMENT:

- Power meter
- Power sensor (high Level)

REMARKS:

The UUT must be operated at room temperature for at least one hour with the module plate covers in place before continuing with this adjustment procedure.

This adjustment is required if any of the following events occur:

- The Output PCA, the Modulation Control PCA, or the Attenuator/RPP Assembly has been replaced.
- The AM depth adjustment is made.
- The level dac or any associated components are replaced.
- The RF level adjustment has been inadvertently changed.

CAUTION

The RF level adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

With the UUT programmed to +9 dBm, adjust the RF level adjustment, R20, for +9 dBm output as measured with the power meter.

1. Program the UUT to SPCL 01, 350 MHz, and +9 dBm.
2. Zero the power meter.
3. Remove the RF level adjustment access screw from the bottom module plate cover.
4. Connect the power sensor to the UUT RF OUTPUT connector.
5. Adjust RF level adjustment, R20, for a reading of exactly +9 dBm on the power meter.
6. Reinstall the RF level adjustment access screw.

Mod Control PCA External Modulation Level Indicator Adjustment, R71 6D-16.

TEST EQUIPMENT:

- DVM

REMARKS:

This adjustment is normally made if CR12 or R70-R74 are replaced.

PROCEDURE:

Adjust the potentiometer to provide 0.98V dc at TP1. This adjusts both AM and FM indicators, as the remaining levels are set by fixed resistors.

1. Remove the bottom instrument cover and remove the access screws for TP1 and R71.
2. Connect the DVM to TP1 and ground.
3. Set the UUT to SPCL 01 and observe the DVM.
4. Adjust R71 for 0.980 volts.
5. Reinstall the access screws and bottom cover.

Mod Control PCA Sum Steer Gain Adjustment, R99 6D-17.

TEST EQUIPMENT:

- DVM

REMARKS:

The Sum Steer Gain Adjustment is normally required only when U32, U36, or any associated components are replaced.

PROCEDURE:

The sum steer voltage is adjusted to 10.24V with the Sum Loop VCO steering dac set to full scale.

1. Program the UUT to SPCL 01.

2. Program the UUT to SPCL 942. This special function programs all dacs to full scale.

3. Connect the DVM to measure the voltage between J2 pin 14 and module ground.

4. Adjust R99 for 10.24V ±0.01V.

5. Program the UUT for SPCL 00. This clears all special functions.

Output PCA Het Mixer Level Adjustment, R72 6D-18.

TEST EQUIPMENT:

- Power meter
- Power sensor (high Level)
- Spectrum analyzer

REMARKS:

The UUT must be operated at room temperature for at least one hour with the module covers in place before continuing with this adjustment procedure.

This adjustment is normally required only when mixer U4 or het band LO circuitry is replaced. When adjusted, an interaction with R10 exists, therefore R10 adjustment is included in this procedure.

CAUTION

This adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

With the UUT programmed to +16 dBm and 14.9 MHz, the worst in band spur is adjusted to be well within specification. A lower level of this spur degrades the broadband noise in the het band. The het level is then appropriately readjusted.

1. Remove the bottom cover and the appropriate access screws on the bottom module plate for R10 and R72.

2. Program UUT to SPCL 01, 15 MHz, and +16 dBm. Connect the power meter to the output of the UUT. Edit the level to +16 dBm. Set the power meter to dB(ref).

3. Edit the frequency to 14.9 MHz, and adjust R10 for 0 dB(REL)

4. Connect the spectrum analyzer to the UUT and observe the spur at 5.5 MHz. Observe this spur with high spectrum analyzer attenuation (typically 30 dB) to avoid internal analyzer spurs. The resolution bandwidth and span should be narrow (typically a span of 1 kHz and resolution bandwidth of 10 Hz) to allow the spur to be seen clearly.

5. Adjust the spur to a level of -89 dBm ±2 dB with R72. This has changed the adjustment in step 3 above, so steps 3 through 5 must be sequenced again until the level is 0 dB(REL) ±0.1 dB.

6. Reinstall the access screws.

Output PCA Het Level Adjustment, R10 6D-19.

TEST EQUIPMENT:

- Power meter
- Power sensor (high level)

REMARKS:

The UUT must be operated at room temperature for at least one hour with the module plate covers in place before continuing with this adjustment procedure.

This adjustment is normally required only when components in the het band circuits have been replaced or when R72 is adjusted.

CAUTION

This adjustment directly affects the output level and should not be made indiscriminately.

PROCEDURE:

With the UUT programmed to +9 dBm, adjust the het level adjustment, R10, for equal output power at 14.9 and 15 MHz.

1. Program the UUT to SPCL 01, 15 MHz, and +9 dBm.

2. Zero the power meter.

3. Remove the het level adjustment access screw from the bottom module plate cover.

4. Connect the Power Sensor to the UUT RF OUTPUT connector. Note the power meter reading.

5. Program the UUT to 14.9 MHz.

6. Adjust the het level adjustment, R10, for a reading equal to that previously noted.

7. Reinstall the het level adjustment access screw.

Premodulator PCA Level Adjustment, R51 6D-20.

The following procedure covers the adjustment of R51 on the Premodulator PCA. This adjustment optimizes the Premodulator output level in the 256- to 1056-MHz band.

TEST EQUIPMENT:

- Power meter

REMARKS:

Normally this adjustment is performed when changes are made to the A10 Premodulator PCA.

PROCEDURE:

Adjust R51 so that the premodulator output is +3.5 dBm at 800 MHz.

1. Remove both the bottom instrument cover and the bottom module plate cover.
2. Program the UUT to SPCL 01, 800 MHz, and +7 dBm. Measure the output power of the Premodulator PCA by disconnecting the cable from J16 on the Premodulator PCA and connecting the power meter. Adjust R51 for +3.5 dBm.
3. Remove the power meter and move the cable from the output board to J16 on the Premodulator PCA.
4. Reinstall the bottom module cover and the bottom cover.

Output PCA Q16 Bias Adjustment, R96 6D-21.

Perform the following procedure to adjust R96 on the Output PCA.

TEST EQUIPMENT:

- DVM

REMARKS:

Perform this adjustment only if Q16 or any associated parts are replaced. This adjustment sets the bias current in the output transistor for designed operating conditions.

PROCEDURE:

Adjust R96 for 1.355V dc between TP1 and TP2.

1. Remove the bottom cover of the instrument, the bottom module cover, and the pulse cover. This allows access to both the test points and R96.
2. Place the positive (+) lead of the DVM on TP2 and the negative (-) lead on TP1. Set the DVM to Vdc and the 2 volt range.

3. Turn the Signal Generator on and let it operate for 15 minutes. Program the UUT with SPCL 01.

4. Adjust R96 until the DVM reads 1.355V dc.

5. Reinstall the pulse cover, the module cover, and the instrument bottom cover.

Output PCA Q9 Bias Adjustment, R1 6D-22.

Perform the following procedure to adjust the bias of Q9 on the Output PCA.

TEST EQUIPMENT:

- Spectrum analyzer

REMARKS:

Perform this adjustment only when Q9 or its associated circuitry is replaced.

PROCEDURE:

R1 adjusts the collector current of Q9 to minimize harmonic distortion.

1. Remove the bottom instrument cover, bottom module plate cover, and the pulse cover.

2. Connect UUT RF OUTPUT to the spectrum analyzer. Set the spectrum analyzer sweep to cover the frequency range of 1 to 1300 MHz and set the analyzer reference level to +13 dBm.

3. Set UUT to SPCL 01, and set the amplitude to +13 dBm.

4. Edit the frequency to display signal and harmonics on the spectrum analyzer. Adjust R1 to minimize the worst harmonic on the display. This is typically the second harmonic with the UUT frequency at about 300 MHz. The harmonic must be less than 30 dBc for proper operation.

5. Reinstall the pulse cover, the module plate cover, and the instrument cover.

Output PCA Gain Flatness Adjustment, C201 6D-23.

This procedure describes adjusting C201 to optimize gain flatness. Perform this adjustment when CR20 (detector diode) or parts in the RF path following C180 are replaced. Follow this adjustment by the output compensation. See Section 7.

TEST EQUIPMENT:

- Power meter
- Tuning tool, 0.025 in. square, Johanson #4192

PROCEDURE:

1. Zero the power meter

2. Program the UUT to SPCL 01, 350 MHz, and +7 dBm. Connect the power meter to the UUT RF OUTPUT.

3. Set the power meter to dB REF.

4. Edit the UUT frequency from 15 to 1056 MHz and note the variation in level. Adjust C201 to minimize the level variation. C201 will have the greatest effect at high frequencies. Level should be flat with a maximum allowed variation of 3dB.

FM Gain Adjustment, R82, on Mod Control PCA 6D-24.

See "Alignment of FM PCA" in Section 6E.

FM Steer Gain, R101 on Mod Control PCA 6D-25.

See "Alignment of FM PCA" in Section 6E.

FM INV Balance, R102 on Mod Control PCA 6D-26.

See "Alignment of FM PCA" in Section 6E.

ATTENUATOR/REVERSE POWER PROTECTION (RPP) 6D-27.

The A20 Attenuator/RPP Assembly consists of the A21 Attenuator/RPP PCA, the A7 Relay Driver PCA, and a metal housing. The Attenuator/RPP PCA mounts inside the housing and the Relay Driver attaches on top of the housing. This assembly mounts to the Output Module, opposite the Output PCA. The output signal of the Output PCA (at P1) is input to the Attenuator/RPP PCA (at J1).

The Attenuator section of the Attenuator/RPP PCA provides an attenuation range of 0 to 138 dB in 6-dB steps through the use of seven, independently cascaded, 50Ω attenuation sections (K1 through K7). The seven sections consists of one 6-dB, one 12-dB, and five 24-dB sections. Each section includes a DPDT relay and a pi attenuator pad. When dc power is applied to the relay, one relay position provides a low-loss through path for the RF signal. When no dc power is applied to the relay, the other position inserts the attenuator into the RF signal path. The Controller PCA controls the attenuation sections through the Relay Driver PCA. The compensation memory on the Controller PCA stores the attenuation correction data for each attenuator. The leveling-loop control voltage applies the necessary correction.

The reverse power protection section of the Attenuator/RPP PCA protects the attenuator and the output amplifier from excess applied dc voltage or RF power. C6 and C7 provide a dc voltage block. With no dc power applied to the relay, K8 is in the protect position. This position protects against long duration excess RF power.

Detector diode CR1 senses excess RF power and trips the latching comparator circuit (U1A) on the Relay Driver PCA. This change of state of U1A passes through U1D, Q8, and Q9 to remove the dc power from K8. This puts K8 into the protect state. Diodes CR2 through CR9 on the Attenuator/RPP PCA form an RF limiter circuit. This provides protection against short duration excess power events or until K8 can change state, which may take up to 4 ms.

When latching comparator U1A, on the Relay Driver PCA, changes to the tripped state, the positive voltage on U1A pin 1 is applied to the inverting input of U1C causing the output of U1C to go low (approximately 0V dc). This signal (RPTRPL) informs the Controller that the RPP has been tripped, which causes the instrument to go into the RF OFF state and flashes the STATUS light. Diodes CR8 and CR9 provide bias voltage for the limiter diodes to set the limiting threshold. The excess power detection threshold (for CR1 on the Attenuator/ RPP PCA) is set by the resistor network at the input of U1A.

ATTENUATOR/RPP TROUBLESHOOTING 6D-28.

Attenuator problems are most often caused by relay contact problems.

Connect the power meter to the UUT RF OUTPUT connector and by referring to Table 6D-5, check the nominal levels at 100 kHz and 1056 MHz to isolate a faulty attenuator section.

Table 6D-5. Attenuator Levels

ATTENUATOR	PROG LEVEL	SPECIAL FUNCTION	OBSERVED LEVEL (NOMINAL)
6 dB	+6 dBm	-	+6 dBm
12 dB	0 dBm	-	0 dBm
24 dB #1	-12 dBm	-	-12 dBm
24 dB #2	-12 dBm	923	-12 dBm
24 dB #3	-12 dBm	924	-12 dBm
24 dB #4	-12 dBm	925	-12 dBm
24 dB #5	-12 dBm	926	-12 dBm

Use Table 6D-6 to verify proper control of the attenuator sections versus the programmed UUT level. Errors could indicate a failure of the Controller PCA or the Relay Driver PCA, especially Q1 through Q7 and their associated circuitry.

To isolate a through-path problem on the Attenuator/RPP PCA, first verify the Output PCA signal, see “Unleveled Condition” in Section 6D. If there is an apparent through-path problem but one of the observed levels from Table 6D-5 is correct, that associated relay may be at fault.

Another way to isolate a bad relay is to remove the Attenuator/RPP assembly from the module, leaving the control/power ribbon cable attached. Connect a grounding lead between the Attenuator/RPP housing and the Output Module. Program the UUT to +10 dBm and check continuity with an ohmmeter from J1 through to C7. Be sure that the RPP is not tripped. Tracing through the Attenuator/RPP may locate a defective relay contact.

Check RPP trip operation using the test points provided on the Relay Driver PCA. Connect a power meter to the UUT RF OUTPUT connector, and program the UUT to SPCL 01 and then set level to +10 dBm. A momentary short across the terminals of TP1 should trip the RPP, causing the observed output power to drop by more than 30 dB. Failure indicates a problem with U1A, U1D, Q8, Q9, K8, or associated circuitry.

You can reset the RPP by pressing the RF OUTPUT ON/OFF switch. You can reset just the RPP by momentarily shorting across TP2, but this will not reset the rest of the UUT to RF output on. If the RPP cannot be reset, this indicates a problem with U1B, U1A, or its associated circuitry.

Program the UUT to amplitude fixed range (SPCL 51), and edit the level to -10 dBm using the knob. Place a clip lead short across TP3. This will allow the RPP to trip at low RF levels. Use the EDIT knob and adjust the level upwards in 1-dB steps. The RPP should trip before the level reaches +13 dBm. Failure indicates a problem with CR1 (on the Attenuator/RPP PCA) or with U1A, U1D, Q8, Q9, K8, or associated circuitry (on the Relay Driver PCA).

Table 6D-6. Attenuator Level Control

AMPLITUDE RANGE IN dBm (CW)	ATTENUATOR SECTIONS INSERTED (INDICATED BY X)						
	A6DB	A12DB	A241	A242	A243	A244	A245
+7.0 to +20.0							
+1.0 to +6.9	X						
-5.0 to +0.9		X					
-11.0 to -5.1	X	X					
-17.0 to -11.1			X				
-23.1 to -17.1	X		X				
-29.1 to -23.2		X	X				
-35.1 to -29.2	X	X	X				
-41.1 to -35.2			X	X			
-47.1 to -41.2	X		X	X			
-53.2 to -47.2		X	X	X			
-59.2 to -53.3	X	X	X	X			
-65.2 to -59.3			X	X	X		
-71.2 to -65.3	X		X	X	X		
-77.2 to -71.3		X	X	X	X		
-83.3 to -77.3	X	X	X	X	X		
-89.3 to -83.4			X	X	X	X	
-95.3 to -89.4	X		X	X	X	X	
-101.3 to -95.4		X	X	X	X	X	
-107.4 to -101.4	X	X	X	X	X	X	
-113.4 to -107.5			X	X	X	X	X
-119.4 to -113.5	X		X	X	X	X	X
-125.4 to -119.5		X	X	X	X	X	X
-147.0 to -125.5	X	X	X	X	X	X	X

Section 6E

Frequency and Phase Modulation

FM/ϕM FAULT TREE 6E-1.

Refer to the FM/ϕM Fault Tree, Figure 6E-1, when troubleshooting FM/ϕM problems.

FM/ϕM BLOCK DIAGRAM 6E-2.

Figure 6E-2, the FM/ϕM Block Diagram, illustrates connections and signal paths between the A6 Mod Oscillator PCA, the A11 Modulation Control PCA, and the A14 FM PCA that are discussed in this section. In addition, the diagram details the major functional sections and signal paths of the FM section.

FM/ϕM CIRCUIT DESCRIPTION 6E-3.

The A14 FM PCA controls correct ranging and frequency modes for the Signal Generator's FM and ϕM function. (See the A14 FM PCA schematic diagram in Section 10.) The FM phase-locked loop consists of the following:

- An 80-MHz voltage-controlled oscillator that operates in one of two selectable bandwidths. The oscillator has a modulation port, a control port, and a presteering section.
- Programmable dividers for reference and variable frequencies.
- Selectable normal and wide range phase detectors.
- Loop amplifier and filter circuitry.
- Logic circuitry.
- Modulation section with both high modulation rate and low modulation rate paths.

The A11 Modulation Control PCA circuitry processes input signals that are used for modulation. The tasks of this PCA include: internal or external signal selection, input amplitude sensing, signal polarity, level venier, and dc FM oscillator steering.

The A6 Mod Oscillator PCA provides the internal FM signal to the Modulation Control PCA.

Refer to Section 2, Theory of Operation for additional discussion about the frequency and phase modulation circuits.

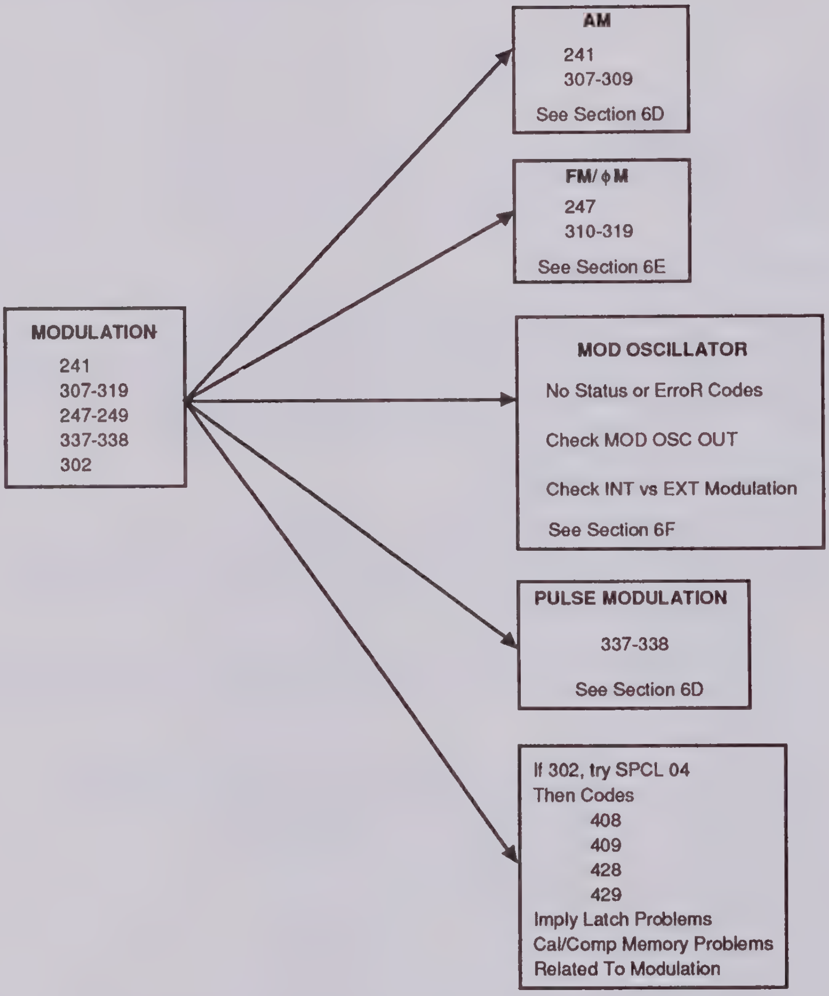

MODULATION
241
307-319
247-249
337-338
302
AM
241
307-309
See Section 6D
FM/ϕM
247
310-319
See Section 6E
MOD OSCILLATOR
No Status or ErroR Codes
Check MOD OSC OUT
Check INT vs EXT Modulation
See Section 6F
PULSE MODULATION
337-338
See Section 6D
If 302, try SPCL 04
Then Codes
408
409
428
429
Imply Latch Problems
Cal/Comp Memory Problems
Related To Modulation

Figure 6E-1. FM/ϕM Fault Tree

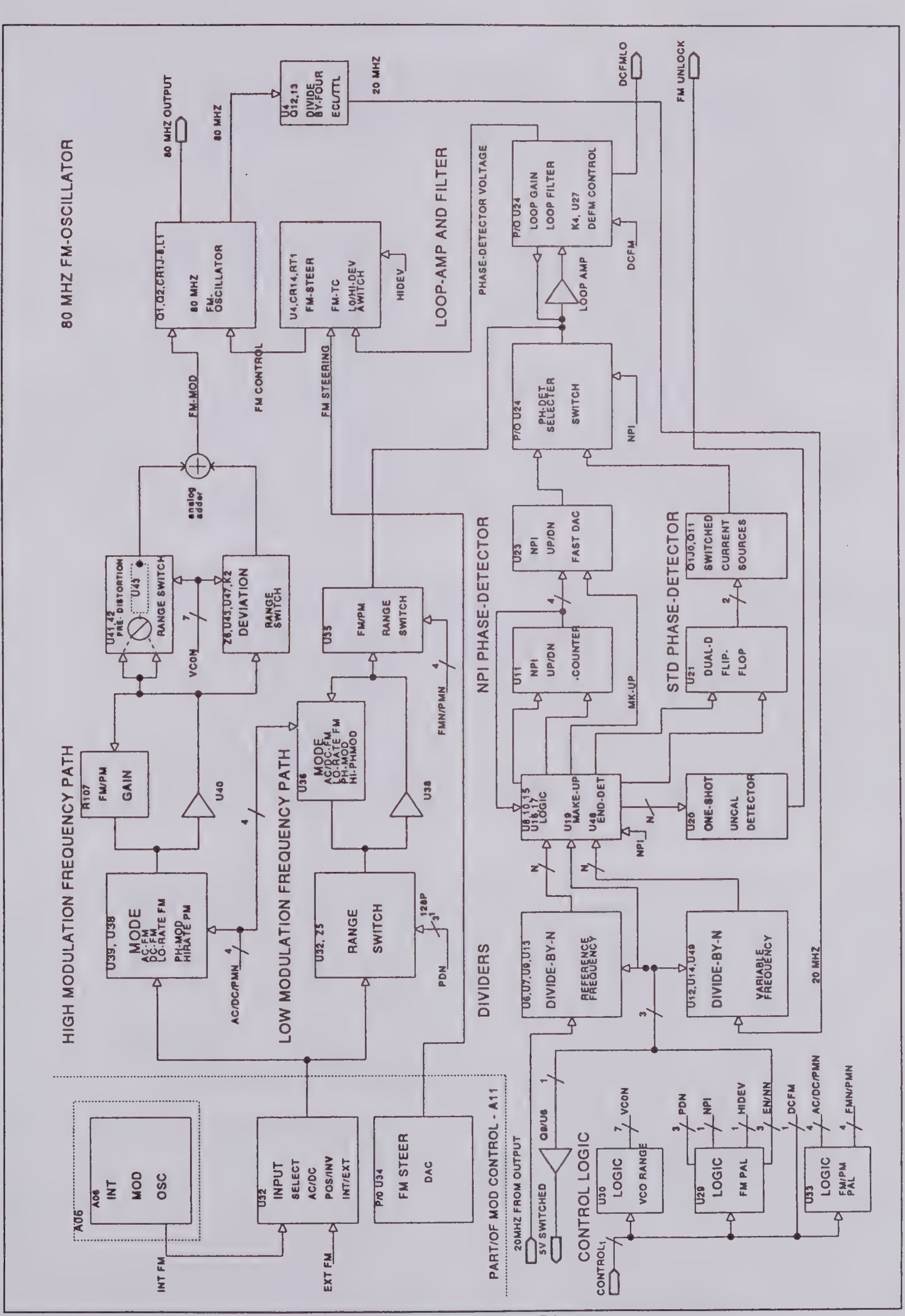

80 MHZ FM-OSCILLATOR
80 MHZ OUTPUT
80 MHZ
U4 Q12,13 DIVIDE BY-FOUR ECL/TTL
20 MHZ
Q1,Q2,CR1,L1 80 MHZ FM-OSCILLATOR
U4,CR14,RT1 FM-STEER FM-TC LO/HI-DEV SWITCH
HIDEV
LOOP-AMP AND FILTER
PHASE-DETECTOR VOLTAGE
P/O U24 LOOP GAIN LOOP FILTER K4, U27 DEFM CONTROL
LOOP AMP
DCFM
DCFMLO
FM UNLOCK
FM-MOD
FM CONTROL
FM STEERING
analog adder
P/O U24 PH-DET SELECTER SWITCH
NPI
HIGH MODULATION FREQUENCY PATH
U41,42 PRE-DISTORTION U43 RANGE SWITCH
VCON
7
Z6,U43,U47,K2 DEVIATION RANGE SWITCH
R107 FM/PM GAIN
U40
U39, U38 MODE AC-FM DC-FM LO-RATE FM PH-MOD HIRATE PM
AC/DC/PMN
4
LOW MODULATION FREQUENCY PATH
U35 FM/PM RANGE SWITCH
FMN/PMN
U36 MODE AC/DC-FM LO-RATE FM PH-MOD HI-PHMOD
U38
U32, 25 RANGE SWITCH
128P
3
PDN
NPI PHASE-DETECTOR
U23 NPI UP/DN FAST DAC
U11 NPI UP/DN COUNTER
MK-UP
STD PHASE-DETECTOR
Q1,Q,Q11 SWITCHED CURRENT SOURCES
2
U21 DUAL-D FLIP-FLOP
U8,10,15 U16,17 LOGIC U19 MAKE-UP U48 END-DET
N
U20 ONE-SHOT UNCAL DETECTOR
NPI
DIVIDERS
U6,U7,U9,U13 DIVIDE-BY-N REFERENCE FREQUENCY
U12,U14,U49 DIVIDE-BY-N VARIABLE FREQUENCY
20 MHZ
A06
A06 INT MOD OSC
U32 INPUT SELECT AC/DC POS/INV INT/EXT
P/O U34 FM STEER DAC
INT FM
EXT FM
PART/OF MOD CONTROL - A11
20MHZ FROM OUTPUT
5V SWITCHED
Q8/U6
1
CONTROL LOGIC
CONTROL
U30 LOGIC VCO RANGE
VCON
U29 LOGIC FM PAL
PDN
NPI
HIDEV
EN/NN
U33 LOGIC FM/PM PAL
DCFM
AC/DC/PMN
FMN/PMN

Figure 6E-2. FM/ϕ M Block Diagram

Oscillator Section 6E-4.

The voltage-controlled oscillator (vco) section includes two variable components: L1 and C9, along with varactors (voltage variable capacitors) CR1-CR8, and associated capacitors. Capacitors C2 and C4 couple the resonant circuit to the input of active circuit Q1 and Q2. Capacitors C10, C11, and C13 couple the circuit to the output of the active circuit. Q3 and Q4 provide clean power supply voltages of +14V dc and -14V dc, respectively.

The oscillator operates in one of two modes: the normal high "Q" mode, and the high deviation mode. The normal mode is the default setting. The oscillator can be reconfigured to a high deviation mode, which provides greater bandwidth to attain the wide deviations needed in the two upper bandwidths.

Components C9, CR15, and L4 switch between the high deviation mode and normal mode. Depending on the level of control line HIDEVL, Q5 and Q8 drive PIN diode CR15 between either conduction or high impedance. Conduction (low impedance) adds C9 into the resonant circuit for a normal mode high "Q" oscillator circuit. High impedance removes C9 from the oscillator during the high deviation mode. Depending on whether C9 is in conduction or high impedance, the varactor voltage adjusts to compensate for the change in capacitance of C9. The varactor voltage both controls and modulates the circuitry.

A control voltage applied to the center connection of the varactors (TP11) keeps the oscillator center frequency at 80 MHz. The cathode voltage is about +15V dc for normal high "Q" mode and about +7V dc for the high deviation mode. The anode of the varactors is nominally 0V dc with the applied modulation. Other components in the vco section isolate and filter the control and modulation lines.

Amplifier U2 buffers the 80-MHz oscillator output to the A12 Sum Loop PCA. Potentiometer R45 and its associated resistors adjust and establish the proper input level. U1 buffers the 80-MHz signal, and U3 and its resistors establish ECL levels to the divide-by-four IC, U4. The 20 MHz signal from U4 is translated from ECL level to TTL level by Q12 and Q13.

During the dc FM mode, a steering circuit made up of quad op amp U5, and Q6 and Q7, keeps the oscillator frequency centered. Diode CR14 provides a stable voltage reference used to control varactor voltages as required. Op amp U5A, Q6, the FM-STEER and V-TC-COMP inputs, potentiometers R35 and R39, and associated resistors provide the nominal voltage at Q7 for the programmed voltage V-PROG at TP2. This voltage is divided by the resistor string of R40, R41, R74, and R133, along with the loop control voltage PH-DET at TP12 and provides the voltage VCO-CONTROL for correct oscillator frequency. The control line HIDEVL is programmed by the instrument control to select HI DEVIATION.

The remaining sections of U5 with RT1, a temperature-sensitive resistor, provide the temperature compensation signal V-TCCOMP (TP9).

Divider Section 6E-5.

The divider section consists of two programmable divider sections: the reference frequency divider and the variable frequency divider. The reference frequency divider consists of U7, U8, U9, U10, and U13. The variable frequency divider consists of U12, U14, U15, U16, U17, and U49.

Each divider section respectively divides the reference frequency and the variable frequency by the same division. The divider sections receive 20 MHz and divide it to one of the following frequencies: 5 MHz, 200 kHz or 50 kHz. which is a division by 4, 100, or 400 from the 20 MHz, or is 16, 400, or 1600 from the 80 MHz FM oscillator. Both dividers are programmed by the control logic to divide by the same division ratio. The modulation mode (normal ac FM, dc FM, ϕM, etc.) and the deviation range (refer to Figure 6E-1) determine the correct division. The lower the range, the less division is required. Less division results in greater bandwidth and less circuit noise.

Each divider consists of three parts: two divide-by-four sections, and a divide-by-25 section. Multiplexers U13 and U49 control each divider section for the correct division. A division by 4 (5 MHz) uses just the first divide-by-four. A division by 100 (200 kHz) uses the first divide-by-four and the divide-by-25. A division by 400 (50 kHz) uses all three divider sections.

Each of the divider sections has different outputs. The reference divider section has two outputs, "RSIG" and "Rck". The variable frequency divider has three output signals: "VSIG", "Vck1", and "Vck2". Within the signals of each divider the signal relationship is fixed, as, for example between RSIG and Rck. But the relationship between the RSIG signals and the VSIG signals can vary in timing as shown by the first and second set of pulses. The output signals are used to control the phase detectors. The relationship of these signals is shown in Figure 6E-3. The reference divider also has a circuit, REF ON/OFF SWITCH, part of U6 and Q9, which controls the 20-MHz input that comes from the A8 Output PCA. The circuit enables the 20 MHz from the Output PCA, except when dc FM is active. These signals drive the phase detectors and are discussed in the following paragraphs.

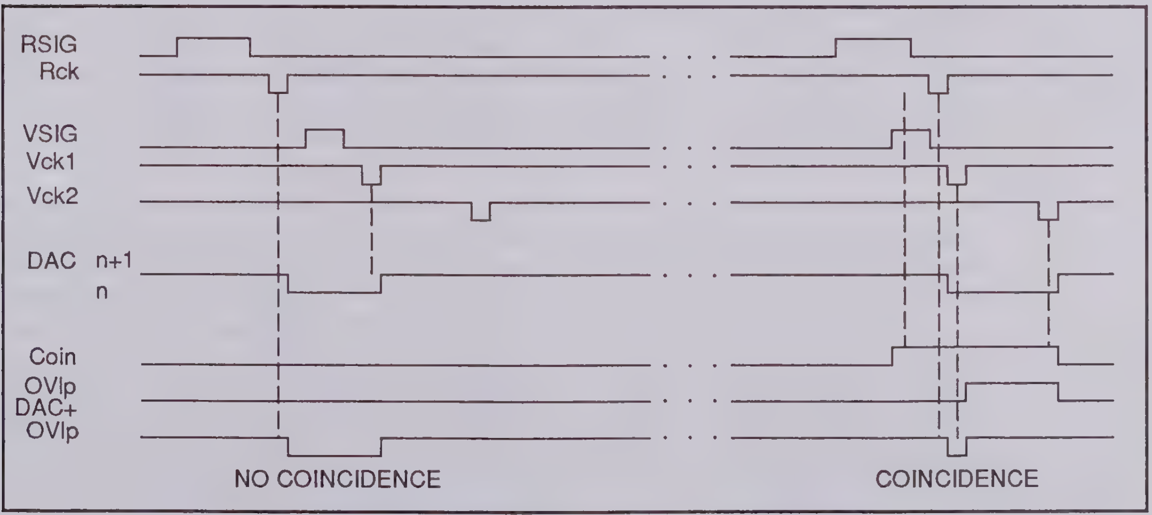


Figure 6E-3. Divider/Phase Detector Timing Diagram

Phase Detectors, Loop Circuits, and Logic Section 6E-6.

Two phase detectors provide for selection of the appropriate frequency: the standard phase detector and the N-PI phase detector. Only one of two phase detectors is active at any time. The first phase detector uses U21 as a normal, standard dual D flip-flop. The other is a wide range, N-PI phase detector that uses up-down counter U11. U21 uses diode-switched resistor current sources; U11 uses switched dac U23. Also associated with the phase detectors and dividers is an unlock detector, U20. This detector responds if an overmodulation or unlocked condition exists at the phase detector divider combination.

The two phase detectors operate at the phase detector reference frequency to produce the output signals. The output signals are related to the phase relationship of the fm-oscillator divider combination and to the phase of the reference frequency divider combination.

One of the phase detectors is programmed active. Analog switch U24 selects the output of the active phase detector and amplifies the signal in the integrating loop amplifier U25. The result is filtered in the low-pass filter (L5-7) and its associated capacitors to reduce the modulation of the 80-MHz FM oscillator by the phase detector reference frequency. The filtered output drives the VCO-CONTROL port of the 80-MHz FM oscillator to achieve phase lock and maintain correct center frequency.

One of two outputs in the standard phase detector U21 is a pulse whose duty cycle is related to the phase relationship of the inputs. The other output becomes active for wide phase deviation. These output signals drive the voltage level-shift circuits, Q10, Q11, and connected resistors, which drive diode (CR20-24) switched resistor current sources. These current pulses are passed through analog switch U24A to the virtual ground input of loop amplifier U25. The average current, proportional to the phase error between the FM oscillator and the reference, is combined with a fixed current in the input. The difference in current is then amplified in the integrating loop amplifier U25 and phase locked, as discussed in the previous paragraph.

For the wide deviation range N-PI phase detector, the reference and variable frequency dividers alternately clock up/down counter U11 between two states with Rck and Vck signals. Refer to Figure 6E-3. The up/down counter output four bits connect to the four most significant bits of dac U23, alternating the dac between two states of its total range of 16 states. This output is converted to a voltage output in an op amp, U50, and into a current output with resistors R134 and R94 to drive through analog switch U24 into loop amplifier U25. The alternating action of up/down continues smoothly as long as the up/down inputs do not coincide.

To prevent coincidence problems from occurring, an approaching coincidence condition is detected with one part of the OVERLAP PULSE AND COINCIDENCE detector, U19, using the divider outputs "RSIG" and "VSIG". The "RSIG" input connects to the "D" input of a first D flip-flop, and "V" connects to the clock input of the same flip-flop. This sets up the flip-flop and Vck1/Vck2 switch, U18, so that the second flip-flop, U19 will make an overlap pulse, clocked by signal "Vck1" and reset by signal "Vck2" to drive the dac least significant bits. Switch U18 causes the up/down counter to use the second "V" clock ("Vck2" instead of "Vck1") for clocking, causing a missing portion. The overlap pulse, which occurs at the time between the "Vck1" and "Vck2" clock signals, just fills in for the missing portion. The smoothing adjustment R88 makes up for inaccuracies of timing and lower order dac bit substitution.

The up/down counter is prevented from wrapping around from either high to low or low to high by end-count detectors, inverters, and four-input NAND gates that control the appropriate clock inputs. This control information is also used to determine overmodulation or an unlocked loop condition. This information passes to the uncal detector.

The uncal detector U20 receives these inputs and the inputs from the other phase detector. When the phase detectors are close enough to the edge of normal operation, this will trigger the uncal one-shot, U20, which will stretch out the time of abnormal indication. The output, FM UNLCK, is sent to the instrument controller.

Following the phase detectors is the loop amplifier U25, which in combination with the analog switch, selects the appropriate phase detector and gain resistors, R66 and R87, to control the phase-locked bandwidth. The circuit is followed by the loop filter, which has rejection notches at 50 kHz, 90 kHz, and 200 kHz. This filter rejection reduces the pulses from the phase detectors to maintain minimum spurious modulation of the FM oscillator.

Also associated with the loop amplifier and loop filter are comparator U27 and relay K4, which are used in dc FM mode in the FM PCA. The instrument enables dc-coupled FM under internal software control as follows:

1. Set up normal ac fm, except disconnect the input modulation signals.

2. Monitor the comparator output, DCFMLO.

3. Adjust the FM STEER dac on the A11 Modulation Control PCA, using an appropriate algorithm until the comparator senses nearly zero voltage at TP12. Repeat as necessary.

4. When satisfied with the null at TP12, assert the DCFMH control closing relay K4. This effectively puts TP12 at 0V dc ground, disables the dividers and phase lock, and disconnects the phase modulation path. The input modulation signals are reconnected through a dc path.

ICs U29, U30, and U33 generate the control signals for the rest of the circuits for the different ranges of modulation and the different modes of operation in FM, ϕM, and DC FM. The inputs are the control lines from the instrument controller, and the outputs control the divider, phase detector, oscillator, and modulation circuits. See the Modulation Control Table (Table 6E-1) for the relationship.

Table 6E-1. Modulation Control Table (@ 800 MHz RF Frequency*)

FM MODES	INPUT						OUTPUT																
	FREQUENCY DEVIATION (kHz) MIN - MAX OR RADIANS+	CONTROL					U30RNG	U29					FREQ REF PHASE DET. (kHz)	U33								LOOP	
		FMRNG	LOWFM	DCFM	PMOD	HRPM		pdsel	NPI	HIDEV	n	EN		ACCP	DCCP	PM0	PM1	pdFM2	pdFM1	pdPM2	pdPM1	R+	BW (Hz)
NORMAL ACFM	N/A	7	UNDEFINED FOR ALL MODES																				
	1.01-4.0M	6	0	0	0	0	6	6	1	1	3	1	50	0	1	1	1	0	1	1	1	1	90
	251k-1.0M	5	0	0	0	0	5	5	1	1	3	1	50	0	1	1	1	0	1	1	1	1	90
	62.5-250k	4	0	0	0	0	4	4	1	0	3	1	50	0	1	1	1	0	1	1	1	2	130
	15.7-62.5	3	0	0	0	0	3	4	0	0	2	1	200	0	1	1	1	0	1	1	1	2	520
	3.91-15.6	2	0	0	0	0	2	5	0	0	2	1	200	0	1	1	1	1	0	1	1	2	520
	0.00-3.90	1	0	0	0	0	1	4	0	0	2	1	200	0	1	1	1	1	0	1	1	2	520
	CW	0	0	0	0	0	0	0	0	0	1	1	5MHz	0	1	1	1	1	1	1	1	1	2.2k
DCFM	1.01-4M	6	0	1	0	0	6	0	0	1	0	0	50	1	0	1	1	1	1	1	1	x	x
	251-1.0M	5	0	1	0	0	5	0	0	1	0	0	50	1	0	1	1	1	1	1	1	x	x
	62.5-250	4	0	1	0	0	4	0	0	0	0	0	50	1	0	1	1	1	1	1	1	x	x
	15.7-62.5	3	0	1	0	0	3	0	0	0	0	0	200	1	0	1	1	1	1	1	1	x	x
	3.91-15.6	2	0	1	0	0	2	0	0	0	0	0	200	1	0	1	1	1	1	1	1	x	x
	0.00-3.90	1	0	1	0	0	1	0	0	0	0	0	200	1	0	1	1	1	1	1	1	x	x
	CW	SEE CW UNDER NORMAL ACFM ABOVE																					
LOW-RATE FM	1.01-4M	6	1	0	0	0	6	6	1	1	3	1	50	1	0	1	1	0	1	1	1	1	90
	251-1.0M	5	1	0	0	0	5	5	1	1	3	1	50	1	0	1	1	0	1	1	1	1	90
	62.5-250	4	1	0	0	0	4	4	1	0	3	1	50	1	0	1	1	0	1	1	1	2	130
	15.7-62.5	3	1	0	0	0	3	3	1	0	3	1	50	1	0	1	1	0	1	1	1	2	130
	3.91-15.6	2	1	0	0	0	2	4	1	0	3	1	50	1	0	1	1	1	0	1	1	2	130
	0.00-3.90	1	1	0	0	0	1	3	1	0	3	1	50	1	0	1	1	1	0	1	1	2	130
	CW	SEE CW UNDER NORMAL ACFM ABOVE																					
PHASE MODULATION	101-400	6	0	0	1	0	6	6	0	1	2	0	200	1	1	0	1	1	1	0	1	1	360
	25.1-100	5	0	0	1	0	5	5	0	1	2	0	200	1	1	0	1	1	1	0	1	1	360
	6.26-6.25	4	0	0	1	0	4	4	0	0	2	0	200	1	1	0	1	1	1	0	1	2	520
	1.57-6.25	3	0	0	1	0	3	3	0	0	2	0	200	1	1	0	1	1	1	0	1	2	520
	.391-1.56	2	0	0	1	0	2	4	0	0	2	0	200	1	1	0	1	1	1	1	0	2	520
	0.00-.390	1	0	0	1	0	1	3	0	0	2	0	200	1	1	0	1	1	1	1	0	2	520
	CW	0	0	0	1	0	0	0	0	0	1	1	5 MHz	1	1	0	1	1	1	1	1	1	2.2k

Table 6E-1. Modulation Control Table (@ 800 MHz RF Frequency*) (cont)

	INPUT						OUTPUT																
FM MODES	FREQUENCY DEVIATION (kHz) MIN - MAX OR RADIANS+	CONTROL					U30RNG	U29					FREQ REF PHASE DET. (kHz)	U33								LOOP	
		FMRNG	LOWFM	DCFM	PMOD	HRPM		pdsel	NPI	HIDEV	n	EN		ACCP	DCCP	PM0	PM1	pdFM2	pdFM1	pdPM2	pdPM1	R+	BW (Hz)
HIGH-RATE PHASE MODULATION	10.1-40	6	0	0	1	1	6	6	0	1	2	0	200	1	1	1	0	1	1	0	1	1	360
	2.51-10.0	4	0	0	1	1	5	5	0	1	2	0	200	1	1	1	0	1	1	0	1	1	360
	.626-2.50	4	0	0	1	1	4	4	0	0	2	0	200	1	1	1	0	1	1	0	1	2	520
	.157-.625	3	0	0	1	1	3	3	0	0	2	0	200	1	1	1	0	1	1	0	1	2	520
	.040-.156	2	0	0	1	1	2	4	0	0	2	0	200	1	1	1	0	1	1	1	0	2	520
	0.00-.039	1	0	0	1	1	1	3	0	0	2	0	200	1	1	1	0	1	1	1	0	2	520
	CW	0	0	0	1	1	0	0	0	0	1	1	5 MHz	1	1	1	0	1	1	1	1	1	2.2k

+ Radians in Phase Modulation

* Ranges and deviation depend on dialed rf frequency. See specifications.

** For column R (under Outputs), 1 is R66, 2 is R87.

Modulation Section 6E-7.

The modulation section consists of a high rate modulation path and a low rate modulation path. The modulation signal comes from the A11 Modulation Control PCA at J6. The signal frequency at this point can range from dc to 200 kHz. Full-scale amplitude for each range is 4V ac pk for full deviation at the modulation frequency. The type of modulation is determined following this point. The logic control signals for range switching and type of modulation are generated in two PAL ICs, U29 and U33, and selector U30. Refer to the previous discussion under the paragraph heading "Phase Detector, Loop Circuits, and Logic Section" for more information about logic control signals, and see Tables 6E-1 and 6E-2.

The high rate path consists of U37, U39 through U43, U45 through U47, K2, and Z6. Level translators U37, U45, and U46 operate from TTL (CMOS) level to the drive level for the analog FET (or DMOS) switches that require levels for "off" of nominal -12V dc and for "on" of +12V dc. The mode switch for ac FM, dc FM (as well as low-rate FM), phmod (normal), and high-rate phmod is U39. This switch functions as a one-of-four selector on the input of an amplifier, U40. Adjustments R104 and C75 are used to balance the different modes of operation. Feedback resistors R107 and R108 around amplifier U40 determine the gain of this path. The amplifier output drives the range resistor network Z6 and range switches.

The range switches consist of relay switch K2, analog switches U47, and part of U43. These are controlled by level translators U45 and U46. The modulation signal is also amplified by U41, which drives analog multiplier U42 to generate a second harmonic. The second harmonic is added to the fundamental modulation signal for predistorting the signal to the modulation port of the 80-MHz VCO. This predistortion cancels the distortion of the VCO. The analog switches in U43, along with the associated resistors, control and adjust the correct amount of predistortion for each range. The output of the range network and switches and the output of the predistortion network are added in the summing resistors R126 and R127. The relay K1 shorts out the large resistor R127 for the low deviation ranges (high "Q" mode). The 49.9Ω resistor R126 improves low-noise performance. The ranges are labeled for FM modulation; however, there are corresponding phase modulation ranges, e.g., 4 MHz, is 400 (40) radians, etc. The range and predistortion paths are interactive and require interactive adjustment for each range; range match: R139, R140, or R141, distortion match: R115, R117, or R119, respectively.

The high rate modulation signal and some of the range control logic signals are sent to the A12 Sum Loop PCA to maintain correct operation there. Since this causes an interaction between the Sum Loop PCA and the A14 FM PCA, a lead-lag compensation is made with R120 and C99 controlled by analog switch Q15 and translator U45. The lead-lag compensation is controlled by the range bit FMRN2H.

Table 6E-2. Modulation Ranges and FM DAC Values

FM DAC = (FM Deviation * Mult)/1111						
FREQ BAND / FM RANGE	512-1056	256-512	128-256	64-128 and 0.01-15	32-64	15-32
6	4.00 MHz 1.01 MHz mult= 1	2.00 MHz 501 kHz mult= 2	1.00 MHz 251 kHz mult= 4	500 kHz 126 kHz mult= 8	250 kHz 62.6 kHz mult= 16	125 kHz 31.3 kHz mult= 32
5	1.00 MHz 251 kHz mult= 4	500 kHz 126 kHz mult= 8	250 kHz 62.6 kHz mult= 16	125 kHz 31.3 kHz mult= 32	62.5 kHz 15.7 kHz mult= 64	31.2 kHz 7.82 kHz mult= 128
4	250 kHz 62.6 kHz mult= 16	125 kHz 31.3 kHz mult= 32	62.5 kHz 15.7 kHz mult= 64	31.2 kHz 7.82 kHz mult= 128	15.6 kHz 3.91 kHz mult= 256	7.81 kHz 1.96 kHz mult= 512
3	62.5 kHz 15.7 kHz mult= 64	31.2 kHz 7.82 kHz mult= 128	15.6 kHz 3.91 kHz mult= 256	7.81 kHz 1.96 kHz mult= 512	3.90 kHz 977 Hz mult=1024	1.95 kHz 489 Hz mult=2048
2	15.6 kHz 3.91 kHz mult= 256	7.81 kHz 1.96 kHz mult= 512	3.90 kHz 977 Hz mult=1024	1.95 kHz 489 Hz mult=2048	976 Hz 245 Hz mult=4096	488 Hz 123 Hz mult=8192
1	3.90 kHz 0 hz mult=1024	1.95 kHz 0 hz mult=2048	976 hz 0 hz mult=4096	488 hz 0 hz mult=8192	244 hz 0 hz mult=16384	122 hz 0 hz mult=32768
0	CW MODE					

The low rate modulation path consists of Z5, Z7, U32, U35, U36, U38, and associated components. This path operates in all modes of modulation except in the dc FM mode and the cw mode. A range network and switch, Z7 and U32, in conjunction with a range network and switch, Z5 and U35, relative to the reference frequency determines the modulation range. The modulation signal is applied to the range resistor network Z7, selected by analog switch U32, and applied to the virtual ground input of a first section of dual op amp U38.

The selected feedback network determines the gain and function. The output of the first op amp U38 is processed by the range network Z5 and range switch U35. Potentiometers R102 and R145 determine the gain of the low rate path for ac FM and phase modulation, respectively. The selected feedback network consists of capacitors and resistors: C70 and R95 for ac FM, R98 and C71 for phase modulation, and R146, R147, and C76 for high rate phase modulation.

The active feedback network consisting of a second op amp U38 and resistors R99 and R95, switches from ac FM to low rate FM. Analog switch U36 controls the selected feedback network for various modes. The Z5, U35 range selection is selected in conjunction with the Z7, U32 combination and has a 16-to-1 relationship. The Z5, U35 combination is also selected relative to ac FM or phase modulation.

Table 6E-1 shows the relationship between selected modulation ranges and functions for inputs, controls, and outputs. Table 6E-2 shows the relationship between the modulation ranges and the FM dac values.

MODULATION CONTROL CIRCUIT DESCRIPTION 6E-8.

The following paragraphs describe the FM modulation circuitry on the A11 Mod Control PCA. Refer to the A11 Mod Control PCA schematic diagram in Section 10. The description is broken into three parts:

- FM input voltage processing
- FM STEER and SUM STEER voltage generation
- FM control signals generation

FM Input Voltage Processing 6E-9.

The circuits listed below select and amplify the external FM input signal and the internal mod oscillator signal from 1V ac pk to 4V ac pk at the top of each FM range (4 MHz, 1 MHz, etc.). They also provide a vernier output within each range as the controller programs the multiplying dac.

- Op Amp U27
- Associated input resistors, capacitors, and CMOS switches, U39
- DAC U34 and Op Amp U9A
- Inverter/amp U9B

Selecting combinations of EXT AC FM or EXT DC FM and INT FM inputs (front panel controls) is done by using the CMOS switches in U39 (and its associated resistors and capacitors) at the input of op amp U27. Potentiometer R82 sets the gain to amplify a 1V ac pk signal to 4V ac pk. The FM DEV dac, U34-1,2 is set to 3600 counts (out of 4096 at full scale).

U34 and op amp U9A produce 4V ac pk to the inverter/amplifier circuit U9B, which in conjunction with CMOS switch Q6 either amplifies directly or inverts the signal to produce the proper polarity output. This accommodates the instrument action of either over or under programming at the sum loop. The multiplying FM DEV dac U34 is under controller operation to produce a vernier output within each range, or overrange in fixed range, or variation of nominal reference of 3600 counts (out of 4096) for closed-case calibration.

Comparators U16C and U16D, and associated resistors, trigger one-shots U26A and U26B when the peak amplitude of the applied external level is centered around 1V ac pk. The controller responds to deviations from 1V ac pk by alerting the operator by way of front panel "HI" or "LO" indicators.

FM STEER Voltage Generation 6E-10.

The FM STEER signal is produced by dac, U32 pins 23 and 24, and op amp U36B. The signal ranges between 0 and 10.2V dc (nominally 5.1V dc) and is adjusted with potentiometer R101. The voltage level is regulated by the controller to zero the frequency offset in dc FM.

FM Control Signals Generation 6E-11.

The controller sends the control signals to the A14 FM OSC PCA where they are latched by U35. These signals are:

- Three range switches: FMRN2H, FMRN1H, and FMRN0H
- Four controls: DCFMH, LOWFMH, PMODH, and HRPMH

FM TROUBLESHOOTING (A14) 6E-12.

FM troubleshooting is divided into three parts:

- Frequency check
- Modulation check
- Input signals and control input checks

Frequency Check 6E-13.

Use Table 6E-3 when checking the performance of the FM oscillator for faults in frequency lock. Note the relationship between the modulation frequency and the divider frequencies.

1. If the frequency is wrong, check the adjustment of oscillator frequency, L1, and C9.

2. If the voltages are wrong at TP11 and TP2, check steering circuit U5.

3. If the divider frequencies are wrong, check the dividers and input drive levels.

4. If the phase detector output at TP12 is high or low, check the phase detectors U11 or U21, current sources U23 and U50, or the Q10 and Q11 circuits.

5. Check the low rate modulation path. Op amp U38 should have 0V at the junction of pin 1 and C70.

6. Check CMOS switches U32, U35, U36, U39, U43, and U47 for proper control voltages.

7. Check associated CMOS switch drivers. Use the Modulation Control Table (Table 6E-1) for logic information. For U36, U39, U43, and U47:

    - V-on > +10V dc, nominally +13V dc.
    - V-of < -12V dc.

8. Check for CMOS switch leakage of control voltage to the signal path.

Table 6E-3. FM Oscillator Frequency Check Table (Normal Operation)

NOTE: Set SPCL to 909, frequency to 800 MHz. Have EXT FM input equal zero.

FM DEV EXT FM	FREQ MHz	VOLTS DC						DIVIDER FREQUENCIES TP 5,15,6,8 U21	DETECTOR TYPE
		TP11	TP 12	TP 4	TP 2	TP 3	TP 9		
Off	80	15	0	0	22	6.3	0-1	--* 5 MHz	std U21
50 kHz	80	15	0	0	22	6.3	0-1	200 kHz 200 kHz	std U21
100 kHz	80	15	0	0	22	6.3	0-1	50 kHz --	NPI U11,23
400 kHz	80	7	0	0	11	6.3	0-1	50 kHz --	NPI U11,23

* TP 5, 15 positive pulses; TP 6, 8 negative narrow pulses

Tolerances TP 2, 11, 12 = 0.5V; TP 4 = 0.01V; TP 3 0.2V

Modulation Check 6E-14.

For errors and faults in modulation, use Table 6E-4.

To check modulation, proceed as follows:

1. First check the FM input to FM PCA at J6 for 4V pk. If no input is present, check the Modulation Control PCA FM circuitry and inputs.

2. For error at TP4 and TP1, check the high modulation frequency path, U40, etc.

3. For error at the junction of U38 pin 1 and C70, check the low frequency modulation path U38, etc.

4. Check all ranges for correct modulation at the output. Use the Modulation Control Table (Table 6E-1) for the logic levels and the ranges for all FM DEV ranges. Check CMOS analog switches and drivers for proper operation.

5. Check phase modulation for a correct output. If the output is not correct, check the ϕM circuits associated with U40 for problems at high modulation frequencies. For errors at low modulation frequencies, check the ϕM circuits associated with U38.

6. For errors in Special Functions LORATE FM and HIRATE ϕM check the circuits associated with U40 and U38.

7. For errors in dc FM, check circuits associated with FM STEER and U5, circuits with the loop amp U25 and relay K4, and the LODCFM detector U27. Also check the FM steer circuits on the Modulation Control PCA. The process is implemented by the controller.

Table 6E-4. FM Oscillator Modulation Control (Normal Operation)

NOTE: Set SPCL 909, RF Freq 800 MHz, INTFM DEV 250 kHz @ 1 kHz (Alternate: Use EXTFM with low frequency signal generator, JF 6011 set to 1 kHz and 383 mV RMS into EXT FM input.)

MOD FREQ	VOLTAGE AT TP4	SIGNAL AT JUNCTION U38-1/C70	SIGNAL TP1
100 Hz	500 mV pk	250 mV pk	4V p-p
1 kHz	500 mV pk	25 mV pk	4V p-p
5 kHz	500 mV pk	< 5 mV pk	4V p-p

Input Signals and Control Input Signals Checks 6E-15.

Check the input signals and control input signals as follows:

1. If the modulation signal is not present at FM PCA J6, check the A11 Modulation Control PCA for the FM dac and amplifiers and switch inverter.

2. If the 20 MHz is not present from the A8 Output PCA, check the switched +5V square wave on J4, and the +5V dc on J7 to the Output PCA.

3. If the control signals are not correct on J1 according to the Modulation Control Table (Table 6E-1), check the latches on the A11 Modulation Control PCA.

FM ADJUSTMENTS 6E-16.

FM adjustments are made on the following pca's:

- A11 Mod Control PCA (FM modulation section)
- A14 FM Board PCA

Make FM adjustments using the following equipment:

- DMM (Fluke 8840A)
- Modulation meter (HP 8901A)
- LFSSG (Fluke 6011A)
- Spectrum analyzer (HP 8586)
- Oscilloscope (Tektronix)

Adjustments on the Modulation Control PCA (A11) 6E-17.

NOTE

Perform the following procedure to adjust the modulation circuitry. Other adjustments are covered in other procedures.

The following procedure describes how to make adjustments to the Modulation Control PCA.

1. Make the following equipment settings:
   a. Set the UUT to SPCL 909, 800 MHz, 0 dBm, 4 MHz dev, EXT AC FM.
   b. Set the 8840A DMM to ac volts, autorange.
   c. Set the 6011A Signal Generator to 1 kHz, 383 mV rms.
2. Connect the 6011A to the UUT EXT FM input and to the 8840A.
3. Set the 6011A (as measured by the 8840A) to 707 mV rms. Set the 8840A to ac volts, and autorange. Connect the 8840A to J16-P1 on 4048 Modulation Control PCA. Adjust R82 for 2.828V rms ±2 mV.
4. Set the UUT to 700 MHz. Set the 8840A to ac volts, autorange. Connect the 8840A to J16-P1 on the A11 Mod Control PCA. Adjust R102 for a reading of 2.828V rms ±2 mV on the 8840A.
5. Set the UUT EXT AC FM off, and set the UUT INT FM on. The 8840A should read 2.828V rms ±2 mV rms.

   Set the UUT INT FM off, and set the UUT EXT AC FM on.
6. Set the UUT to SPCL 943. Connect the 8840A to J2-P14. Set the 8840A to dc volts. Adjust R99 for 10.24V dc ±10 mV.

   Connect the 8840A to J1-P3. Set the 8840A to dc volts. Adjust R101 for 10.24V dc ±10 mV.

   Connect 8840A to J6-P24. Verify that the 8840A reads 10V dc ±.1V dc.
7. Set the UUT to SPCL 909. Connect a 50Ω termination to UUT EXT PULSE MOD. Connect the 8840A to J4-P5. The 8840A should read 0V dc ±0.2V dc. Press the External Pulse Modulation button on the UUT front panel to on. The 8840A should read 4.2V dc ±0.2V dc.
8. Set the UUT to SPCL 909. Set the 8840A to dc volts, 2V range. Connect the 8840A to TP1 on the 4048 board. Adjust the modulation level sense R71 for 0.98V ±0.5V. Remove the 8840A from TP1.
9. Set the UUT to EXT FM. Set the 6011A to 1 kHz and 383 mV. Connect the 6011A and the 8840A to the UUT FM EXT input.
   a. Edit the 6011A level until the 8840A reads 0.707V rms. Verify on the UUT front panel that the EXT FM LO and the FM HI annunciators are off.
   b. Increase the 6011A output voltage to 0.728V rms as measured on the 8840A. Verify that the EXT FM HI annunciator is on.
   c. Decrease the 6011A output voltage to 0.685V rms as measured on the 8840A. Verify that the EXT FM LO annunciator is on.

10. Set the UUT to SPCL 909, EXT AM. Set the 6011A to 1 kHz and 383 mV. Connect the 6011A and the 8840A to the UUT AM EXT input.
    a. Edit the 6011A level until the 8840A reads 0.707V rms. Verify on the UUT front panel that the EXT AM LO and the AM HI annunciators are off.
    b. Increase the 6011A output voltage to 0.728V rms as measured on the 8840A. Verify that the EXT AM HI annunciator is on.
    c. Decrease the 6011A output voltage to 0.685V rms as measured on the 8840A. Verify that the EXT AM LO annunciator is on.

Alignment of FM PCA (A14) 6E-18.

Align the FM PCA as described in the following procedure:

1. Center all pots on the FM PCA. Turn the UUT off. Set the 6011A to 50 kHz at 0 dBm. Connect the 6011A to TP12. Connect the spectrum analyzer to TP11. Adjust L6 for a minimum 50-kHz level. Remove the 6011A and the analyzer.

2. Set the UUT to SPCL 909, 800 MHz, 62.5-kHz dev, 1-kHz mod rate, INT AC FM. Set the 8840A to ac volts, autorange. Connect the 8840A to TP1 on the FM PCA. Adjust R107 for 2.828V rms ±2 mV rms. Turn INT AC FM off.

3. Remove the cap from J3 to J17 that connects the FM PCA to the A12 Sum Loop PCA. Connect the counter to J3. Adjust L1 to be flush with the top of its housing. Adjust C9 for a locked 80 MHz as read on the counter.

4. Remove the counter from J3 and connect 436A to J3. Adjust R45 for -5 dBm ±0.1 dB. Disconnect 436A from J3. Install the 1000-pF cap from J3 to J17 on the Sum Loop PCA.

5. Connect the 8840A to TP9. Set the 8840A to dc volts. Adjust R44 for 0V dc ±10 mV dc.

6. Cover the FM oscillator (Q1, Q2 section only) with a metal cover.

7. Set the 8901A to Auto, FM, +peak, 300-Hz HP, 15-kHz LP. Connect the 8901A to J3. Set the UUT to SPCL 909, 800 MHz, INT AC FM, 1-kHz mod rate, 400-kHz FM dev. Set 8840A to dc volts, autorange. Connect the 8840A to TP11. Adjust L1 for 400-kHz FM dev ±2 kHz. The 8840A should read 7V dc ±100 mV dc. Set the UUT to 40 kHz FM dev. Adjust C9 for 40 kHz ±0.2 kHz dev. The 8840A should read 15V dc ±200 mV dc. Repeat these steps until both specs are met. Remove the 8840A from TP11.

8. Set the 8840A to dc volts, autorange. Connect the 8840A to TP12. Set the UUT to 300-kHz dev, INT AC FM on, 1-kHz mod rate. Key SPCL 942 to set FM steer dac to 2048. Adjust R39 for 0.0V dc ±20 mV dc.

9. Set the UUT to 200-kHz dev AC FM, INT AC FM on, 1-kHz mod rate. Set the FM steer dac to 2048. Set the 8840A to dc volts, autorange. Connect the 8840A to TP12. Adjust R35 for 0.0V dc ±20 mV dc.

10. Set the UUT to INT AC FM, 10-kHz mod rate. Connect oscilloscope channel 1 to TP8 and channel 2 to TP6. Set the UUT for 200-kHz AC FM. Adjust R63 until one pulse on channel 1 is exactly in the middle of two pulses on channel 2. This represents a 50% alignment of the pulses on TP6 and TP8. Set the UUT to 10-kHz dev AC FM. Check for a pulse alignment of 22/78% ±3%. Remove the scope probes.

11. Set the UUT to INT AC FM, 5-rad ϕM dev, 5-kHz mod rate. Set the 8901A to FM, AVE, 300-Hz HP, 15-kHz LP, %. Note the 8901A reads 100%. Press the kHz button on the UUT. Adjust R104 for a reading of 102% to 102.2% on the 8901A.

12. Set the UUT to 800 MHz, 50-kHz dev, 5-kHz mod rate, INT AC FM. Set the 8901A for +peak, % off, >20-kHz filter, and all other filters off. Adjust R107 for equal plus and minus readings around 50 kHz. Plus and minus readings must be within 0.5 kHz of each other. This is a distortion check.

13. Set the UUT to SPCL 909, 800 MHz, 50-kHz dev, 70-Hz mod rate, int ac FM. Set the 8901A to +peak, >20 kHz filter. Adjust R102 for a 50-kHz reading on the 8901A.

14. Set the UUT to SPCL 909, 800 MHz, 100-kHz dev, 70-Hz mod rate, int ac FM. Set 8901A to +peak, >20-kHz filter, all other filters off. Adjust R94 for a 100-kHz reading on the 8901A.

15. Set the UUT to 50-kHz dev, 5-kHz mod freq, INT AC FM. Set the 8901A to %. The 8901A should read 100%. Check the mod rates in Table 6E-5 to determine if the UUT is within specification.

Table 6E-5. FM Modulation Rate Specifications

MOD RATE (Hz)	SPECIFICATION (kHz)
1000	100 +2% -2%
500	100 +2% -2%
200	100 +2% -2%
100	100 +2% -2%
50	100 +1.5% -1.5%

16. Set the UUT to SPCL 909, 800 MHz, 150-kHz DEV, 25-Hz mod rate, int ac FM. Connect the oscilloscope to the 8901A MOD OUT. Adjust the scope for almost full scale display with one cycle. Adjust R88 for a smooth waveform.

17. Set the UUT to 800 MHz, 5-kHz mod rate, 200-kHz DEV, INT AC FM. Set the 8901A to FM, +peak, 300 Hz HP, 15 kHz LP. Adjust R141 for a 8901A reading of 200 kHz ±1 kHz. Adjust R119 for symmetrical plus and minus readings about 200 kHz ±1 kHz. Repeat until both specs are met.

18. Set the UUT to 200 MHz, 5-kHz mod rate, 200-kHz DEV, INT AC FM. Set the 8901A to FM, +peak, 300-Hz HP, 15-kHz LP. Adjust R140 for a 8901A reading of 200 kHz ±1 kHz. Adjust R117 for symmetrical plus and minus readings about 200 kHz ±1 kHz. Repeat until both specs are met.

19. Set the UUT to 50 MHz, 5-kHz mod rate, 200-kHz dev, INT AC FM. Set the 8901A to FM, +peak, 300-Hz HP, 15-kHz LP. Adjust R139 for a 8901A reading of 200 kHz ±1 kHz. Adjust R115 for symmetrical plus and minus readings about 200 kHz ±1 kHz. Repeat until both specs are met.

20. Set the UUT to 800 MHz, 70-Hz MOD rate, 5-rad dev, INT AC FM. Set the 8901A to ϕM, +peak, 15 kHz LP (all other filters removed), Avg and 70.7%. Adjust R145 for 5 rad.

21. Set the UUT to 800 MHz, 10-kHz mod rate, 5-rad dEV, SPCL 721, INT AC FM. Set the 8901A to ϕM, +peak, 300 Hz HP, >20 kHz LP. Adjust C75 for a 8901A reading of 5 rad. Set the UUT to 1 kHz MOD rate. The 8901A reading must be 5 rad ±0.05 rad.

22. Set the UUT to 800 MHz, 70 Hz MOD rate, 5-rad dev, SPCL 721, INT AC FM. Set the 8901A to ϕM, +peak, no filters, Avg and 70.7%. Adjust R146 for 5 rad. Set UUT to SPCL 720.

23. Connect the 8840A to TP12 and adjust R49 to 0V dc. Connect the 8840A to TP9. Verify that the 8840A reads between -3V dc and +10V dc.

24. Set the UUT to SPCL 909, 800 MHz, -5 dBm, 10 Hz mod freq, 25 kHz FM dev, SPCL 711, SPCL 752. Set the spectrum analyzer to IP, center freq 800.06 MHz, span 100 kHz, ref level -5 dBm, resolution bandwidth 30 kHz, video bandwidth 30 kHz, sweep time 200 ms, log scale 6 dB, trigger free run.

    Set the UUT to INT FM. Set analyzer to span 0 Hz, trigger video. Verify that the droop of the demodulated FM is less than 10%. Set the UUT to EXT DC FM. Verify that the droop of the demodulated dc FM is less than 2%.

25. Set the UUT to 800 MHz, 300-kHz dev, 1-kHz mod rate, EXT AC FM on. Connect the 8840A to TP12 and check that the 8840A reads 0V dc ± 200 mV dc.

    Set the UUT to 200-kHz dev. Check that the 8840A reads 0V dc ±200 mV dc.

26. Set the UUT to 800 MHz, 10-kHz dev, 1-kHz mod rate, EXT AC FM. Place a 600Ω load on the UUT EXT FM input. Connect the 1953A Counter to the UUT output, and set the 1953A to read 800 MHz with 1-Hz resolution.

    Set the UUT to EXT DC FM. The front panel DC FM indicator should light within 1 second. The 1953A should read within 350 Hz of the 800-MHz ac FM frequency. Connect the 8840A to TP12. TP12 should read 0V dc. Connect the 8840A to J1-P3. The 8840A should read between 3V dc and 8V dc.

    Set the UUT to AC FM. Repeat step 25 to verify the performance.

27. Set the UUT to 300-kHz dev. Set the UUT to EXT DC FM. The front panel DC FM indicator should illuminate within one second. The 1953A should read within 500 Hz of the 800-MHz ac FM frequency. Connect the 8840A to TP12. TP12 should read 0V dc. Connect the 8840A to J1-P3. The 8840A should read between 3V dc and 8V dc.

    Set the UUT to AC FM. Repeat step 26 to verify the performance.

Section 6F
Internal Modulation Oscillator

MODULATION OSCILLATOR BLOCK DIAGRAM 6F-1.

Refer to the Modulation Oscillator Block Diagram (Figure 6F-1) to identify the major functional sections and follow the signal paths of the internal modulation oscillator.

INTERNAL MODULATION OSCILLATOR CIRCUIT DESCRIPTION 6F-2.

The modulation oscillator is configurable either as a direct digital synthesizer (DDS) or as a pulse generator. Both functions are implemented in a custom integrated circuit and are synthesized from the main reference frequency source of the instrument.

The A6 Mod Oscillator PCA provides two outputs:

- An internal modulation source (Int Mod)
- A modulation output source (Mod Out), available at the MOD OUTPUT BNC connector on the front panel.

All power, data, control, and clock signals are received by the Mod Oscillator PCA via a bus connector (J1) and clock connector (J2).

Direct Digital Synthesized Wave Generator 6F-3.

The direct digital synthesizer frequency is the modulation source for the internal AM, FM, ϕM, and pulse functions. It can be set from 0.1 Hz to 200 kHz with resolution of 0.1 Hz. The amplitude of the internal modulation source (Int Mod signal) is a leveled 1V pk, internally routed to the A11 Modulation Control PCA. The amplitude of the modulation output is controlled by a level dac. An algorithmic wave generation method provides a very accurate and stable oscillator signal source of high purity and low harmonic distortion.

Custom IC U1 acts as the wave generator by using external wave lookup table U2 and U3, and 12-bit wave reconstruction dac U7 and U9B. A discrete time sample method generates the various waves. A low-pass antialiasing filter made up of R6, R7, C13, C14, and L1 is required to reject the sampling frequency, the alias signals, and the out-of-band spurious signals from the output signal.

The amplitude of oscillation at the MOD OUTPUT connector is controlled by 12-bit multiplying dac U8 and U11A. This output level can be set between 0 and 4V pk, with 1-mV pk steps, into a 600-ohm load.

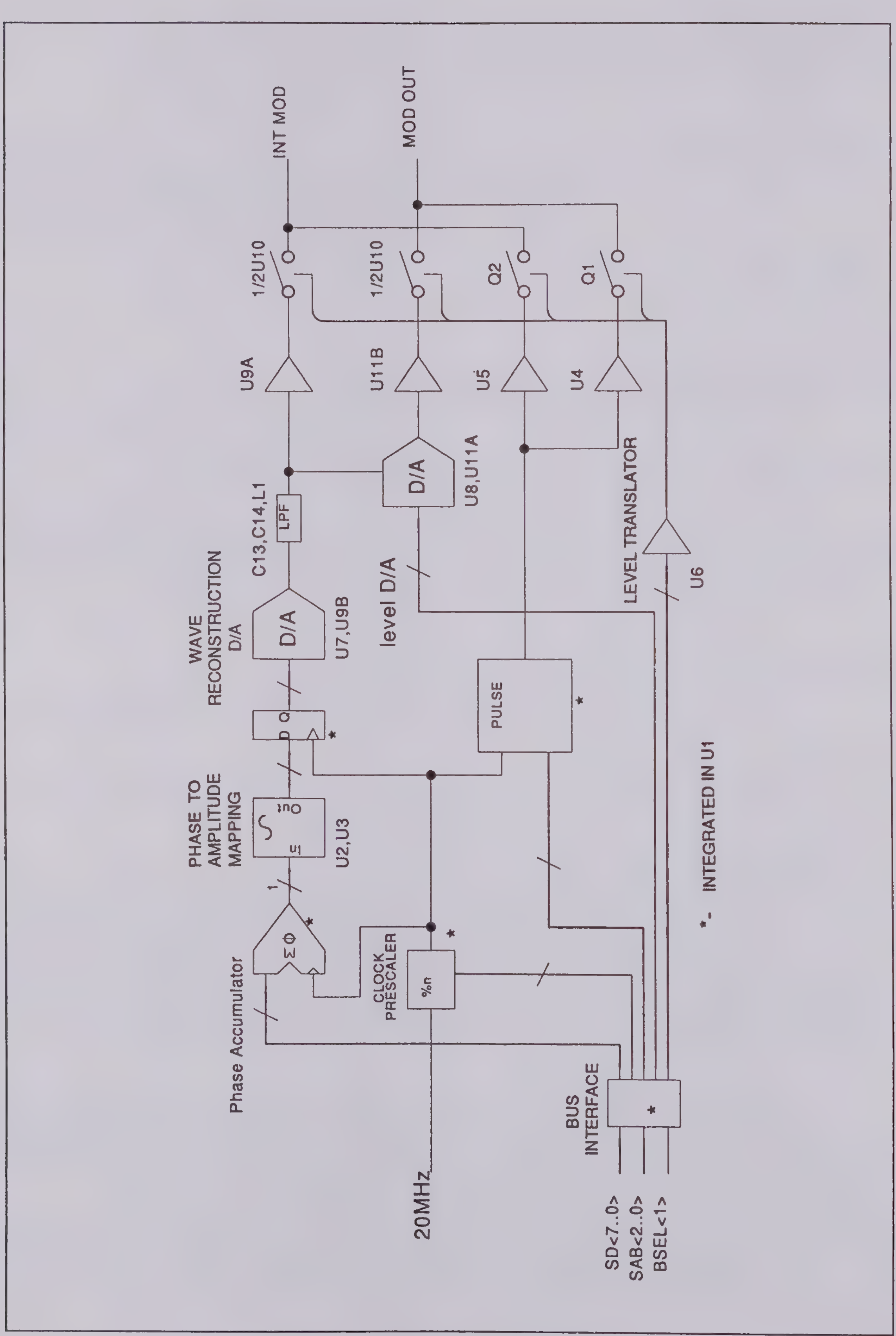

INT MOD
MOD OUT
1/2U10
1/2U10
Q2
Q1
U9A
U11B
U5
U4
D/A
U8,U11A
LEVEL TRANSLATOR
U6
C13,C14,L1
LPF
WAVE RECONSTRUCTION D/A
D/A
U7,U9B
level D/A
PULSE
*
D Q
*
PHASE TO AMPLITUDE MAPPING
U2,U3
Phase Accumulator
ΣΦ
*
CLOCK PRESCALER
%n
*
20MHz
BUS INTERFACE
*
SD<7..0>
SAB<2..0>
BSEL<1>
*- INTEGRATED IN U1

Figure 6F-1. Mod Oscillator Block Diagram

Waveform data is stored in EPROMS U2 and U3. Three control lines from U1 control waveform selection, allowing up to eight waveforms to be selected via a front panel special function. When you select a wave other than the sine wave, make sure you consider the low-pass filter cutoff frequency of 200 kHz. There will be a progressive deterioration of the fidelity of waves with increased frequency, depending on the wave shape selected. This relates to the higher frequency components of the waves other than the sine wave.

Pulse Generator 6F-4.

The pulse generation mode is selected via the front panel or IEEE Special Function commands. The frequency of the pulse generator can be set from 10 Hz to 200 kHz. Frequency and pulse width are determined by numeric values written to the oscillator. The built-in pulse generator can be used as a modulation source for the internal AM, FM, ϕM, and pulse.

The pulse generator is also based on custom IC U1, which contains a programmable period and pulse width sections. Both the period and the pulse width can be set in increments of 100 ns. Internally, the pulse frequency is rounded and set to the nearest 100 ns period increment of the entered modulation frequency.

U4, U5, Q1, Q2, and their associated components condition the external and internal pulse signals. When in the pulse generation mode of operation, the internal pulse at Int Mod is preset to 1V pk via U5. U4 buffers the pulse output of U1 to provide Mod Out, which is fixed at 4.5V CMOS/TTL logic level. Both the frequency and the pulse width are set numerically through front panel entry or via IEEE commands. In pulse generation mode, Mod Out is terminated with a nominal 180Ω.

To avoid the ambiguity of the pulse output from being set to a dc value, the software limits the pulse width to a value that is no wider than the set period minus 100 ns, and the software prevents the pulse width from being set narrower than 100 ns.

See the Special Function list in Appendix B for selections modulation oscillator modes of operations. The appropriate Special Functions allow the selection of direct digital synthesis, output waveform, pulse generator, and pulse width setting. Additionally, by selecting the appropriate special function code, you can enable MOD OUT to be continuously on (default) or to be turned on only during the selection of internal modulation.

Signal Routing 6F-5.

The modulation oscillator selects the active outputs through six analog switches. Signals from U1 control the various switches that route the pulse generator and direct digital synthesizer output signals to the two outputs (Int Mod, Mod Out) of the A6 Modulation Oscillator PCA.

Switches S1 and S2 (associated with U9A, U6A, and U6B) facilitate the connection of the direct digital synthesizer to the internal modulation source (Int Mod).

Switches S3 and S4 (associated with U11B, U6C, and U6D) facilitate the connection of the direct digital synthesizer to the modulation output (Mod Out).

Switches S5 and S6 (associated with U4, U5, U6B, and U6D) facilitate the connection of the pulse generator to both the modulation output (Mod Out) and to the internal modulation source (Int Mod).

MOD OSCILLATOR TROUBLESHOOTING AND ADJUSTMENTS 6F-6.

Since both the direct digital synthesizer and the pulse generator sections are clocked by the same clock, verify the 20 MHz input signal first. The amplitude of this wave should be at least 300 mV p-p. If this clock signal is absent, none of the functions on the assembly will operate.

Direct Digital Synthesizer Troubleshooting 6F-7.

To troubleshoot the direct digital synthesizer (DDS), proceed as follows:

SETTING UP:

1. Select SPCL 909 to set the UUT to the preset default state. This sets the DDS to generate a sine wave.
2. Enable INT AM modulation.
3. Set MOD LEV to a modulation output level of 4V pk.
4. Enter MOD FREQ of 1 kHz.
5. Connect a 600Ω load at the MOD OUTPUT connector.

TEST PROCEDURE:

NOTE

S1-S6 refers to analog switches on the A6 Mod Oscillator.

1. Check U1 output clock CLKO at TP10. This logic level signal should be 3.33 MHz. If there is no signal at this point or if the frequency is wrong, either U1 is faulty, wrong data is written to it, or the 20-MHz signal is inadequate. If this signal is absent, the DDS sections will not operate.
2. Use an oscilloscope to verify that the most significant bit (MSB) of the phase accumulator (TP8) is at TTL level and is 1 kHz (the set modulation frequency). If the MSB is not as indicated, the U2 most significant lookup table, or the U1 phase accumulator section may have failed.
3. Use the oscilloscope to verify the presence of a 10V p-p (±5%) sine wave at the output of the U7 wave reconstruction dac (TP2). If the sine wave is not present, suspect U7 and the dac output amplifier U9A, or wave tables U2 and U3. If the signal is not zero centered or the amplitude is in error, check R4 and R5, also verify 10V ±2% at U7 pin 4.
4. Verify that a 4.77V p-p ±5% sine wave is present at TP3. If the sine wave is not present, or is the wrong amplitude, check the 3-pole low-pass filter components R6, C13, C14, L1 and R7.
5. Enter MOD FREQ of 100 kHz.
6. Repeat step 4 above.
7. Enter MOD FREQ of 1 kHz.

8. Use an oscilloscope to check for a 2V p-p sine wave at TP4. Measure its amplitude with an ac voltmeter and verify that it is 0.7071V rms within ±0.1% (±0.7 mV). If the sine wave is not present or is distorted, check S1 and S2 at U10, and check U9B and its associated components. If the amplitude is slightly off, recalibrate R9 using normal calibration procedures.

9. Use an oscilloscope to verify a 4.66V p-p (±5%) sine wave signal at TP9, and check for visible distortions. If the sine wave is not present, is distorted, or is the wrong amplitude, check level dacs U8, and U11A.

   If U8 and U11A are OK, check for a failed U1, which would cause a write data error. If U1 is operating correctly, check for an interface bus fault.

10. Use an oscilloscope to verify a zero centered 8V p-p sine wave at TP5. If the signal is distorted, check U11B and associated resistors R11, R12, and R13 and switches S3 and S4. With an ac voltmeter, check for 2.8284V rms ±0.1% (±2.8 mV). If the signal not within specifications, recalibrate R13 using normal calibration procedures.

Pulse Generator Troubleshooting 6F-8.

To troubleshoot the pulse generator, proceed as follows:

SETTING UP:

1. Enter SPCL 758 to set the instrument to the preset default state.
2. Enter SPCL 741 to set the instrument to internal pulse operation.
3. Enable INT AM modulation.
4. Enter MOD FREQ of 10 kHz (100 μs period).
5. Enter SPCL 759 to set the pulse width to 25 μs.

TEST PROCEDURE:

NOTE

Modulation level control has no effect in pulse mode.

1. Verify a 10.0-MHz logic signal at TP10. If no signal is present at this point or the signal is the wrong frequency, either U1 has failed, a data write error has occurred, or the 20-MHz signal is inadequate.

2. Use an oscilloscope connected to TP11 to verify that the TTL-level pulse signal from U1 is 10 kHz with a positive pulse width of 25 us. If it is not, U1 may be faulty.

3. Use an oscilloscope to verify that the TTL-level pulse described in step 2 above is present at TP5.

4. Use an oscilloscope to observe TP4 and verify that the same pulse shape described in step 2 is zero centered with an amplitude of 2V ±10% p-p. If either the amplitude or wave shape is incorrect, check U5 and associated resistors R22, R23, R24, and R25.

Section 7
Compensation Procedures

INTRODUCTION 7-1.

The internal software compensation procedures generate the instrument-specific compensation data for the following assemblies:

- A3 Subsynthesizer VCO
- A5 Coarse Loop VCO
- A8 Output
- A9 Sum Loop VCO
- A20 Attenuator/RPP

These procedures must be performed following any repair to the related assembly that affects the compensation. The procedures restore the operating specifications of the Signal Generator provided there are no remaining hardware failures. If the required adjustments exceed the procedure's adjustment limits, the Signal Generator needs to be repaired. Refer to Section 6, "Circuit Descriptions, Troubleshooting, and Alignment" for details. Section 6 explains the Module Exchange Program as well as component-level troubleshooting hints.

LEVEL FLATNESS COMPENSATION 7-2.

The level flatness compensation procedures generate the instrument-specific compensation data for the A8 Output PCA and the A20 Attenuator/RPP Assembly.

Output flatness compensation corrects for frequency-dependent level flatness errors in the A8 Output PCA. The Output Flatness Compensation Procedure (also referred to as the Output Compensation Procedure) involves measuring the level error at up to 60 frequencies, from which correction factors are calculated and stored in the non-volatile compensation memory on the A13 Controller PCA. When an RF frequency is programmed, the correction factors associated with the two nearest frequencies are interpolated to determine the applied level compensation.

The Output Compensation Procedure must be performed following any repair to the A8 Output PCA that affects the output flatness compensation. In addition, there is storage provided for alternate output compensation data that you can use to compensate for an external system without affecting the normal output compensation data. This alternate compensation data corrects for level flatness errors at the output of an external amplifier or at the end of a length of cable. There is typically 1-dB of overrange available for this purpose.

The Output Compensation Procedure requires the use of a power meter, or a measuring receiver in the power meter mode. You can perform the procedure from the front panel or remotely under the control of an IEEE-488 bus controller. It consists of the following steps:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.
2. Connect the power meter sensor to the Signal Generator's RF output.
3. Initiate the compensation procedure.
4. Adjust the RF level until the power meter reading matches the displayed target level for every step in the procedure.
5. Store the updated compensation data.

Attenuator flatness compensation corrects for frequency-dependent level flatness errors in the Attenuator/RPP. The Attenuator Flatness Compensation Procedure (also referred to as the Attenuator Compensation Procedure) involves measuring the level error for each attenuator section at up to 29 frequencies, from which the correction factors are calculated. When an RF frequency or amplitude is programmed, the correction factors associated with the two nearest frequencies for the programmed RF level are interpolated to determine the applied level compensation. The attenuator compensation procedure must be performed following a repair to the Attenuator/RPP that affects the attenuator flatness compensation.

The Attenuator Flatness Compensation Procedure must be performed using a measuring receiver in order to guarantee the level flatness specification. An alternate procedure may be performed using a power meter, but this procedure does not guarantee compliance with the flatness specification. You can perform the procedure from the front panel or remotely under the control of an IEEE-488 bus controller. It consists of the following steps:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.
2. Lock the measuring receiver and Signal Generator references together.
3. Connect the measuring receiver sensor module to the Signal Generator's RF output.
4. Initiate the compensation procedure.
5. For each of the frequency steps in the procedure, tune the measuring receiver to match the Signal Generator frequency. For the first three level settings at the frequency step, measure the RF level using the power meter mode of the measuring receiver. Adjust the RF level of the signal generator until the measuring receiver reading matches the displayed target level.

6. For the remaining level settings at the frequency step, measure the RF level in tuned RF mode. If the frequency is below 2.5 MHz, the measuring receiver must be used in power meter mode. Irrespective of the measurement mode, adjust the Signal Generator level until the measuring receiver reading matches the displayed target level.
7. If the frequency step in the procedure is above a specified 'break frequency', the effects of VSWR are significant in the level measurement. Thus, additional level measurements and adjustments must be made using combinations of attenuators to reduce VSWR effects. In making these measurements, care must be taken to ensure that the measuring receiver calibration is transferred correctly through its level bands as successively lower RF levels are measured.
8. Repeat steps 5, 6, and 7 for every frequency step in the procedure.
9. Store the updated compensation data.

Level Flatness Compensation Accuracy Notes 7-3.

Proper use of the level compensation procedures will restore the operating specifications of the Signal Generator. You can verify level accuracy by doing the "High-Level Accuracy Test", "Mid-Level Accuracy Test", and "Low-Level Accuracy Test", or the "Alternate Level Accuracy Test" in Section 3.

Failure to observe the following guidelines may result in less than optimal or out-of-specification operation:

- The measuring receiver and sensor module must be calibrated and operated according to its manufacturer's instructions. The calibrated measuring receiver and sensor module combination must yield 0.05-dB measurement accuracy or better.
- The power meter and sensor must be calibrated and operated according to its manufacturer's instructions. The frequency-dependent power meter calibration factors must be set for each frequency. The calibrated power meter/sensor combination must yield 0.05-dB measurement accuracy or better. The meter must be zeroed whenever a procedure calls for this to be done.
- Both the output and attenuator level measurements must be made with the measuring receiver sensor module connected at the RF OUTPUT connector. Do not use a length of cable between the RF OUTPUT connector and the power sensor unless you are intentionally correcting for losses in the cable.

Level Flatness Compensation Limits 7-4.

The maximum compensation allowed for the output section is 4.0 dB. The maximum compensation allowed for the 6080A attenuator section is 6.0 dB.

The measured output corrections are normalized before being stored to remove any fixed level offsets. The 4.0-dB limit is checked after the measurements are normalized so it is possible to make adjustments greater than 4.0 dB as long as the range of values does not exceed 4.0 dB. The measured data cannot be stored if the limit is exceeded. Any offset removed by the normalization process must be eliminated by adjusting the main level adjustment potentiometer R20, on the A11 Modulation Control PCA, after the procedure is complete.

The maximum output compensation allocation allows approximately 1 dB of margin over typical usage. You can put this additional range to use when compensating an external system. If measurements taken at the front panel RF connector exceed the maximum limit, suspect a faulty or misaligned output section. Refer to the related paragraphs in Section 6 of this manual.

The measured attenuator corrections are normalized then summed into all programmable attenuator combinations before being stored. The compensation limit of 6.0 dB is the maximum allowed for any combination of attenuators. This makes it difficult to tell if the maximum allocation will be exceeded until all measurements have been completed. The measured data cannot be stored if the maximum allocation has been exceeded for any combination of attenuators. If the maximum allocation has been exceeded, suspect a faulty attenuator section. Refer to the related paragraphs in Section 6 of this manual.

If the output and attenuator circuits are operating correctly but the maximum compensation allocations have been violated, and a level flatness compensation procedure has been previously performed, there may be excessive mixing of the output and attenuator compensation data. Refer to “Level Compensation Data Mixing”, below.

Level Compensation Data Mixing 7-5.

The A8 Output and A20 Attenuator assemblies are compensated separately during the manufacturing process. Upon receipt from the Fluke factory, the output compensation data only corrects for errors in the output circuitry, and the attenuator compensation data only corrects for errors in the attenuator circuitry.

Measurements made during the user output and attenuator compensation procedures are made at the front panel RF OUTPUT connector. The measured level includes errors from both the output and attenuator circuits. Therefore, performing an output compensation procedure may correct for some errors in the attenuator circuitry, and performing an attenuator procedure may correct for errors in the output circuitry.

The resultant mixing of the correction data usually has a negligible effect. Mixing of this data may cause problems if an Output or Attenuator Compensation Procedure is performed improperly, or is used to compensate misaligned hardware. As a result, there may be measurement points that contain excessively large or unusually small correction values. There may be sufficient correction range to complete the procedure successfully. However, subsequent compensation procedures may fail.

For example, assume that in a 6080A at 1056 MHz, the output circuitry requires 3 dB of correction and the attenuator circuitry requires 5 dB of correction. An Output Compensation Procedure is performed improperly so that a 1-dB correction is stored at 1056 MHz instead of the expected 3 dB correction, resulting in a 2 dB error. The 4-dB limit for the output procedure is not violated so the procedure is completed successfully. At a later time, an Attenuator Compensation Procedure is attempted. To reach the target level at 1056 MHz, the attenuator procedure must apply the expected 5 dB of correction plus an additional 2 dB to correct for the error in the output data. The 6-dB limit for the 6080A attenuator procedure is violated and the data cannot be stored even though both the output and attenuator circuits are operating properly.

Errors due to mixing the correction data rarely occur when you exercise reasonable care. If the problem does arise, use the Output Compensation Procedure with Default Attenuator Data to reduce the mixing. Refer to "Front Panel Output Compensation with Default Attenuator Data," further on in this section.

Replacement Output and Attenuator modules from the Module Exchange Center (MEC) are compensated separately during the manufacturing process. If the current Output and Attenuator data was generated by the Fluke Factory, an Output or Attenuator module exchange PROM can be uploaded without performing any compensation procedures. If an output compensation procedure was performed prior to the installation of an attenuator MEC assembly, it may be necessary to perform an output compensation procedure. Alternately, if an attenuator compensation procedure was performed prior to the installation of a new Output module, it may be necessary to perform an attenuator compensation procedure.

To determine where data in the compensation memory originated, use Special Function SPCL 05.

If all data was generated by the Fluke factory, the status code 00 is displayed. If any of the data was generated in any other way, a status code or list of status codes are displayed. Press STATUS to scroll through the list if there are more than three status codes. Refer to Appendix F, "Compensation Memory Status Codes".

Front Panel Output Flatness Compensation Procedure 7-6.

REQUIREMENTS:

- Adjustment Range: up to 4.00 dB
- Adjustment Resolution: 0.01 dB
- Target Level: 10.0 dBm
- Number of Measurement Steps: One per frequency (up to 60 frequencies).

TEST EQUIPMENT:

- RF Power Meter (HP 436A or equivalent)
- Power Sensor (HP 8482A or equivalent)

REMARKS:

See Table 7-1 for front panel controls for Output Flatness Compensation Procedure. You initiate the front panel output flatness compensation procedure is by pressing the following key sequence: [SPCL][9][8][1].

Table 7-1. Front Panel Controls for Output Flatness Compensation Procedure

CONTROLS	FUNCTION AND DESCRIPTION
[◁] [▷]	BRIGHT DIGIT EDITING
KNOB	Turn edit knob to increment or decrement the level adjustment. Use the left/right arrow keys to move the bright digit.
[ON/OFF]	RF ON/OFF Toggles the RF output on/off.
[STATUS]	OVERRANGE/UNCAL or REJECTED ENTRY STATUS Normally displays the overrange/uncal status. Displays the rejected entry status code if there is a rejected entry.
[STO]	STORE MEASURED DATA Press once, the prompt "Sto ?" is displayed. Press again to store the data. "-- Sto --" is displayed for approximately 10 seconds while the data is stored. Attempts to store the data before all steps have been measured will be rejected with error code 92. Attempts to store data with out of limit conditions will be rejected with error code 93. Press any other key to cancel the store operation and resume the procedure.
CAUTION **Do not turn the power off or change the CAL|COMP switchuntil the store operation is complete. Doing so coulddamage the contents of the compensation memory.**	
[CLR|LCL]	ABORT THE PROCEDURE Press the key once, the prompt "Clr ?" is displayed. Press the key again to abort the procedure. "-- Clr --" is displayed to confirm the selection. All measured data is discarded and the previous instrument state is restored. Press any other key to resume the procedure.

The target RF level of 10 dBm is displayed in the MODULATION field, the RF frequency is displayed in the FREQUENCY field and the level adjustment is displayed in the AMPLITUDE field. The frequencies may vary from instrument to instrument.

The RF level is adjusted using the edit knob until the measured level at the RF output is 10 dBm at each of up to 60 frequencies. This procedure typically takes 15 minutes to perform. The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this procedure.

PROCEDURE:

Proceed as follows to execute the Front Panel Output Flatness Compensation Procedure:

1. Press SPCL 0 1, then program 350 MHz and +9 dBm.

2. Disable the Signal Generator's RF output, and connect the power sensor to the RF output.

3. Zero the power meter and select the power meter calibration factor. Enable the RF output.

4. Measure the RF level.

   If it is more than +9.0 dBm ±1.0 dB, the A8 Output PCA or A20 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.

5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Press SPCL 9 8 1 to initiate the Output Compensation Procedure. Verify that COMP and OUT annunciators are lit.

7. Set the CAL factor on the power meter for the displayed frequency.

8. Use the edit knob to adjust the level until the the power meter reads 10 dBm.

9. Press STEP △ to go to the next frequency step.

10. Repeat steps 7 through 9 until the last frequency step has been completed (a frequency 1056 MHz). At this point, pressing the STEP △ key causes the message "End" to be displayed.

11. Press the STO key twice to store the data.

NOTE

If the store operation is rejected (flashing "—Sto—"), press STATUS *to determine the cause of the rejected entry. Refer to the list of rejected entry error codes in Appendix C. Also refer to "Level Flatness Compensation Limits", "Level Compensation Data Mixing", "Het Band Level Adjustment" in this section.*

12. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:
    a. Enter [SPCL][9][9][3].
    b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.
    c. Press [STO] twice to store the new calibration factor.
13. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.
14. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.
15. Press [SPCL][0][1], then program 350 MHz and +9 dBm.
16. Disable the Signal Generator RF output, zero the power meter, then enable the RF output. Select the power meter calibration factor.
17. Adjust RF level adjustment at A11R20 for a reading of exactly +9 dBm on the power meter.
18. Replace the RF level adjustment access screw and the bottom instrument cover.

Het Band Level Adjustment 7-7.

A store operation at the end of an Output Compensation procedure can fail because the Het Band level is not adjusted properly. When a store operation is rejected with error 93 (too much correction), exit the procedure and perform the following steps.

1. Enter [SPCL][9][8][9], and note the frequency displayed in the FREQUENCY field, and the amplitude adjustment displayed in the AMPLITUDE field.
2. Program the 6080A to the frequency displayed in the FREQUENCY field and +10.0 dBm.
3. Program the power meter with the calibration factor that corresponds with the frequency displayed in the FREQUENCY field.
4. Adjust the Het Level Adjustment A8R72 by the amount displayed in the AMPLITUDE field.
5. Perform the output compensation procedure again.

The default attenuator data may not accurately characterize the current state of the attenuator circuitry. However, it will have a typical distribution and should allow the procedure to be performed successfully regardless of the amount of mixing in the normal compensation data. Upon completion, the Attenuator Compensation Procedure must be performed to restore the instrument specifications.

The process is identical to the Output Compensation Procedure except that it initiated by special function 983. Refer to "Front Panel Output Flatness Compensation Procedure" next in this section.

Front Panel Attenuator Flatness Compensation Procedure 7-10.

REQUIREMENTS:

- Adjustment Range: up to 6.00 dB
- Adjustment Resolution: 0.01 dB
- Target Levels: 10.0 dBm, 4.0 dBm, -2.0 dBm, -14.0 dBm, -38.0 dBm, -44.0 dBm, -50.0 dBm, -62.0 dBm
- Number of Frequency Steps: Up to 29
- Number of Measurement Steps: 8 per frequency (fc < 850 MHz typical) 14 per frequency (fc >= 850 MHz typical)

TEST EQUIPMENT:

- RF Measuring Receiver (HP 8902 or equivalent)

REMARKS:

You initiate the front panel attenuator flatness compensation procedure by pressing the following key sequence: SPCL 9 8 2.

The target RF level is displayed in the MODULATION field, the RF frequency is displayed in the FREQUENCY field and the level adjustment is displayed in the AMPLITUDE field. The frequencies may vary from instrument to instrument.

The RF level is adjusted using the edit knob until the measured level at the RF output matches the target level. This sequence is repeated for each attenuator section (the through-path, and each of seven attenuators) at up to 29 frequencies. Additionally, six combinations of attenuators are measured for frequencies typically above 850 MHz.

NOTE

The Front Panel Attenuator Compensation Procedure may take up to two and one half hours to perform. Exercise care to ensure that the measured value matches the target value for every measurement step. Failure to do so may result in not meeting performance specifications.

Compensating Level Flatness Errors in an External System 7-8.

The Output Flatness Compensation Procedure corrects for level flatness errors in an external system connected to the Signal Generator RF output. Compensation for losses attributable to the external system can be applied up to the specified limits of the Output Compensation Procedure. There is typically 1 dB of overrange available for this purpose.

Proceed as follows to compensate an external system:

1. Connect the input of external system to the RF output of the 6080A and connect the power meter sensor to the RF output of the external system.
2. Select the alternate output compensation data by entering: SPCL 9 3 1
3. Perform the "Output Flatness Compensation Procedure" as described earlier in this section.

NOTE

It is not necessary to set the CAL|COMP switch to the 1 (on) position as specified in the Output Flatness Compensation Procedure when the alternate output compensation data has been selected by special function 931.

While Special Function 931 is enabled, compensation data generated by the Output Flatness Compensation Procedure is stored in a separate location, leaving the normal output compensation data unchanged. Subsequent frequency programming operations use the alternate output compensation data. Enter Special Function 930 to select the normal output compensation data.

After the alternate output compensation data has been generated, Special Functions 930 and 931 can be used to switch between the normal and alternate data as desired. The special function setting is retained while the instrument power is off and is not affected by instrument preset or memory recall operations.

NOTE

The alternate output compensation data is set to 0 dB of correction when the 6080A is manufactured. If any alternate data are stored, they are set to 0 dB if the memory erase function (SPCL 8 2 9) is executed. See Section 4D of the Operator Manual for more information on the memory erase function.

Front Panel Output Compensation with Default Attenuator Data 7-9.

The Output Compensation Procedure with Default Attenuator Data may be used to reduce the mixing of the output and attenuator compensation data. In this procedure, the compensation data for the A8 Output PCA is generated while the attenuator circuitry is compensated using the last Fluke Factory or module exchange data for the attenuator circuit.

The target RF output level displayed in the MODULATION field is determined by the attenuator section(s) to be measured. Table 7-2 lists the target levels.

Table 7-2. Attenuator Target Levels

ATTENUATOR	TARGET LEVEL
Through-path	10 dBm
6 dB	4 dBm
12 dB	-2 dBm
24a	-14 dBm
24b	-14 dBm
24c	-14 dBm
24d	-14 dBm
24e	-14 dBm
24a + 24b	-38 dBm
24a + 24b + 6 dB	-44 dBm
24a + 24b + 12 dB	-50 dBm
24a + 24b + 24c	-62 dBm
24a + 24b + 24d	-62 dBm
24a + 24b + 24e	-62 dBm

Table 7-3 summarizes the operation of the front panel keys used during the Front Panel Attenuator Flatness Compensation Procedure. All other keys are ignored.

NOTE

The 6080A rear panel REF switch must be set to EXT, and the external reference input must be connected to the measuring receiver's REF OUT connector.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

PROCEDURE:

Proceed as follows to execute the Front Panel Attenuator Flatness Compensation Procedure:

1. Press SPCL 0 1, then program 1 MHz, +10.0 dBm, and SPCL 9 2 2 to disable attenuator output compensation. Note that the STATUS annunciator is lit. Press STATUS, status code 201 (Level Correction Disabled) should be displayed.

2. Disable the Signal Generator's RF output and connect the sensor module to the RF output.

Table 7-3. Front Panel Controls for Attenuator Flatness Compensation Procedure

CONTROLS	FUNCTION AND DESCRIPTION
◁ ▷	BRIGHT DIGIT EDITING
KNOB	Turn edit knob to increment or decrement the level adjustment. Use the left/right arrow keys to move the bright digit.
ON/OFF	RF ON/OFF Toggles the RF output on/off.
STATUS	OVERRANGE/UNCAL or REJECTED ENTRY STATUS Normally displays the overrange/uncal status. Displays the rejected entry status code if there is a rejected entry.
STO	STORE MEASURED DATA Press the key once, the prompt "Sto ?" is displayed. Press the key again to store the data. "-- Sto --" is displayed for approximately 30 seconds while the data is stored. Attempts to store the data before all steps have been measured will be rejected with error code 92. Attempts to store data with out of limit conditions will be rejected with error code 93. Press any other key to cancel the store operation and resume the procedure.
	CAUTION **Do not turn the POWER switch off or change the CAL COMPswitch until the store operation is complete. Doing socould damage the contents of the compensation memory.**
CLR|LCL	ABORT THE PROCEDURE Press the key once, the prompt "Clr ?" is displayed. Press the key again to abort the procedure. "-- Clr --" is displayed to confirm the selection. All measured data is discarded and the previous instrument state is restored. Press any other key to resume the procedure.

3. Tune the measuring receiver to 1 MHz, select the power meter mode, and zero the measuring receiver. Enable the RF output.

4. Measure the RF level.

   If it is more than +10.0 dBm ±0.5 dB, the A8 Output PCA or A21 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.

5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Press [SPCL][9][8][2] to initiate the Attenuator Flatness Compensation Procedure. Verify that the COMP and ATT annunciators are lit.

7. Tune the measuring receiver to the displayed frequency. For the first target level (10 dBm) at the tuned frequency, select the power meter mode of the measuring receiver. Zero the measuring receiver.

8. Use the edit knob to adjust the level until the measuring receiver reading matches the target level.

9. Press STEP [△] to go to the next measurement target level. For this level (4 dBm) and the following target level (-2 dBm) use the measuring receiver in the power meter mode and repeat the adjustment described in step 8. Note that for levels below 0 dBm, the level reading on the measuring receiver in power meter mode does not respond instantaneously to changes in the Signal Generator level, and when finally settled, the receiver may have ±0.01 dB jitter.

10. After completing the measurement and adjustment of the 10, 4, and -2 dBm levels, press STEP [△] to go to the next measurement target level (first of five -14 dBm levels). For this level and all subsequent level measurements at this frequency, the measuring receiver must be operated in tuned RF mode (unless the displayed frequency is less than 2.5 MHz, in which case the remaining level measurements must be made in the power meter mode). This requires that you transfer the calibration across the level bands of the measuring receiver. The measuring receiver indicates a need to do this by lighting a RECAL annunciator; the transfer is accomplished by pressing the CALIBRATE button on the front panel of the measuring receiver. When the transfer is complete, the RECAL annunciator turns off. You should always press CALIBRATE after entering the tuned RF mode.

NOTE

Details of the measuring receiver recalibration process are beyond the scope of this procedure. Refer to the measuring receiver operator manual for this information.

11. Use the edit knob to adjust the level until the measuring receiver reading matches the target level. Press STEP [△], and repeat the adjustment for the remaining four -14 dBm target levels.

12. If the displayed frequency is above the 'break frequency' (typically 850 MHz), level measurements and adjustments must be performed for six additional target levels (-38 dBm, -44 dBm, -50 dBm, and three at -62 dBm). These levels are measured in the tuned RF mode, using the edit knob to adjust the level, and the STEP [△] to advance the next target level. Again, you should watch for the RECAL annunciator on the measuring receiver, and press the CALIBRATE button when it appears.

13. On some occasions, when attempting measure target power levels that are near the lower end measuring receiver's level band breaks, the measuring receiver may become uncalibrated (UNCAL annunciator is lit). This is usually due to compound effects of losses in the measurement path. To recalibrate the measuring receiver under these circumstances, it is necessary to boost the 6080A level so that it can be measured in the desired band. To do this, use the edit knob to adjust the level up on the Signal Generator until the UNCAL and the RECAL annunciators go out. Then, use the edit knob to lower the signal level until the RECAL annunciator is lit on the measuring receiver. At this point, perform the measuring receiver recalibration as described in step 12.

14. Repeat steps 7 through 13 until the last measurement step (third -62 dBm target level at frequency of 1056 MHz) has been completed. At this point, pressing the STEP [△] key causes the message "End" to appear in the display.

15. Press the [STO] key twice to store the data.

NOTE

If the store operation is rejected (flashing "—Sto—"), press [STATUS] *to determine the cause of the rejected entry. Refer to the list of rejected entry error codes in Appendix C. Also refer to paragraph "Level Flatness Compensation Limits" and "Level Compensation Data Mixing" earlier in this section.*

16. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:

    a. Enter [SPCL][9][9][3]

    b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.

    c. Press [STO] twice to store the new calibration factor.

17. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.

18. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.

19. Program [SPCL][0][1], 350 MHz and +9.0 dBm

20. Tune the measuring receiver to 350 MHz, disable the RF output, select the power meter mode, zero the measuring receiver, then enable the RF output.

21. Adjust RF level adjustment at A11R20 for a reading of exactly +9 dBm on the measuring receiver.

22. Replace the RF level adjustment access screw, and the instrument bottom cover.

Front Panel Attenuator Flatness Compensation Procedure Using Power Meter 7-11.

REQUIREMENTS:

- Adjustment Range: up to 6.00 dB
- Adjustment Resolution: 0.01 dB
- Target Levels: 10.0 dBm, 4.0 dBm, -2.0 dBm, -14.0 dBm
- Number of Measurement Steps: 8 per frequency (up to 29 frequencies).

TEST EQUIPMENT:

- RF Power Meter (HP 436A or equivalent)
- Power Sensor (HP 8482A or equivalent)

NOTE

Use of this Procedure does not guarantee compliance with the 6080A level accuracy specification over temperature. For the best obtainable results, use the procedure in section 7-9. The following procedure gives good results with much less test equipment and in less time.

You initiate the front panel attenuator flatness compensation procedure using power meter by pressing the following key sequence: SPCL 9 8 8 .

The target RF level is displayed in the MODULATION field, the RF frequency is displayed in the FREQUENCY field and the level adjustment is displayed in the AMPLITUDE field. The frequencies may vary from instrument to instrument.

The RF level is adjusted using the edit knob until the measured level at the RF output matches the target level. This sequence is repeated for each attenuator section (seven attenuators plus the through-path) at up to 29 frequencies.

NOTE

This procedure may take up to 1 hour to perform. Exercise care to ensure that the measured value matches the target value for every measurement step. Failure to do so may result in poor Signal Generator performance.

The target RF output level displayed in the MODULATION field is determined by the attenuator section being measured. Table 7-4 lists the target levels.

Table 7-4. Attenuator Target Levels (Power Meter Procedure)

ATTENUATOR	TARGET LEVEL
Through-path	10 dBm
6 dB	4 dBm
12 dB	-2 dBm
24a	-14 dBm
24b	-14 dBm
24c	-14 dBm
24d	-14 dBm
24e	-14 dBm

Table 7-3 summarizes the operation of the front panel keys used during the Front Panel Attenuator Flatness Compensation Procedure. All other keys are ignored.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this procedure. Proceed as follows to execute the Front Panel Attenuator Flatness Compensation Procedure Using Power Meter:

1. Press SPCL 0 1, then program 1 MHz, +10.0 dBm, and SPCL 9 2 2.

2. Zero the power meter and select the power meter calibration factor.

3. Connect the power sensor to the Signal Generator's RF output.

4. Measure the RF level.

   If it is more than +10.0 dBm ±0.5 dB, the A8 Output PCA or A21 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.

5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Press SPCL 9 8 8 to initiate the Attenuator Flatness Compensation Procedure. Verify that the COMP and ATT annunciators are lit.

7. Disable the RF output, zero the power meter, then enable the RF output.

8. Set the frequency dependent CAL factor on the power meter at each new frequency (target level of 10 dBm).

9. Use the edit knob to adjust the level until the power meter reading matches the target level.

10. Press STEP △ to go to the next measurement step.

11. For the first 24-dB attenuator at each frequency (target level of -14 dBm), the power meter must be zeroed.

12. Repeat steps 8 through 11 until the last measurement step (fifth 24-dB attenuator at frequency of 1056 MHz) has been measured. At this point, pressing the STEP △ key causes the message "End" to be displayed.

13. Press the STO key twice to store the data.

NOTE

If the store operation is rejected (flashing "—Sto—"), press STATUS *to determine the cause of the rejected entry. Refer to the list of rejected entry error codes in Appendix C. Also refer to paragraph 7-4, "Level Flatness Compensation Limits" and paragraph 7-5, "Level Compensation Data Mixing".*

14. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:

    a. Enter SPCL 9 9 3

    b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.

    c. Press STO twice to store the new calibration factor.

15. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.

16. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.

17. Program SPCL 0 1, 350 MHz and +9.0 dBm

18. Disable the RF output, zero the power meter, then enable the RF output. Select the power meter calibration factor.

19. Adjust RF level adjustment at A11R20 for a reading of exactly +9 dBm on the power meter.

20. Replace the RF level adjustment access screw, and the instrument bottom cover.

REMOTE LEVEL FLATNESS COMPENSATION PROCEDURES 7-12.

The remote level compensation procedures allow the output and attenuator compensation data to be generated in a totally automated station. The sole function of the controller software is to obtain valid readings from the measurement equipment and convert them into a format understood by the 6080A. It must ensure that every reading is settled and valid before sending it to the 6080A.

Remote Output Compensation Procedures 7-13.

The structure of an output flatness compensation program is outlined in Figure 7-1. A complete listing of a program that runs on a Fluke 1722A controller is in Appendix G.

```
initiate the Output Compensation Procedure with "COMP_OUT"
      or the Output with Default Attenuator Procedure with "COMP_OUTDEF"
initialize power meter
zero power meter

MAIN_LOOP:
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    request the target level with "CC_TARGET?"
    read power meter
    send reading to 6080A with "CC_RDPOWER"

    goto MAIN_LOOP

DONE:
store new data in compensation memory with "CC_SAVE"
end
```

Figure 7-1. Basic Structure of an Output Compensation Program

The programming commands used in a remote output compensation procedure are listed in Table 7-4. Refer to Section 5B in the 6080A/82A Operator Manual for complete syntax descriptions of each command.

The output compensation procedure is initiated with the command COMP_OUT, or COMP_OUTDEF. After initializing the power meter, the controller requests the Signal Generator's RF frequency with the command CC_FREQ? and waits for a response. When a response is received, it gets a power meter reading and sends it to the Signal Generator with the command CC_RDPOWER. It remains in the main loop until the Signal Generator returns the end code "9E+09, HZ" in response to the CC_FREQ? command. The main loop is then exited and the data is saved with the CC_SAVE command.

The controller queries the Signal Generator's RF frequency at each step to synchronize its actions with the Signal Generator and to determine when the procedure is complete. When the Signal Generator receives a reading, it updates its internal settings and does not respond to the next frequency query until it is ready for another reading. This forces the controller to wait for the Signal Generator's output to settle before it is allowed to take another reading.

When the controller receives two consecutive readings within 0.01 dB of the target level, it considers the displayed adjustment value correct and cycles to the next step.

The controller program must ensure that each power meter reading is settled before sending it to the 6080A. In addition, the frequency dependent power meter calibration factor must be applied to every reading. The program listing in Appendix G uses a simple but effective method to obtain valid power meter readings.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

Proceed as follows to execute the Remote Output Compensation Procedure:

1. Press [SPCL][0][1], then program 350 MHz and +9 dBm.
2. Zero the power meter and select the power meter calibration factor.
3. Connect the power meter sensor to the Signal Generator's RF output.
4. Measure the RF level.

   If it is more than +9.0 dBm ±1.0 dB, the A8 Output PCA or A20 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.
5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Run the controller program.
7. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:
   a. Enter [SPCL][9][9][3]
   b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.
   c. Press [STO] twice to store the new calibration factor.
8. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.

9. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.

10. Press [SPCL] [0] [1], then program 350 MHz and +9 dBm.

11. Disable the RF output, zero the power meter, then enable the RF output. Select the power meter calibration factor.

12. Adjust RF level adjustment at A11R20 for a reading of exactly +9 dBm on the power meter.

13. Replace the RF level adjustment access screw and the bottom instrument cover.

Remote Attenuator Compensation Procedure 7-14.

The structure of an attenuator flatness compensation program is outlined in Figure 7-2. A complete listing of a program that runs on a Fluke 1722A controller is in Appendix G.

```
initiate the Attenuator Compensation Procedure with "COMP_ATT"

initialize measuring receiver

MAIN_LOOP:
    request the RF frequency with "CC_FREQ?"
    if( frequency = 9e9) goto DONE

    recalibrate measuring receiver if needed
    request the target level with "CC_TARGET?"

    if target level > -14 dBm or frequency < 2.5 MHz
        read measuring receiver in power meter mode
        send reading to 6082A with "CC_RDPOWER"
    endif

    if target level <= -14 dBm and frequency >= 2.5 MHz
        read measuring receiver in tuned RF mode
        send reading to 6082A with "CC_RDPOWER"
    endif

    goto MAIN_LOOP

DONE:
store new data in compensation memory with "CC_SAVE"
end
```

Figure 7-2. Basic Structure of an Attenuator Level Compensation Program

The attenuator compensation procedure is initiated with the command COMP_ATT. After initializing the measuring receiver, the controller requests the Signal Generator's RF frequency with the command CC_FREQ? and waits for a response. When a response is received, it tunes the measuring receiver to the selected frequency, gets a power meter reading and sends it to the Signal Generator with the command CC_RDPOWER. It continues to make measurements in the power meter mode until the first 24-dB attenuator is measured. At or below this level, all readings are made in the tuned RF mode.

To do this, the controller must query the target level at each step and switch to the tuned RF mode when it detects the transition from the 12-dB attenuator (target level -2 dBm) to the first of the five 24-dB attenuators (target level -14 dBm). The controller must recalibrate the measuring receiver at this transition, and as necessary at lower levels. The sample program performs all calibration transfers before making measurements at the given frequency to avoid conflicts between the target levels and the calibration levels.

The controller proceeds through each of the frequency steps until the signal generator returns the end code "9E+09, HZ" in response to the CC_FREQ? command. The main loop is then exited and the data is saved with the CC_SAVE command.

The controller queries the Signal Generator's RF frequency at each step to synchronize its actions with the Signal Generator and to determine when the procedure is complete. When the Signal Generator receives a reading, it updates its internal settings and does not respond to the next frequency query until it is ready for another reading. This forces the controller to wait for the Signal Generator's output to settle before it is allowed to take another reading.

When it receives two consecutive readings within 0.01 dB of the target level, it considers the displayed adjustment value correct and cycles to the next step.

The division of responsibility between the controller and Signal Generator allows measurement equipment from various manufacturers to be used. Adding a different meter to the system requires only that a new driver module be written for the controller.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

Proceed as follows to execute the Remote Attenuator Flatness Compensation Procedure:

1. Press SPCL 0 1, then program 1 MHz, +10.0 dBm, and SPCL 9 2 2. Note that the STATUS annunciator is lit. Press STATUS , status code 201 (Level Correction Disabled) should be displayed.

2. Turn off the Signal Generator's RF output. Connect the the power sensor to the RF output.

3. Tune the measuring receiver to 1 MHz, select power meter mode, and zero the measuring receiver. Turn the RF output on.

4. Measure the RF level.

   If it is more than +10.0 dBm ±0.5 dB, the A8 Output PCA or A20 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.

5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Run the controller program.
7. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:
   a. Enter SPCL 9 9 3
   b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.
   c. Press STO twice to store the new calibration factor.
8. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.
9. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.
10. Program SPCL 0 1, 350 MHz and +9.0 dBm
11. Disable the RF output, zero the power meter, then enable the RF output. Select the power meter calibration factor.
12. Adjust RF level adjustment, R20 on the A11 Modulation Control PCA, for a reading of exactly +9 dBm on the power meter.
13. Replace the RF level adjustment access screw, and the instrument bottom cover.

7-15. Remote Attenuator Compensation Procedure Using Power Meter

The basic structure of the attenuator compensation program using a power meter is shown in the program outline in Figure 7-3. A complete listing of a program that runs on a Fluke 1722A controller is in Appendix G.

NOTE

Use of this Procedure does not guarantee compliance with the 6080A level accuracy specification over temperature. For the best obtainable results, use the procedure under the heading "Remote Attenuator Compensation Procedure." The following procedure gives good results with much less test equipment and in less time.

```
initiate the Attenuator Compensation Procedure with Power Meter
    with "COMP_ATTPMTR"
initialize power meter
zero power meter

MAIN_LOOP:
    request the RF frequency with "CC_FREQ?"

    if( frequency = 9e9) goto DONE

    request the target level with "CC_TARGET?"
    if( measuring 1st 24-dB pad )
        zero power meter

    read power meter
    send reading to 6080A with "CC_RDPOWER"

    goto MAIN_LOOP

DONE:
store new data in compensation memory with "CC_SAVE"
end
```

Figure 7-3. Basic Structure of an Attenuator Compensation Program Using Power Meter

The programming commands used in a remote level flatness compensation procedures are listed in Table 7-5. Refer to Section 5B in the 6080A/82A Operator Manual for complete syntax descriptions of each command.

Table 7-5. Remote Programming Commands for Level Compensation Procedure

COMMANDS	DESCRIPTION
COMP_ATT	Initiates remote attenuator compensation procedure (Using measuring receiver).
COMP_ATTPMTR	Initiates remote attenuator compensation procedure (Using power meter).
COMP_OUT	Initiates remote output compensation procedure.
COMP_OUTDEF	Initiates remote output with default attenuator data
CC_RDPOWER	Accepts the measured power meter reading and updates its internal settings based on the reading.
CC_TARGET?	Retrieves the target RF level.
CC_FREQ?	Retrieves the current RF output frequency in Hz.
CC_SAVE	Calculates correction factors and save in compensation memory.
CC_EXIT	Exits compensation procedure immediately, discard measured data.
ERROR?	Retrieves earliest value from the error queue.
RFOUT	Enables/disables the Signal Generator RF output.

The attenuator compensation procedure using power meter is initiated with the command COMP_ATTPMTR. After initializing the power meter, the controller requests the Signal Generator's RF frequency with the command CC_FREQ? and waits for a response. When a response is received, it gets a power meter reading and sends it to the Signal Generator with the command CC_RDPOWER. It remains in the main loop until the Signal Generator returns the end code "9E+09, HZ" in response to the CC_FREQ? command. The main loop is then exited and the data is saved with the CC_SAVE command.

The controller queries the Signal Generator's RF frequency at each step to synchronize its actions with the Signal Generator and to determine when the procedure is complete. When the Signal Generator receives a reading, it updates its internal settings and does not respond to the next frequency query until it is ready for another reading. This forces the controller to wait for the Signal Generator's output to settle before it is allowed to take another reading.

When it receives two consecutive readings within 0.01 dB of the target level, it considers the displayed adjustment value correct and cycles to the next step.

The power meter must be zeroed before the first 24-dB attenuator is measured at each frequency. To do this, the controller must query the target level at each step and zero the power meter when it detects the transition from the 12-dB attenuator (target level -2 dBm) to the first of the five 24-dB attenuators (target level -14 dBm).

The controller program must ensure that each power meter reading is settled before sending it to the 6080A. In addition, the frequency dependent power meter calibration factor must be applied to every reading. The program listing in Appendix G uses a simple but effective method to obtain valid power meter readings.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

Proceed as follows to execute the Remote Attenuator Compensation Procedure Using Power Meter:

1. Press [SPCL] [0] [1], then program 1 MHz, +10.0 dBm, and [SPCL] [9] [2] [2].
2. Disable the Signal Generator's RF output and connect the the power sensor to the RF output.
3. Zero the power meter and select the power meter calibration factor. Enable the RF output.
4. Measure the RF level. If it is more than +10.0 dBm ±0.5 dB, the A8 Output PCA or A20 Attenuator/RPP Assembly is not operating correctly. Refer to Section 6 in this manual for troubleshooting and repair information.
5. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

6. Run the controller program

7. Zero the RF Level Closed-Case Calibration Factor to provide maximum adjustment range. This step may be performed at the beginning of the procedure between steps 5 and 6 if desired. However, doing so may introduce a fixed offset which must be compensated for at every measurement step. To zero the RF Level Calibration Factor:

   a. Enter SPCL 9 9 3

   b. Use the edit knob to adjust the calibration factor until it reads 0.00 dB.

   c. Press STO twice to store the new calibration factor.

8. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.

9. Remove the bottom instrument cover and the RF level adjustment access screw labeled A11R20 from the bottom module plate cover.

10. Program SPCL 0 1, 350 MHz and +9.0 dBm

11. Disable the RF output, zero the power meter, then enable the RF output. Select the power meter calibration factor.

12. Adjust RF level adjustment, R20 on the A11 Modulation Control PCA, for a reading of exactly +9 dBm on the power meter.

13. Replace the RF level adjustment access screw, and the instrument bottom cover.

SUB-SYNTHESIZER COMPENSATION PROCEDURES 7-16.

The Subsynthesizer Compensation Procedures generate the instrument-specific Subsynthesizer VCO compensation data. The procedures must be performed following any repair to the A3 Subsynthesizer VCO PCA that affects the software compensation data.

The procedure involves measuring the slope of the Subsynthesizer VCO tuning voltage at selected frequencies. The measurement is performed by adjusting the RF frequency until the voltage change measured with an external voltmeter matches the target voltage change. The slope can then be calculated from the known frequency adjustment and voltage change. The compensation DAC values are calculated from the measured slopes and stored in the compensation memory.

Front Panel Subsynthesizer Compensation Procedure 7-17.

REQUIREMENT:

- Number of Measurement Steps: 18
- Target Voltage Change: 0.100V

TEST EQUIPMENT:

- 4 ½-Digit Voltmeter (Fluke 8840A or equivalent DVM with a display offset mode).

REMARKS:

You initiate the front panel subsynthesizer compensation procedure by pressing the following key sequence: [SPCL] [9] [8] [4].

The target voltage difference of 0.100V is displayed in the MODULATION field. The RF frequency/ adjustment is displayed in the FREQUENCY field. The Subsynthesizer VCO identifier code A3 is displayed in the AMPLITUDE field and the COMP and VCO annunciators are lit to signify that the procedure is in progress.

When performing the procedure, connect the voltmeter to TP27 on the A4 Subsynthesizer PCA. Use the edit knob to adjust the RF frequency until the measured change in voltage at TP27 matches the target voltage change. The sequence is repeated for all 18 frequencies. This procedure typically takes 15 minutes to perform.

Table 7-6 summarizes the operation of the front panel keys used during the Front Panel Subsynthesizer Compensation Procedure. All other keys are ignored.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

PROCEDURE:

Proceed as follows to execute the Front Panel Subsynthesizer Compensation Procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position. Verify that the CAL and COMP annunciators on the front panel are flashing.

CAUTION

Do not turn the power off while the CAL|COMP switch is set on. The CAL|COMP switch protects the compensation memory from accidental damage.

2. Remove the instrument top cover.

3. Remove the plug button from the access hole labeled A4TP27 on the top side of the upper module plate. Connect the positive voltmeter probe to TP27 and the negative to ground.

Table 7-6. Front Panel Controls for Subsynthesizer Compensation Procedure

CONTROLS	FUNCTION AND DESCRIPTION
◁ ▷	BRIGHT DIGIT EDITING
KNOB	Turn edit knob to increment or decrement the frequency adjustment. Use left/right arrow keys to move the bright digit within the adjustment field.
ON/OFF	RF ON/OFF Toggles the RF output on/off.
STATUS	OVERRANGE/UNCAL or REJECTED ENTRY STATUS Normally displays the overrange/uncal status. Displays the rejected entry status code if there is a rejected entry.
RCL	APPLY ESTIMATED FREQUENCY ADJUSTMENT Programs a calculated frequency adjustment that will closely approximate the final adjustment for the current step.
STO	STORE MEASURED DATA Press key once, the prompt "Sto ?" is displayed. Press key again to store the data. "-- Sto --" is displayed for about 5 seconds until the store operation is complete. Attempts to store the data before all steps have been measured will be rejected with error code 92. Press any other key to cancel the store operation and resume the procedure.
	CAUTION **Do not turn the power off or change the CAL|COMP switchuntil the store operation is complete. Doing so coulddamage the contents of the compensation memory.**
CLR|LCL	ABORT THE PROCEDURE Press the key once, the prompt "Clr ?" is displayed. Press the key again to abort the procedure. "-- Clr --" is displayed to confirm the selection. All measured data is discarded and the previous instrument state is restored. Press any other key to resume the procedure.

4. Select the DC Volts mode of the Voltmeter with autoranging enabled.

5. Press SPCL 9 8 4 to initiate the Subsynthesizer compensation procedure. Verify that COMP and VCO annunciators are lit.

6. Zero the voltmeter display by enabling the offset mode.

7. Press RCL to program an estimated frequency adjustment.

8. Adjust the RF frequency using the edit knob until the voltmeter displays a 0.100 V offset.

9. Press STEP △ to go to the next step.

10. Repeat steps 6 through 9 until the last measurement step has been completed at 320 MHz.

11. Press the STO key twice to store the data.

NOTE

If the store operation is rejected (flashing "—Sto—"), press STATUS *to determine the cause of the rejected entry. Refer to the list of rejected entry error codes in Appendix C.*

12. Set the rear panel CAL|COMP switch to the 0 (off) position. Verify that the CAL and COMP annunciators on the front panel are not flashing.

13. Install the plug button for the TP27 access hole, and install the instrument top cover.

Remote Subsynthesizer Compensation Procedure 7-18.

The following paragraphs describe the remote Subsynthesizer Compensation Procedure. It describes the remote commands used in the procedure and the elements required to build a functioning controller program.

The basic structure of the Subsynthesizer Compensation Program is shown in Figure 7-4. A complete listing of a program that runs on a Fluke 1722A controller is in Appendix G.

```
initiate the Subsynthesizer Compensation Procedure with COMP_SUBSYN
initialize voltmeter

MAIN_LOOP:
    request the RF frequency with CC_FREQ?

    if( frequency = 9e9) goto DONE

    read voltmeter
    send reading to 6080A with CC_RDDVM
    goto MAIN_LOOP

DONE:
store new data in compensation memory with CC_SAVE
end
```

Figure 7-4. Basic Structure of Subsynthesizer Compensation Program

The procedure is initiated by the command COMP_SUBSYN. The controller requests the Signal Generator's RF frequency with the command CC_FREQ? and waits for a response. When a response is received, it obtains a voltmeter reading and sends it to the 6080A with the command CC_RDDVM. It remains in the main loop until the 6080A returns the end code "9E+09,HZ" in response to the CC_FREQ? command. The main loop is then exited and the data is saved with the CC_SAVE command.

Each time the 6080A receives a reading from the controller, it adjusts its internal settings and programs the new RF frequency. When it receives two consecutive readings within 0.001V of the target voltage change (0.100V) it considers the displayed adjustment value correct and cycles to the next step.

The controller program must ensure that each voltmeter reading is settled before sending it to the 6080A. The program listing in Appendix G uses a simple but effective method to obtain valid voltmeter readings.

NOTE

The rear panel CAL|COMP switch must be set to the 1 (on) position before initiating the compensation procedure.

The programming commands used in a remote Subsynthesizer Compensation Procedure are listed in Table 7-7. See the Operator Manual for complete syntax descriptions of each command.

Table 7-7. Remote Programming Commands for Subsynthesizer Compensation Procedure

COMMANDS	DESCRIPTION
COMP_SUBSYN	Initiates the remote subsynthesizer compensation procedure
CC_RDDVM	Sends the voltmeter reading to the 6080A
CC_FREQ?	Requests the current RF frequency
CC_TARGET?	Requests the target value
CC_SAVE	Saves the measured data
CC_EXIT	Aborts the compensation procedure immediately
ERROR?	Requests the rejected entry status

COARSE LOOP COMPENSATION PROCEDURES 7-19.

The coarse loop compensation procedures generate the instrument-specific compensation data for the A5 Coarse Loop VCO PCA. The procedures must be performed following a module replacement or repair that affects the coarse loop VCO compensation data.

The procedures can be initiated from the front panel or remotely through the IEEE-488 interface. Once initiated, they require no user interaction and need no external measurement equipment. Upon successful completion, the new data is automatically stored in the compensation memory on the A13 Controller PCA. The procedures can be performed in approximately 5 minutes.

The coarse frequency synthesis loop is programmable from 576 MHz to 960 MHz in 8-MHz steps. There is a unique steering DAC and compensation DAC value for each of the 49 steps. The coarse loop compensation procedure generates the steering DAC and compensation DAC values for the entire frequency range.

Front Panel Coarse Loop Compensation Procedure 7-20.

Refer to Table 7-8 for a description of front panel controls used in for coarse loop compensation procedures. You initiate the front panel coarse loop compensation procedure by pressing the following key sequence: SPCL 9 7 1.

Table 7-8. Front Panel Controls for Coarse Loop Compensation Procedure

CONTROLS	FUNCTION AND DESCRIPTION
CLR|LCL	Pause/Abort the procedure Press once; the procedure is paused and the prompt "Clr ?" is displayed. Press again to abort the procedure. "-- Clr --" is displayed to confirm the selection. All measured data is discarded, and the previous instrument state is restored. Press any other key to resume the procedure.

The COMP and VCO annunciators are lit and the coarse loop VCO PCA identifier A5 is displayed in the frequency field to signify that the coarse loop compensation procedure is in progress. Table 7-8. shows all of the active controls and describes their function while performing the procedure.

A 30-second countdown timer is displayed while the coarse loop VCO circuitry thermally stabilizes. This warmup delay is also inserted at the beginning of the second and third VCO bands.

Next, the initial coarse loop frequency of 576 MHz is programmed and is displayed. The software determines the optimal DAC values for the frequency using an iterative search algorithm. The process is repeated every 8 MHz until the entire frequency range has been measured. Upon completion, the message "— Sto —" is displayed and the measured data is loaded into the compensation memory.

If the correct DAC value for any step cannot be found, the procedure is exited immediately and the coarse loop frequency where the problem was encountered is flashed in the FREQUENCY display field.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure. Proceed as follows to execute the front panel coarse loop compensation procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.

CAUTION

Do not turn the power off or change the CAL|COMP switch until the store operation is complete. Doing so could damage the contents of the compensation memory.

2. Enter SPCL 9 7 1 to initiate the procedure.

3. Wait for the procedure to complete.

4. Set the rear panel CAL|COMP switch to the 0 (off) position.

Remote Coarse Loop Compensation Procedure 7-21.

The remote coarse loop compensation procedure is identical to the front panel procedure with the exception that it is initiated by the remote command COMP_COARSE rather than by special function.

The program listing in Figure G-7 in Appendix G illustrates how to initiate the procedure and how to use the *OPC? command to make the controller wait until the procedure is complete.

If the correct DAC value for any step cannot be found, the procedure is exited immediately and the coarse loop frequency where the problem was encountered is flashed in the FREQUENCY display field. The error code and frequency can also be interrogated through the remote interface at a later time with the command CC_ERRFREQ?. The error frequency information is retained until the instrument is powered down.

The commands used in the remote coarse loop compensation procedure are listed in Table 7-9. See Section 5B in the Operator Manual for complete syntax descriptions of each command.

Table 7-9. Remote Programming Commands for Coarse Loop Compensation Procedure

COMMANDS	FUNCTION AND DESCRIPTION
COMP_COARSE	Initiates the remote coarse loop compensation procedure.
CC_EXIT	Exits the compensation procedure immediately.
CC_ERRFREQ?	Reports the most recent coarse loop or sum loop compensation procedure error code and the frequency where the error occurred.
ERROR?	Requests the rejected entry status.

SUM LOOP COMPENSATION PROCEDURES 7-22.

The sum loop compensation procedures generate the instrument-specific compensation data for the A9 Sum Loop VCO PCA. The procedures must be performed following a module replacement or repair that affects the sum loop VCO compensation data.

The procedures can be initiated from the front panel or remotely through the IEEE-488 interface Once initiated, they require no user interaction and need no external measurement equipment. Upon successful completion, the new data is automatically stored in the compensation memory on the A13 Controller PCA. The procedures can be performed in approximately 5 minutes.

The sum loop frequency range is from 480 MHz to 1056 MHz. There is a unique steering DAC and compensation DAC value every 1 MHz. The sum loop compensation procedure generates the steering DAC and compensation DAC values for the entire frequency range.

Front Panel Sum Loop Compensation Procedure 7-23.

You initiate the front panel sum loop compensation procedure by pressing the following key sequence: SPCL 9 7 2.

The COMP and VCO annunciators are lit and the sum loop VCO PCA identifier A9 is displayed in the amplitude field to signify that the Sum Loop Compensation Procedure is in progress. Table 7-10 shows all of the active controls and describes their function while performing the procedure.

Table 7-10. Front Panel Controls for Sum Loop Compensation Procedure

CONTROLS	FUNCTION AND DESCRIPTION
CLR|LCL	Pause/Abort the procedure Press once; the procedure is paused and the prompt "Clr ?" is displayed. Press again to abort the procedure. "-- Clr --" is displayed to confirm the selection. All measured data is discarded, and the previous instrument state is restored. Press any other key to resume the procedure.

A 30 second countdown timer is displayed while the sum loop VCO circuitry thermally stabilizes. This warmup delay is also inserted at the beginning of the other three VCO bands.

Next, the initial sum loop frequency of 480 MHz is programmed and is displayed. The software determines the optimal DAC values for the frequency using an iterative search algorithm. The process is repeated every 5 MHz until the entire frequency range has been measured. Upon completion, the measured DAC values are interpolated to 1 MHz steps, the message "— Sto —" is displayed and the measured data is loaded into the compensation memory.

If the correct DAC value for any step cannot be found, the procedure is exited immediately and the sum loop frequency where the problem was encountered is flashed in the FREQUENCY display field.

The Signal Generator must be operated at room temperature for at least one hour with the module plate covers in place before performing this compensation procedure.

Proceed as follows to execute the front panel sum loop compensation procedure:

1. Set the rear panel CAL|COMP switch to the 1 (on) position.

CAUTION

Do not turn the power off or change the CAL|COMP switch until the store operation is complete. Doing so could damage the contents of the compensation memory.

2. Enter SPCL 9 7 2 to initiate the procedure.
3. Wait for the procedure to complete.
4. Set the rear panel CAL|COMP switch to the 0 (off) position.

Remote Sum Loop Compensation Procedure 7-24.

The Remote Sum Loop Compensation Procedure is identical to the front panel procedure except that it is initiated by the remote command COMP_SUM rather than by special function. A program listing in Appendix G illustrates how to initiate the procedure and how to use the *OPC? command to make the controller wait until the procedure is complete.

If the correct DAC value for any step cannot be found, the procedure is exited immediately and the sum loop frequency where the problem was encountered is flashed in the FREQUENCY display field. The error code and frequency can also be interrogated through the remote interface at a later time with the command CC_ERRFREQ?. The error frequency information is retained until the instrument is powered down.

The commands used in the remote sum loop compensation procedure are listed in Table 7-11. Refer to Section 5B in the 6080A/82A Operator Manual for complete syntax descriptions of each command.

Table 7-11. Remote Programming Commands for Sum Loop Compensation Procedure

COMMANDS	FUNCTION AND DESCRIPTION
COMP_SUM	Initiates the remote sum loop compensation procedure.
CC_EXIT	Exits the compensation procedure immediately.
CC_ERRFREQ?	Reports the most recent sum loop or coarse loop compensation procedure error code and the frequency where the error occurred.
ERROR?	Requests the rejected entry status.

Section 8
List of Replaceable Parts

TABLE OF CONTENTS

ASSEMBLY NAME	DRAWING NO.	TABLE NO.	PAGE NO.	FIGURE NO.	PAGE NO.
6080A Final Assembly	6080A T&B	8-1	8-6	8-1	8-9
A1 Display PCA	6082A-7650	8-2	8-21	8-2	8-22
A2 Coarse Loop PCA	6082A-7660	8-3	8-23	8-3	8-27
A3 Subsynthesizer VCO PCA	6082A-7661	8-4	8-28	8-4	8-29
A4 Subsynthesizer PCA	6082A-7662	8-5	8-30	8-5	8-33
A5 Coarse Loop VCO PCA	6082A-7663	8-6	8-34	8-6	8-35
A6 Mod Oscillator PCA	6082A-7667	8-7	8-36	8-7	8-37
A8 Output PCA	6082A-7640	8-8	8-38	8-8	8-42
A9 Sum Loop VCO PCA	6082A-7641	8-9	8-43	8-9	8-44
A10 Premodulator PCA	6082A-7646	8-10	8-45	8-10	8-48
A11 Modulation Control PCA	6082A-7648	8-11	8-49	8-11	8-52
A12 Sum Loop PCA	6082A-7642	8-12	8-53	8-12	8-56
A13 Controller PCA	6082A-7643	8-13	8-57	8-13	8-59
A14 FM PCA	6082A-7645	8-14	8-60	8-14	8-64
A15 Power Supply PCA	6082A-7670	8-15	8-65	8-15	8-67
A16 IEEE-488 Connector PCA	6082A-7671	8-16	8-67	8-16	8-67
A19 Switch PCA	6080A-7651	8-17	8-68	8-17	8-68
A20 Attenuator/RPP Assembly	6080A-7636	8-18	8-69	8-18	8-69
A7 Relay Driver PCA	6082A-7632	8-19	8-70	8-19	8-71
A21 Attenuator PCA	6080A-4036	8-20	8-72	8-20	8-73
A22 Delay Line Assembly	6080A-7666	8-21	8-74	8-21	8-75

INTRODUCTION 8-1.

Section 8 contains an illustrated list of replaceable parts for the 6080A Synthesized RF Signal Generator. Parts are listed by assembly, alphabetized by reference designator. Each assembly is accompained by an illustration showing the location of each part and its reference designator. The parts lists include the following information:

- Reference Designator
- An indication if the part is subject to damage by static discharge
- Description of each part
- Fluke Stock Number
- Federal Supply Code for Manufacturers (a code-to-name list provided at the end of this section)
- Manufacturer's part number or generic type
- Total Quantity of components per assembly
- Any special notes (i.e., factory-selected part)

CAUTION

Parts with an asterisk (*) in the "S" column are subject to damage by static discharge.

HOW TO OBTAIN PARTS 8-2.

Electrical components may be ordered directly from the manufacturer by using the manufacturer's part number, or from John Fluke Mfg. Co. (or its authorized representative) by using the Fluke stock number. A list of federal supply codes is provided at the end of this section.

To ensure prompt and efficient handling of your order, include the following information.

- Fluke stock number (six-digit part number)
- Description
- Reference designator (e.g., R112)
- Quantity
- Part Number and revision level of the pca containing the part

Price information of parts is available from the John Fluke Mfg. Co., Inc. or its representative.

MANUAL STATUS INFORMATION 8-3.

The first table in this section defines the assembly revision levels that are documented in this manual. Revision levels are printed on the component side of each pca.

SERVICE CENTERS 8-4.

A list of Fluke/Philips technical service centers is provided at the end of this section.

Manual Status Information

REF OR OPTION NO.	ASSEMBLY NAME	FLUKE PART NO.	X = The PCA revision levels documented in this manual.																										
			–	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
A1	Display PCA	882068		X																									
A2	Coarse Loop PCA	882071			X																								
A3	Subsynthesizer VCO PCA	882076		X																									
A4	Subsynthesizer PCA	882084		X																									
A5	Coarse Loop VCO PCA	882089		X																									
A6	Mod Oscillator PCA	882097		X																									
A8	Output PCA	882035				X																							
A9	Sum Loop VCO PCA	882035			X																								
A10	Premodulator PCA	882055		X																									
A11	Modulation Control PCA	882063	X																										
A12	Sum Loop PCA	882043			X																								
A13	Controller PCA	882048		X																									
A14	FM PCA	882050			X																								
A15	Power Supply PCA	882100		X																									
A16	IEEE-488 Connector PCA	868872	X																										
A19	Switch PCA	860858	X																										
A20A7	Relay Driver PCA	882022		X																									
A20A21	Attenuator PCA	860812	X																										
A25, A26	Delay Line PCAs	860887	X																										

Table 8-1. 6080A Final Assembly
(See Figure 8-1.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
		A00					
A 1	*	DISPLAY PCA	882068	89536	882068	1	
A 2	*	COARSE LOOP PCA	882071	89536	882071	1	
A 3	*	SUBSYNTHESIZER VCO PCA	882076	89536	882076	1	
A 4	*	SUBSYNTHESIZER PCA	882084	89536	882084	1	
A 5		COARSE LOOP VCO PCA	882089	89536	882089	1	
A 6	*	MOD OSCILLATOR PCA	882097	89536	882097	1	
A 8	*	OUTPUT PCA	882030	89536	882030	1	
A 9		SUM LOOP VCO PCA	882035	89536	882035	1	
A 10	*	PREMODULATOR PCA	882055	89536	882055	1	
A 11	*	MODULATION CONTROL PCA	882063	89536	882063	1	
A 12	*	SUM LOOP PCA	882043	89536	882043	1	
A 13	*	CONTROLLER PCA	882048	89536	882048	1	
A 14	*	FM PCA	882050	89536	882050	1	
A 15	*	POWER SUPPLY PCA	882100	89536	882100	1	
A 16	*	IEEE-488 CONNECTOR PCA	868872	89536	868872	1	
A 19	*	SWITCH PCA	860858	89536	860858	1	
A 20	*	ATTENUATOR/RPP ASSEMBLY	860812	89536	860812	1	
A 22	*	DELAY LINE ASSEMBLY	860887	89536	860887	1	
MP 1		CORD,LINE,5-15/IEC,3-18AWG,SVT	284174	70903	17239	1	
TM 1		6080A SERVICE MANUAL	868914	89536	868914	1	
TM 2		6080A/6082A OPERATORS MANUAL	861034	89536	861034	1	
TM 3		6080A/6082A PROGRAMMING GUIDE	882147	89536	882147	1	
TM 4		6080A/6082A OPERATOR REFERENCE GUIDE	882154	89536	882154	1	
		A40					
C 1, 2		CAP,CER,1000PF,+-5%,50V,C0G	528539	04222	SR215A102JAT	2	
H 1, 6, 7,		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		81	
H 9- 12, 16-			772236				
H 20, 25,101-			772236				
H 104,201-204,			772236				
H 206-216,301-			772236				
H 310,401,402,			772236				
H 501-514,601-			772236				
H 611			772236				
H 901-930,937-0		SCREW,PH,P,MAG,SS,LOCK,6-32,1.00	861755	COMMERCIAL		38	
H 944			861755				
H 933-936		WASHER,SPRING,STL,.138,.281,.020	571968	COMMERCIAL		4	
MP 1		BARRIER, OUTPUT BOARD, PLATED	868930	89536	868930	1	
MP 3		OUTPUT AMP COVER, PLATED	860952	89536	860952	1	
MP 4		SUM LOOP LID, PLATED	860957	89536	860957	1	
MP 5- 21		AIDE,PCB PULL	541730	89536	541730	17	
MP 23, 24		CLAMP,CABLE,SELF-ADHES,1.00X.88X.055	513606	06915	CFCC-8	2	
MP 53- 55		CABLE ACCESSORY,CLAMP,ADHESIVE,NYLON	838300.881904	06915	MWSSEB-1-01A	3	
MP 100	*	OUTPUT MODULE, FILTER ASSY	881904	89536	881904	1	
MP 101		GASKET,SHIELDING,MONEL MESH,CIRCULAR	720664	53217	20-11101	23	
MP 102		GASKET,SHIELDING,CONDUCTIVE SILICONE	867309	18565	19-09-B363-1350	1	
MP 103		GROUND STRIP,BECU,SPRING FINGERS	811661	34641	97-520-08	8	
MP 104		GROUND STRIP,BECU,SPRING FINGER	756445	34641	97-500-08	7	
W 32, 35		CABLE ASSY,10-CKT RIBBON JUMPER	860747	89536	860747	2	
W 33		CABLE ASSY,OUTPUT-MOD CONTROL	860739	89536	860739	1	
W 34		CABLE ASSY. PREMOD-MOD CTRL	860754	89536	860754	1	
		A50					
H 1, 41, 42		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		3	
H 2- 36		SCREW,TH,P,STL,LOCK,4-40,.187	854658	COMMERCIAL		35	
H 37- 40		SCREW,CAP,SCKT,SS,8-32,.375	295105	COMMERCIAL		4	
J 1		ADAPTER,COAX,SMA(M),N(M)	516963	21845	SF1132-6002	1	
L 1		CORE,TOROID,FERRITE,20X14.5X7.5MM	493551	54583	H5C2-T20-7.5-14.5	1	
MP 1, 2		CORNER HANDLE, FRONT 5.25 IN, GREY	861161	89536	861161	2	
MP 3		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
MP 5		LENS DISPLAY	657718	89536	657718	1	
MP 6		ENCODER WHEEL	764548	0A5E9	764548	1	
MP 7		SHIELD, DISPLAY	812818	89536	812818	1	
MP 8		BUSHING INSULATION R.F. OUTPUT	861174	89536	861174	1	
MP 9		KNOB, ENCODER, GREY	868794	89536	868794	1	
MP 10		ENCODER, MOLDED	861026	89536	861026	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-1. 6080A Final Assembly (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
MP 13		POWER BUTTON, ON/OFF	775338	89536	775338	1	
MP 15		FRONT PANEL	842849	89536	842849	1	
MP 16	*	SWITCH SHIELD	860643	89536	860643	1	
MP 18		RF OUTPUT BRACKET, PLATED	860960	89536	860960	1	
MP 19, 20		CORNER BRACKET	657601	89536	657601	2	
MP 43- 53		WASHER,FLAT,SS,.105,.255,.016	147645	COMMERCIAL		11	
S 1		SWITCH, ELASTOMERIC, LEFT	812743	89536	812743	1	
S 2		SWITCH,ELASTOMERIC,CENTER	812750	89536	812750	1	
S 3		SWITCH,ELASTOMERIC,RIGHT	812768	89536	812768	1	
		A60					
C 1		CAP,CER,1000PF,+-5%,50V,C0G	528539	04222	SR215A102JAT	1	
H 1- 41,101,		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		77	
H 102,201-221,			772236				
H 301-303,501-			772236				
H 503,701-707			772236				
H 42, 43		SCREW,PH,P,SS,LOCK,6-32,.750	376822	COMMERCIAL		2	
H 903-905		WASHER,SPRING,STL,.138,.281,.020	571968	COMMERCIAL		3	
MP 1- 13		AIDE,PCB PULL	541730	89536	541730	13	
MP 19, 20		HEAT SINK, DIVIDER	861047	89536	861047	2	
MP 57, 58		CABLE TIE ANCHOR,ADHSV,.160TIE	407908	06383	ABMM-A-C	2	
MP 62		DECAL, MODULE WARNING	868799	22670	868799	1	
MP 63, 64		INSUL PART,TO-220,SILICONE,ADHESIVE	867804	18565	60-12-D391-1674	2	
MP 65	*	FILTER SUBASSY, SYNTH MODULE	861109	89536	861109	1	1
R 1		RES,CF,0.51,+-5%,0.25W	381954	59124	CF1-4 0R51 J B	1	
		A70					
B 1		FAN ASSEMBLY	864967	89536	864967	1	
F 1		FUSE,.25X1.25,2A,250V,FAST	109173	71400	AGC-2	1	
H 1- 8		SCREW,PH,P,STL,LOCK,6-32,.250	152140	COMMERCIAL		8	
H 14, 15		SCREW,TH,P,STL,LOCK,4-40,.187	854658	COMMERCIAL		2	
H 16- 19		WASHER,FLAT,FIBER,.196,.500,.031	333989	86928	5600-8-32	4	
H 20- 23		NUT,HEX,ELASTIC STOP,STL,8-32,.172	306308	10059	22NTM-82	4	
H 24- 27		SCREW,CAP,BH,SCKT,STL,6-32,.500	542761	COMMERCIAL		4	
H 28- 31		SCREW,PH,P,SS,8-32,2.750	800441	COMMERCIAL		4	
H 36- 39		SCREW,CAP,SCKT,SS,8-32,.375	295105	COMMERCIAL		4	
H 40- 47		WASHER,FLAT,SS,.174,.375,,.032	176743	COMMERCIAL		8	
H 48- 50		NUT,HEX,ELAST STOP,STL,6-32,.125	110841	72962	22NTM-62	3	
H 51, 52		CONN ACC,D-SUB,FEMALE SCREWLOCK,.250	854810	55566	854810	2	
H 53, 54		CONN ACC,MICRO-RIBBON,SCREW LOCK	854737	05791	LT43026	2	
H 55, 56		WASHER,FLAT,SS,.119,.187,.010	853296	COMMERCIAL		2	
H 57, 58		WASHER,FLAT,MYLAR,.205,.309,.007	240820	86928	5622-25-7	2	
H 59- 63		SCREW,PH,P,MAG,SS,LOCK,6-32,.500	853986	COMMERCIAL		5	
MP 2		BUSHING,COVER,R.F. OUTPUT	868781	89536	868781	1	
MP 6		REAR PANEL	860598	89536	860598	1	
MP 7		FAN COVER	860601	89536	860601	1	
MP 8		TRANSFORMER COVER, PAINTED	860606	89536	860606	1	
MP 9		AIR FILTER	861005	50472	861005	1	
MP 10, 11		CABLE ACC,CLAMP,.500 ID,SCREW MOUNT	100974	06915	N8B	2	
MP 12, 13		CORNER BRACKET	657601	89536	657601	2	
MP 14, 15		CORNER HANDLE, FRONT 5.25 IN, GREY	861161	89536	861161	2	
MP 16, 17		POWER SUPPLY BRACKET	860593	89536	860593	2	
MP 18- 21		MOUNT,VIBRATION ISOLATOR,NEOPRENE	854083	1L965	J17736-21	4	
MP 22- 25		PLUG, BUTTON	861166	89536	861166	4	
MP 26- 29		MOUNT ACC,FERRULE,6-32,.365,.175	855036	1L965	Y-31124-4-1	4	
MP 34		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
MP 35		TRANSF PART,COVER,EI150,3 SLOTS	854773	91247	DO-9510/3 ZINC CHROMATE	1	
T 1		POWER TRANSFORMER, 120/240V, 50-60HZ	861141	89536	861141	1	
W 6		CABLE ASSY, RF, W6	861067	89536	861067	1	
W 7		CABLE ASSY, RF, W7	861070	89536	861070	1	
W 11		CABLE ASSY,LINE FILTER	860788	89536	860788	1	
		A80					
H 1		SCREW,TH,P,SS,6-32,.312	335174	COMMERCIAL		1	
H 2- 21		SCREW,FH,P,STL,LOCK,8-32,.375	114116	COMMERCIAL		20	
H 22- 41		SCREW,FHU,P,SS,LOCK,6-32,.250	320093	COMMERCIAL		20	
H 42- 57		SCREW,PH,P,STL,LOCK,4-40,.187	820779	COMMERCIAL		16	
H 58, 59		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		2	

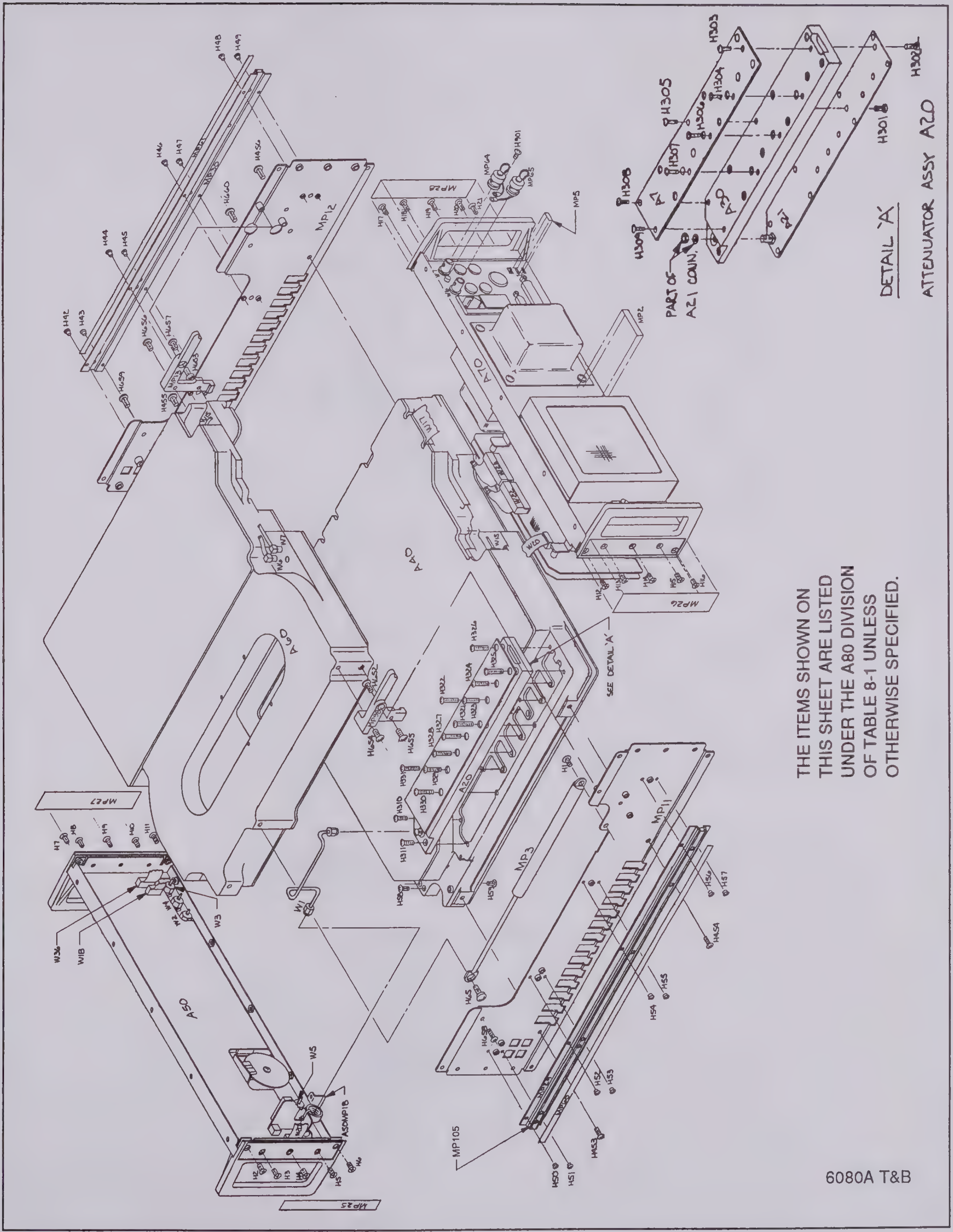
An * in 'S' column indicates a static-sensitive part.

Table 8-1. 6080A Final Assembly (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
H 65		SCREW,SHLDR,TH,SL,STL,8-32,.437	855218	COMMERCIAL		1	
H 310,311,401-		SCREW,PH,P,MAG,SS,LOCK,6-32,.375	783225	COMMERCIAL		116	
H 431,460-491,			783225				
H 601-629,671-			783225				
H 689,901-903			783225				
H 321-331		SCREW,PH,P,SS,LOCK,6-32,.750	376822	COMMERCIAL		11	
H 437-441,448,		SCREW,PH,P,STL,LOCK,10-32,.250	218941	COMMERCIAL		7	
H 449			218941				
H 453-456,652-		SCREW,PH,P,SS,LOCK,8-32,.375	559054	COMMERCIAL		21	
H 660,904-911			559054				
MP 2, 97		LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	22670	844712	2	
MP 3		SPRING,DAMPER,12.50 IN	852160	55787	852160	1	
MP 5		DECAL, CAL	861158	22670	861158	1	
MP 9		COVER, GRAY #3 TOP	881966	89536	881966	1	
MP 10		COVER, GRAY #3 BOTTOM	881917	89536	881917	1	
MP 11		CHASSIS SIDE, RIGHT	842799	89536	842799	1	
MP 12		CHASSIS SIDE, LEFT	842802	89536	842802	1	
MP 13		HINGE, LEFT	860580	89536	860580	1	
MP 14		DECAL, FRONT PANEL	812826	22670	812826	1	
MP 16, 21, 22,		METAL PART,STAMPED,HOLE PLUG,.500	101774	18310	790-3008	11	
MP 35- 41, 68			101774				
MP 17		OUTPUT COVER, PLATED	882659	89536	882659	1	
MP 18		CONTROLLER COVER, PLATED	860940	89536	860940	1	
MP 19		COARSE LOOP COVER, PLATED	860973	89536	860973	1	
MP 20		SUBSYNTH COVER, PLATED	860978	89536	860978	1	
MP 25- 28		DECAL, CORNER HANDLE	861146	22670	861146	4	
MP 29, 30		SIDE TRIM	861042	89536	861042	2	
MP 31- 34		BOTTOM FOOT, MOLDED	868786	89536	868786	4	
MP 46- 50		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	5	
MP 60, 61		DECAL, SIDE TRIM	861153	22670	861153	2	
MP 63		DECAL, MODULE WARNING	868799	22670	868799	1	
MP 64, 65		CONN ACC,COAX,BNC,CAP	478982	00779	1-330022-2	2	
MP 66, 67		CABLE TIE,CLAMP,8"L,1.75 DIA,#10SCREW	104638	06383	SSC2S-S10	2	
MP 69- 79		METAL PART,STAMPED,HOLE PLUG,.250	101766	18310	790.3002	11	
MP 96		OPERATION DECAL	860911	89536	860911	1	
MP 98		HINGE, RIGHT	860585	89536	860585	1	
MP 99		LENS DECAL	882592	89536	882592	1	
MP 105		GASKET,SHIELDING,MONEL MESH	520320	53217	20-90190	6	
W 1		CABLE ASSY, SR, RF OUTPUT	860924	00779	860924	1	
W 14		CABLE ASSY,RF,SEMI-SEMIRIGID	860721	89536	860721	1	
W 16		CABLE ASSY, SYNTHESIZER-CTRLR	860770	89536	860770	1	
W 17		CABLE ASSEMBLY, CONTROLLER-IEEE	860791	89536	860791	1	
W 18		CABLE ASSY,DISPLAY-CTRLR #1	860759	89536	860759	1	
W 19		CABLE ASSY,RELAY DRIVER	860734	89536	860734	1	
W 20		CABLE ASSY.FRONT PANEL POWER	860762	89536	860762	1	
W 22		CABLE ASSY,CTRLR POWER	860742	89536	860742	1	
W 23		CABLE ASSY, SYNTHESIZER POWER	860775	89536	860775	1	
W 36		CABLE ASSY,DISPLAY-CTRLR #2	860767	89536	860767	1	
W 37		RF INTERCONNECT HARNESS	860726	89536	860726	1	

An * in 'S' column indicates a static-sensitive part.

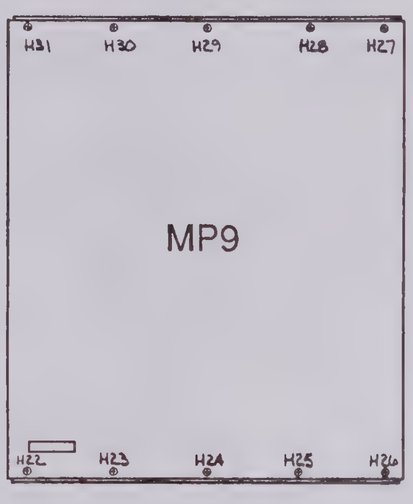
NOTE 1 = Module includes A22 (Delay Line Assembly), filters, and hardware.


DETAIL 'A'
ATTENUATOR ASSY A20
H301
H302
H303
H304
H305
H306
H307
H308
H309
PART OF A21 COUN.
A20
A21
MP5
MP2
A70
MP14
MP15
H901
MP28
MP26
MP12
A60
A40
A20
A50
MP11
MP3
MP27
MP25
MP105
W1
W3
W5
W36
W18
SEE DETAIL 'A'
H42
H43
H44
H45
H46
H47
H48
H49
H50
H51
H52
H53
H54
H55
H56
H57
H452
H453
H454
H455
H456
H457
H459
H460
H463
H652
H654
H655
H310
H311
H322
H324
H325
H326
H327
H328
H330
H331
H2
H3
H5
H6
H7
H8
H9
H10
H11
H12
H13
H14
H15
H16
H17
H18
H19
H20
H21
ASSY MP18

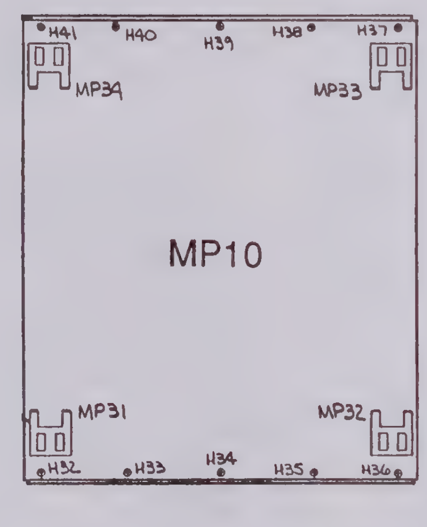
THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A80 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly


H31
H30
H29
H28
H27
MP9
H22
H23
H24
H25
H26

TOP COVER

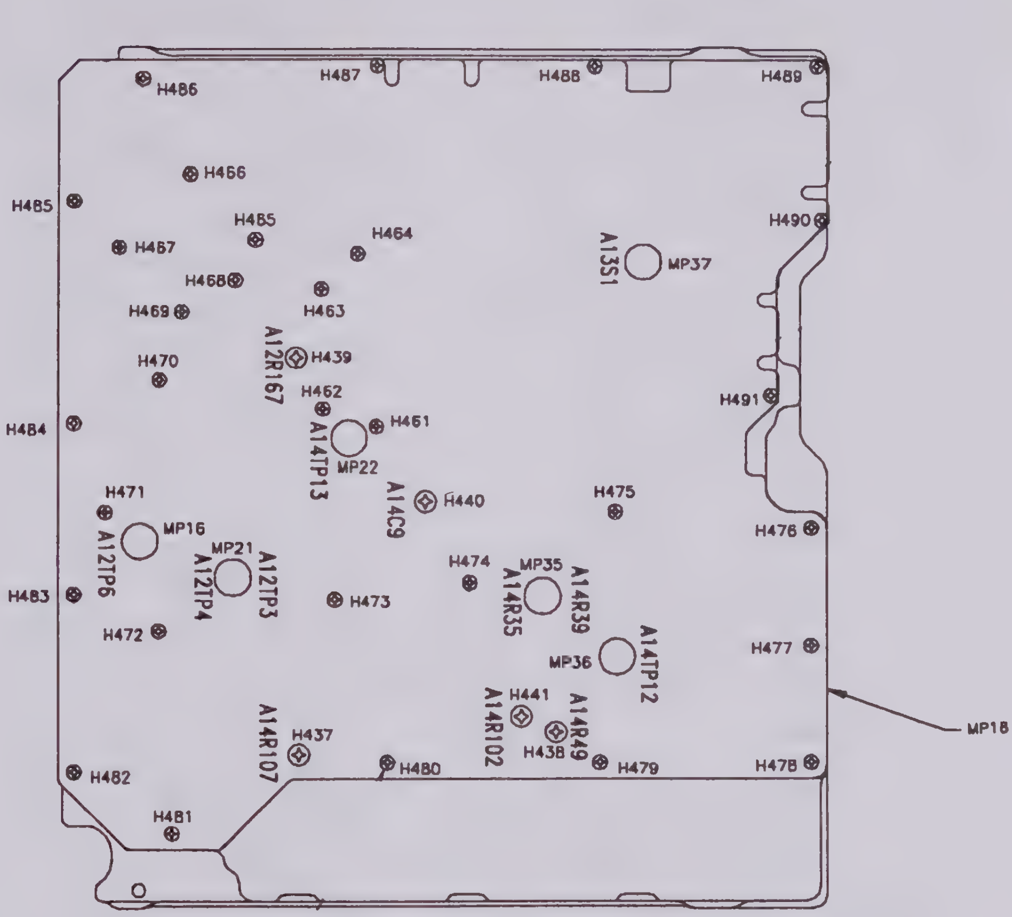

H41
H40
H39
H38
H37
MP34
MP33
MP10
MP31
MP32
H32
H33
H34
H35
H36

BOTTOM COVER

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A80 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

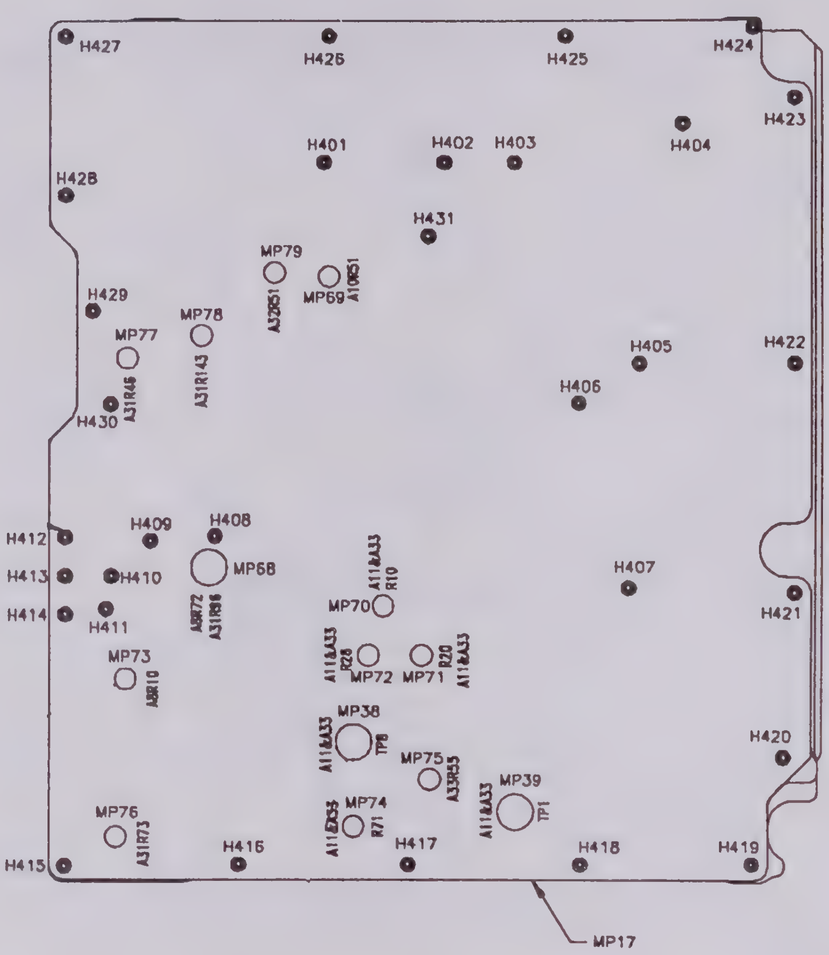

H486
H487
H488
H489
H466
H485
H465
H464
H490
A13S1
MP37
H467
H468
H463
H469
A12R167
H439
H470
H462
H491
H484
H461
A14TP13
MP22
H471
A14C9
H440
H475
MP16
H476
A12TP6
MP21
A12TP4
A12TP3
H474
MP35
A14R35
A14R39
H483
H473
H472
A14TP12
MP36
H477
H441
A14R102
A14R49
MP18
A14R107
H437
H438
H480
H479
H478
H482
H481

CONTROLLER SIDE OF OUTPUT MODULE

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A80 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

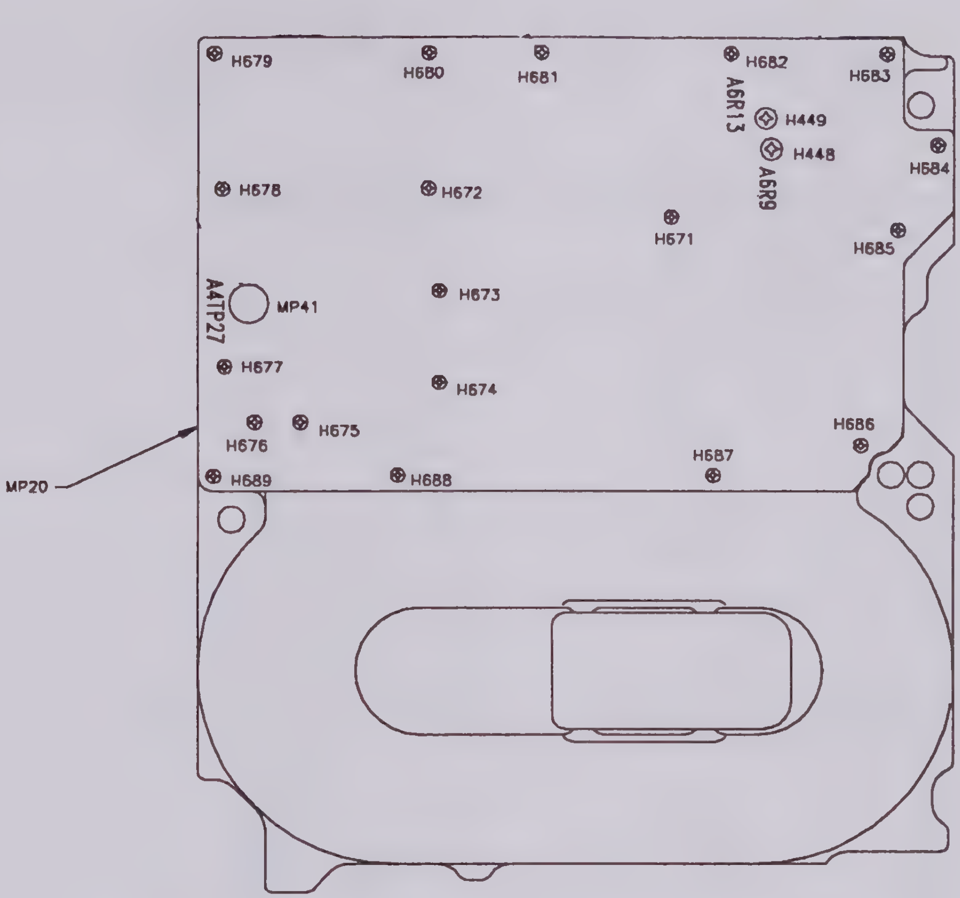

H427
H426
H425
H424
H423
H401
H402
H403
H404
H428
H431
MP79
MP69
A10R51
A32R51
H429
MP78
MP77
H405
H422
H406
A31R46
A31R143
H430
H412
H409
H408
H413
H410
MP68
A11&A33
R10
H407
H414
H411
A8R72
A31R86
MP70
H421
MP73
A8R10
A11&A33
R28
MP72
MP71
R20
A11&A33
MP38
A11&A33
TP8
H420
MP75
A33R55
MP39
A11&A33
TP1
MP76
A31R73
MP74
A11&A35
R71
H415
H416
H417
H418
H419
MP17

OUTPUT SIDE OF OUTPUT MODULE

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A80 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

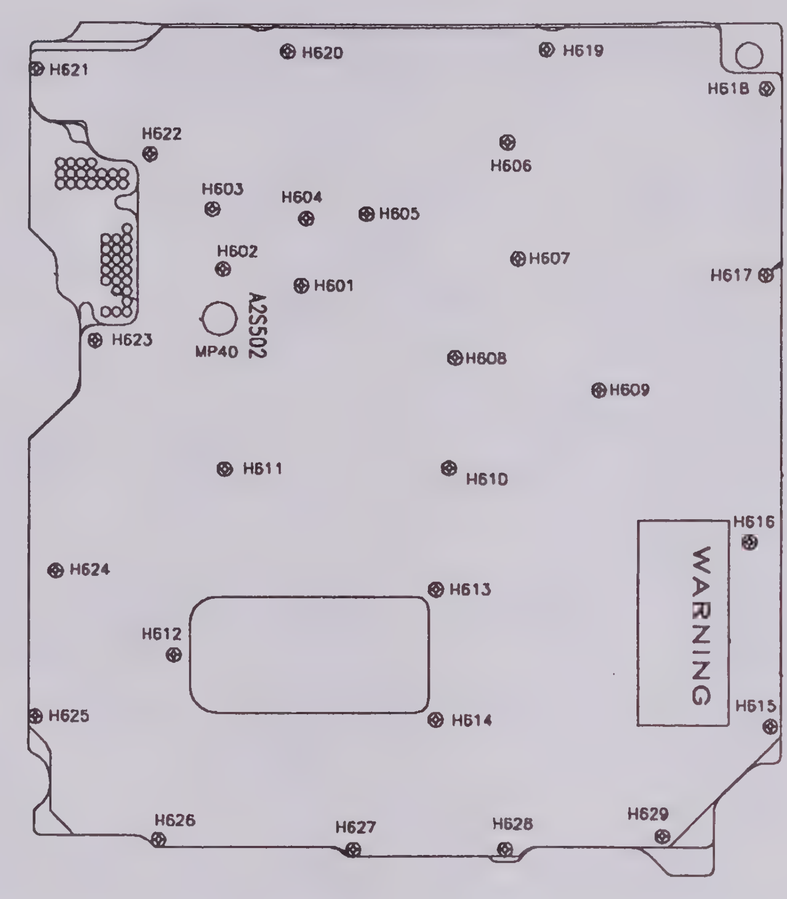

H679
H680
H681
H682
H683
A6R13
H449
H448
A6R9
H684
H678
H672
H671
H685
A4TP27
MP41
H673
H677
H674
H676
H675
H686
H687
MP20
H689
H688

SUBSYNTHESIZER SIDE OF SYNTHESIZER MODULE

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A80 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

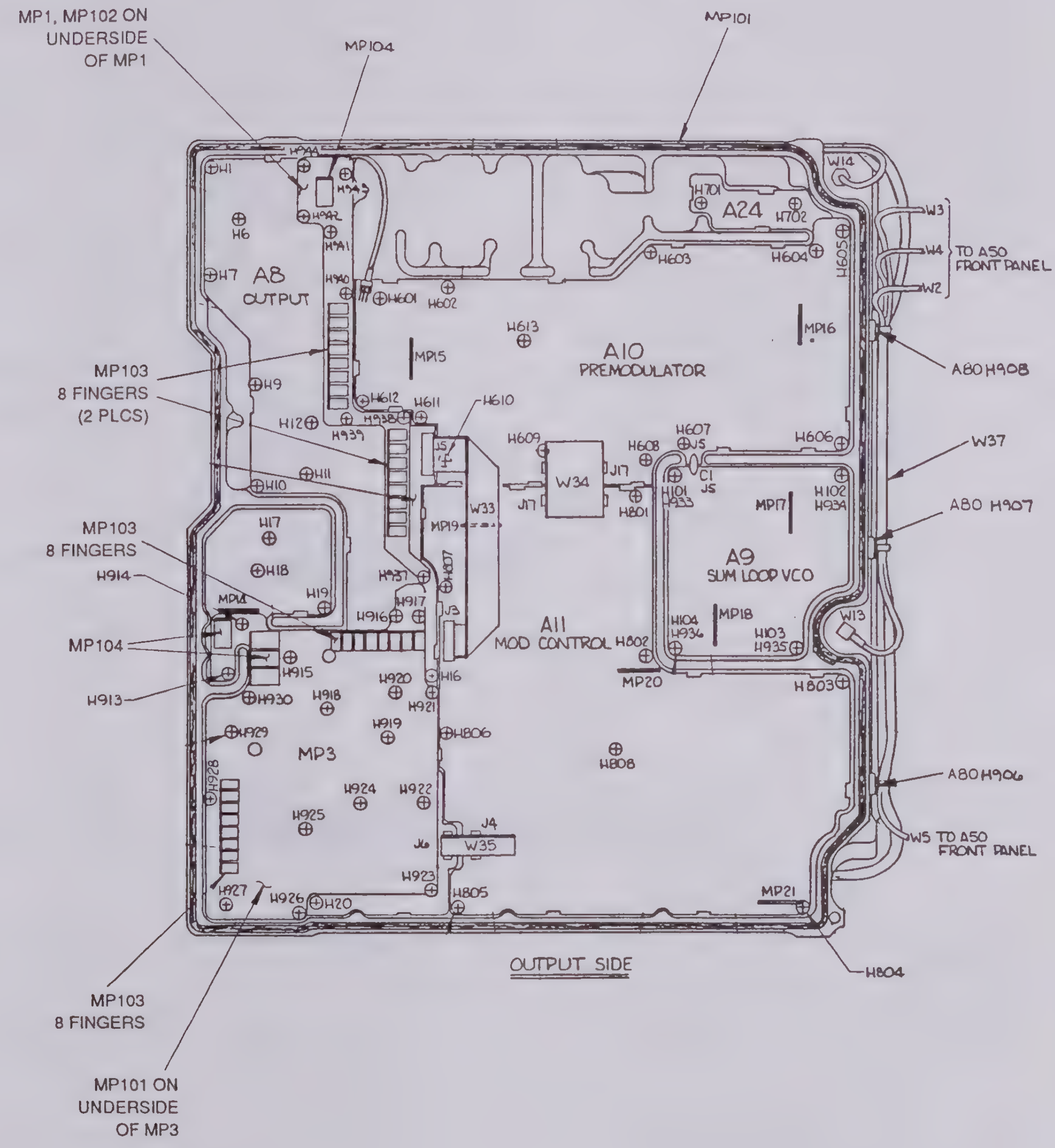

H621
H620
H619
H618
H622
H606
H603
H604
H605
H602
H607
H601
H617
A2S502
H623
MP40
H608
H609
H611
H610
H616
WARNING
H624
H613
H612
H625
H614
H615
H626
H627
H628
H629

COARSE LOOP SIDE OF SYNTHESIZER MODULE

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A80 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

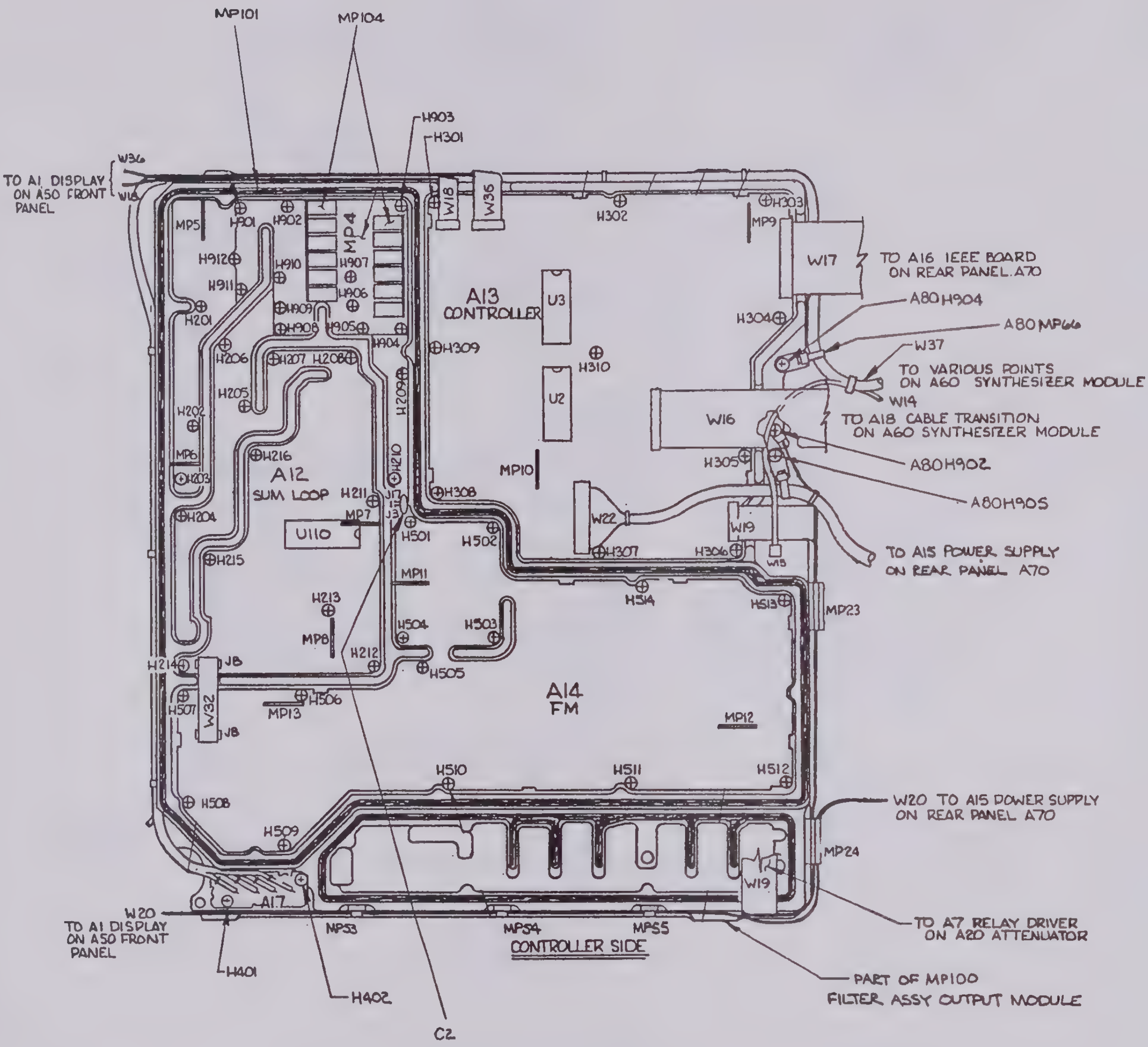

MP1, MP102 ON UNDERSIDE OF MP1
MP104
MP101
H944
H1
H943
H942
H941
H6
H7
A8
OUTPUT
H940
H601
H602
W14
H701
A24
H702
H603
H604
H605
W3
W4
TO A50 FRONT PANEL
W2
H613
MP15
A10
PREMODULATOR
MP16
A80 H908
MP103
8 FINGERS
(2 PLCS)
H9
H612
H611
H610
H12
H938
H939
H609
H607
J5
H608
H606
W37
H11
H10
W34
J17
C1
J5
H101
H933
H801
H102
H934
W33
J17
MP17
A80 H907
MP103
8 FINGERS
H17
MP19
H807
A9
SUM LOOP VCO
H914
H18
H937
H19
H917
MP18
MP14
H916
J3
A11
MOD CONTROL
H802
H104
H936
H103
H935
W13
MP104
H915
H16
MP20
H803
H913
H930
H918
H920
H921
H929
H919
H806
MP3
H808
H928
A80 H906
H924
H922
H925
J4
J6
W35
W5 TO A50 FRONT PANEL
H923
H927
H926
H20
H805
MP21
OUTPUT SIDE
H804
MP103
8 FINGERS
MP101 ON UNDERSIDE OF MP3

A40 OUTPUT MODULE

THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A40 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

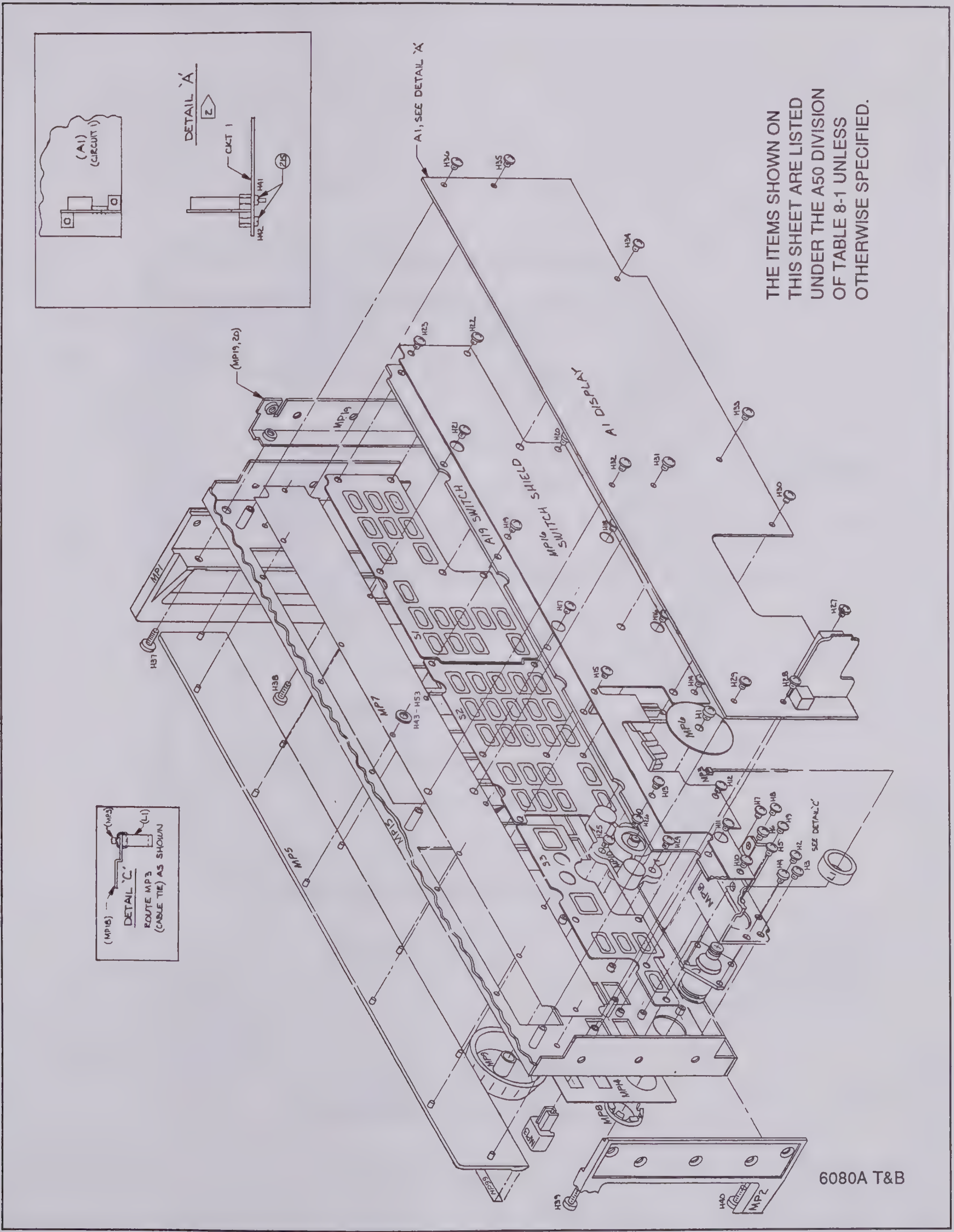

MP101
MP104
H903
H301
W36
W18
TO A1 DISPLAY ON A50 FRONT PANEL
W18
W36
H302
H303
MP5
H901
H902
MP4
MP9
W17
TO A16 IEEE BOARD ON REAR PANEL A70
H912
H910
H907
H911
H906
A13 CONTROLLER
U3
A80 H904
H201
H909
H908
H905
H304
A80 MP66
H904
H309
W37
H206
H207
H208
H310
TO VARIOUS POINTS ON A60 SYNTHESIZER MODULE
H205
W14
H209
U2
H202
W16
TO A18 CABLE TRANSITION ON A60 SYNTHESIZER MODULE
MP6
H216
H210
MP10
H305
A80 H902
H203
A12 SUM LOOP
H211
J17
H308
A80 H905
H204
MP7
J3
W22
W19
U110
H501
H502
H215
H307
H306
W15
TO A15 POWER SUPPLY ON REAR PANEL A70
MP11
H514
H213
H513
MP23
MP8
H504
H503
H214
J8
H212
H505
A14 FM
H506
H507
W32
MP13
J8
MP12
H510
H511
H512
H508
W20 TO A15 POWER SUPPLY ON REAR PANEL A70
H509
MP24
W19
A17
W20
TO A1 DISPLAY ON A50 FRONT PANEL
MP53
MP54
MP55
CONTROLLER SIDE
TO A7 RELAY DRIVER ON A20 ATTENUATOR
H401
PART OF MP100 FILTER ASSY OUTPUT MODULE
H402
C2

THE ITEMS SHOWN ON
THIS SHEET ARE LISTED
UNDER THE A40 DIVISION
OF TABLE 8-1 UNLESS
OTHERWISE SPECIFIED.

A40 OUTPUT MODULE

6080A T&B

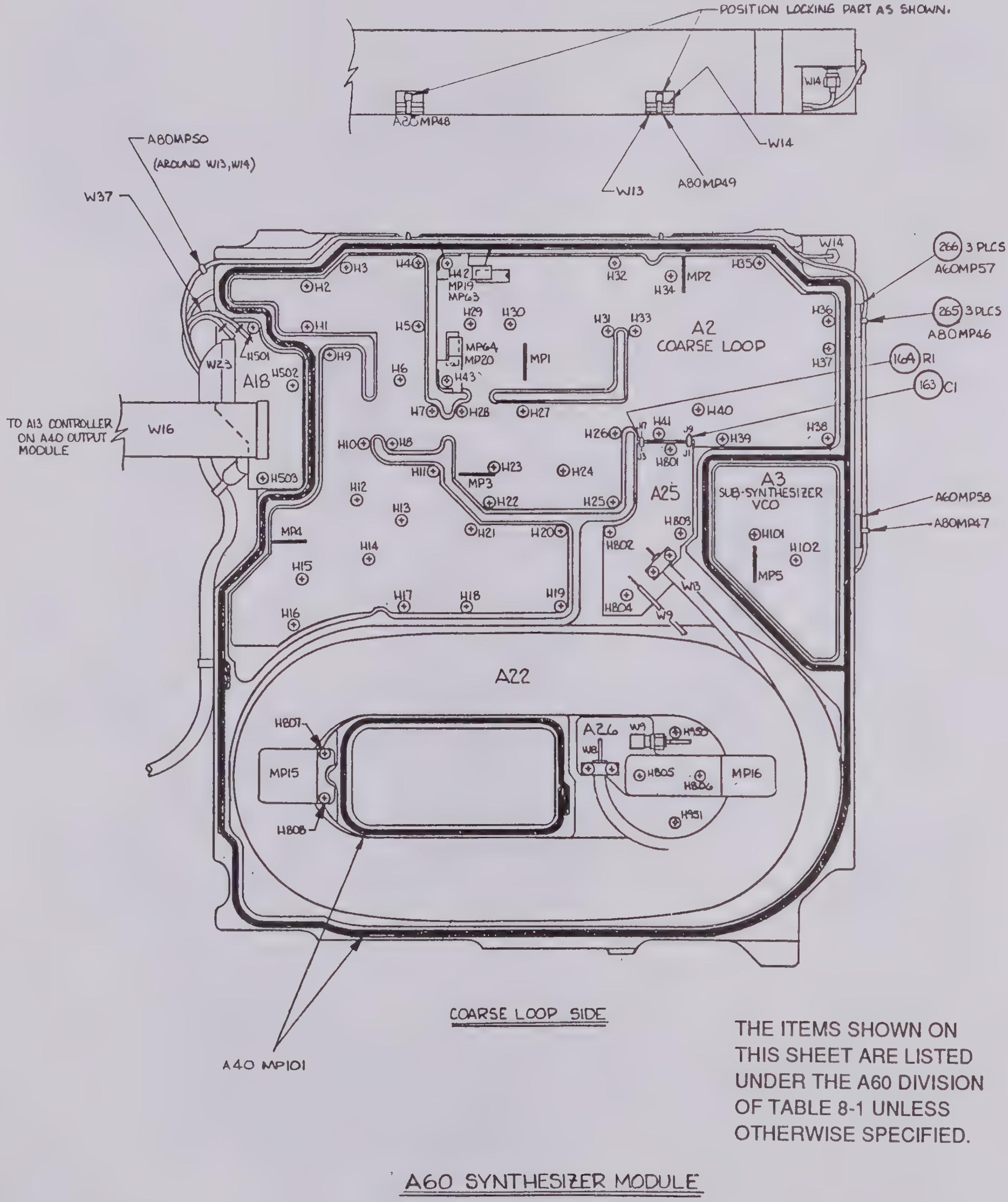
Figure 8-1. Final Assembly (cont)


DETAIL 'A'
(A1)
(CIRCUIT 1)
CKT 1
H41
H42
A1, SEE DETAIL 'A'
H36
H35
H34
H33
H32
H31
H30
H27
H28
H29
A1 DISPLAY
MP16 SWITCH SHIELD
A19 SWITCH
H22
H21
H25
H20
H19
H18
H17
H16
H15
H14
H13
H12
H11
H10
(MP19, 20)
MP19
MP1
H37
H38
MP7
H43-H53
S1
S2
S3
MP15
MP5
DETAIL 'C'
(MP18)
(MP3)
(L1)
ROUTE MP3 (CABLE TIE) AS SHOWN
SEE DETAIL 'C'
MP6
MP8
MP14
MP2
H39
H40

THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A50 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

6080A T&B

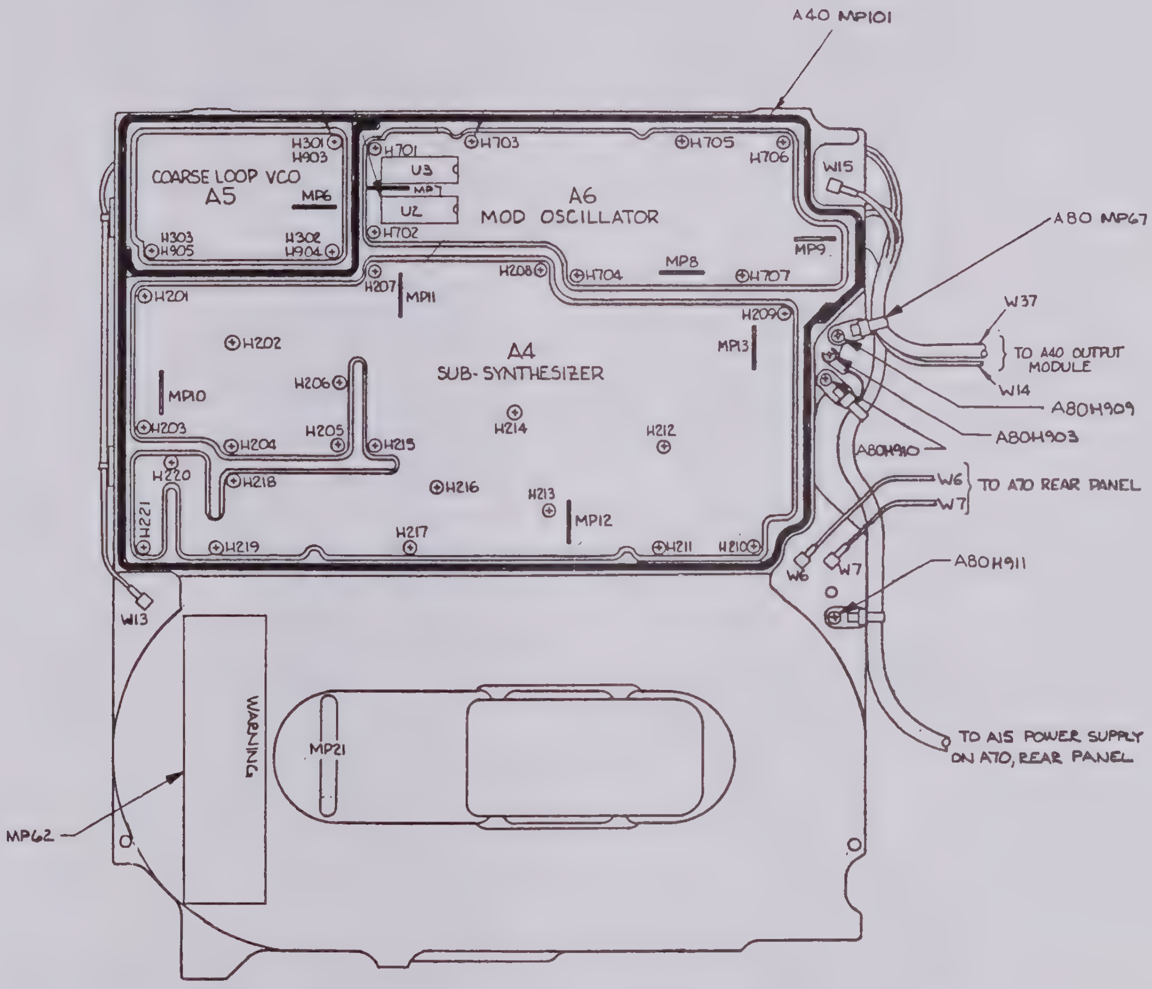
Figure 8-1. Final Assembly (cont)


POSITION LOCKING PART AS SHOWN.
W14
A80MP48
W14
W13
A80MP49
A80MP50
(AROUND W13,W14)
W37
W14
266 3 PLCS
A60MP57
265 3 PLCS
A80MP46
16A R1
163 C1
H3
H2
H4
H42
MP19
MP63
H32
H34
MP2
H35
H1
H5
H29
H30
H31
H33
A2
COARSE LOOP
H36
H37
H501
W23
A18
H502
H9
H6
MP64
MP20
H43
MP1
TO A13 CONTROLLER ON A40 OUTPUT MODULE
W16
H7
H28
H27
H40
H26
J7
H41
J9
H39
H38
J3
H801
J1
H10
H8
H11
H23
H24
MP3
H503
H12
H13
H22
H25
A25
A3
SUB-SYNTHESIZER VCO
A60MP58
A80MP47
H803
H101
MP4
H14
H21
H20
H802
H102
MP5
H15
H17
H18
H19
W13
H16
H804
W9
A22
H807
A26
W9
H950
W8
MP15
H805
H806
MP16
H951
H808
COARSE LOOP SIDE
A40 MP101
A60 SYNTHESIZER MODULE

THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A60 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

6080A T&B

Figure 8-1. Final Assembly (cont)

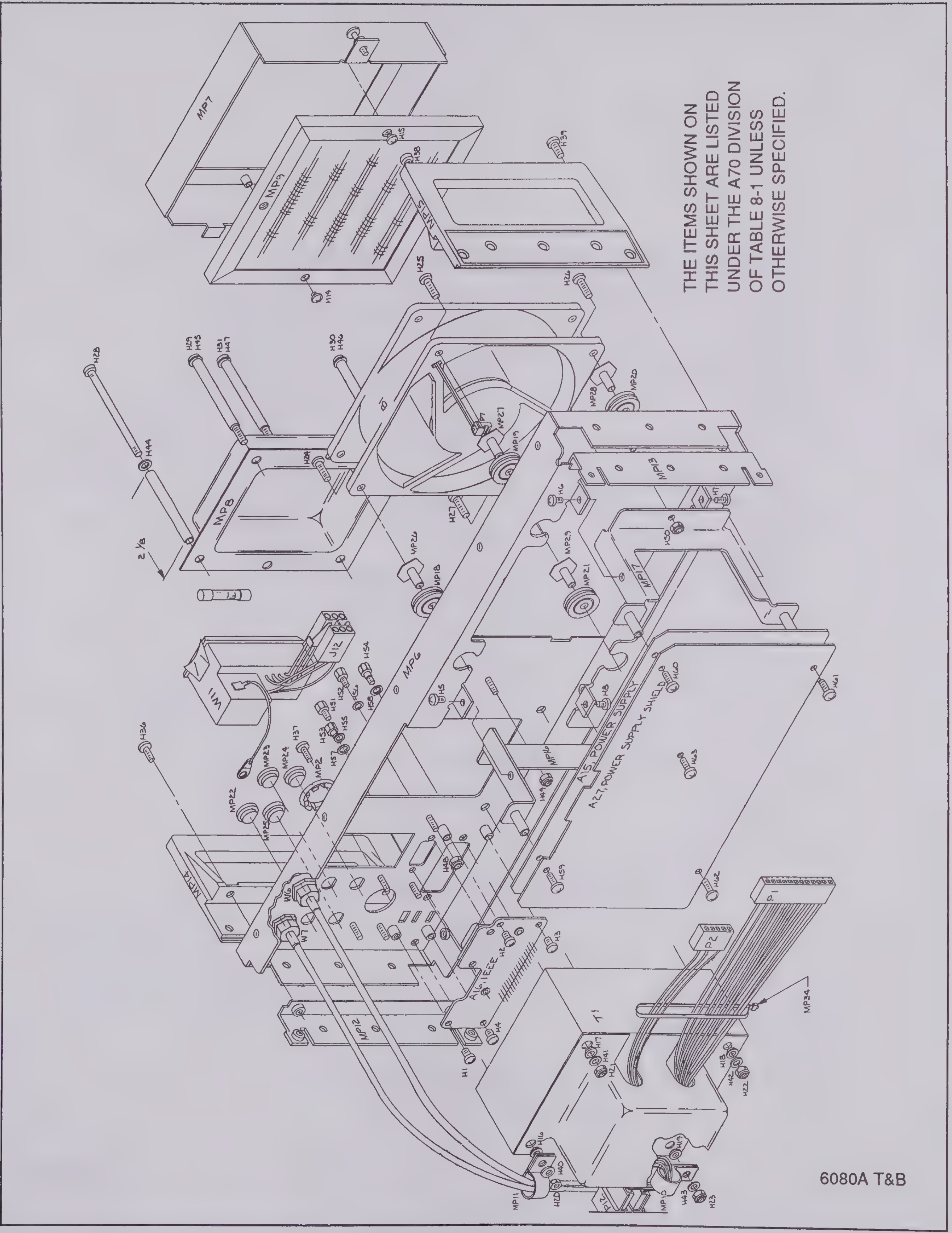

A40 MP101
H301
H903
COARSE LOOP VCO
A5
MP6
H303
H905
H302
H904
H701
H703
H705
H706
W15
U3
MP7
U2
H702
A6
MOD OSCILLATOR
MP8
MP9
A80 MP67
H208
H704
H707
H207
MP11
H201
H209
W37
H202
A4
SUB-SYNTHESIZER
MP13
TO A40 OUTPUT MODULE
W14
A80H909
A80H903
H206
MP10
H203
H204
H205
H215
H214
H212
A80H910
H220
H218
H216
H213
MP12
W6
W7
TO A70 REAR PANEL
H221
H219
H217
H211
H210
W6
W7
A80H911
W13
WARNING
MP21
TO A15 POWER SUPPLY ON A70, REAR PANEL
MP62

SUBSYNTHESIZER SIDE

THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A60 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

A60 SYNTHESIZER MODULE

Figure 8-1. Final Assembly (cont)


MP7
H15
MP9
H38
H39
MP15
H14
H25
H26
H28
H29
H45
H31
H47
H30
H46
H44
2 1/8
MP8
H24
P7
MP27
MP19
MP28
MP20
MP13
H6
H7
H27
MP26
MP18
MP29
MP21
H50
MP17
F1
J12
W11
H54
MP6
H5
H8
H36
H51
H52
H56
H58
H53
H55
H37
H57
MP23
MP24
MP2
MP22
MP25
MP16
H49
A15, POWER SUPPLY
A27, POWER SUPPLY SHIELD
H60
H61
H63
MP14
W6
W7
H48
H59
H62
P1
P2
H2
H3
A16, IEEE
MP34
MP12
H4
T1
H1
H17
H41
H21
H18
H42
H22
H16
H40
H19
MP11
H20
P12
MP10
H43
H23

THE ITEMS SHOWN ON THIS SHEET ARE LISTED UNDER THE A70 DIVISION OF TABLE 8-1 UNLESS OTHERWISE SPECIFIED.

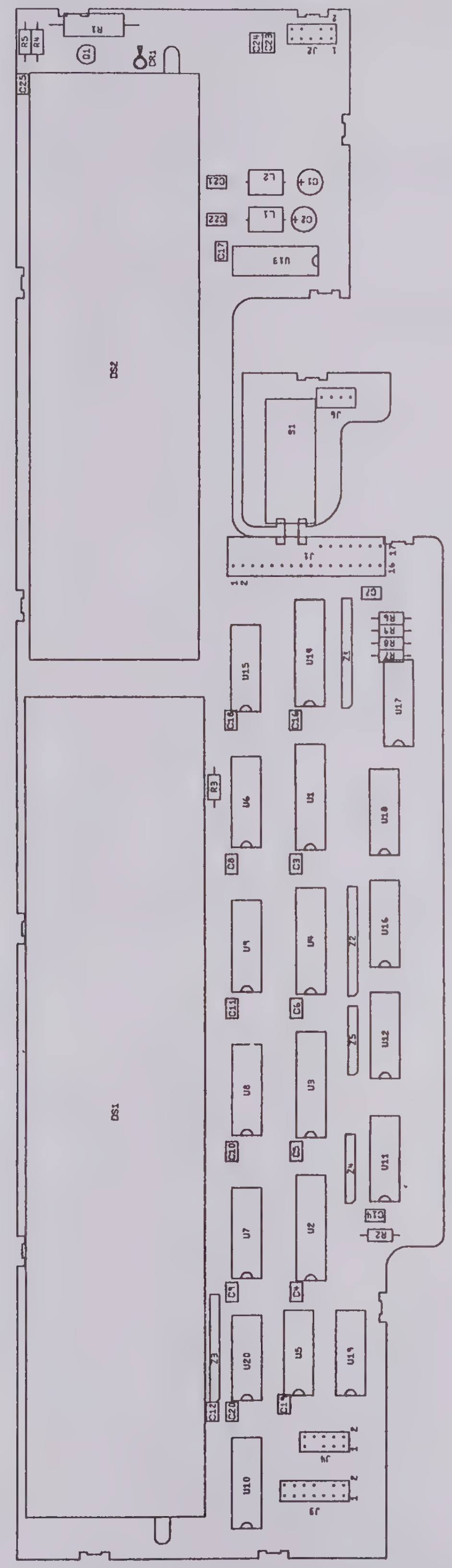
6080A T&B

Figure 8-1. Final Assembly (cont)

Table 8-2. A1 Display PCA
(See Figure 8-2.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1		CAP,TA,4.7UF,+-20%,50V	832675	56289	199D475X0050DG2	1	
C	2		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	1	
C	3- 6, 8-		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	20	
C	12, 14, 16-			837526				
C	25			837526				
C	7		CAP,CER,1000PF,+-20%,100V,X7R	816181	04222	SR071C102MAATR1A	1	
CR	1		LED,YELLOW,T1,24 MCD	854547	28480	HLMP-1440	1	
DS	1		DISPLAY,VACUUM FLUORESCENT,FREQUENCY	812685	0BW21	812685	1	
DS	2		DISPLAY,VACUUM FLUORESCENT,AMPLITUDE	812693	0BW21	812693	1	
H	1, 2		SPACER,SWAGE,RT ANG,AL,6-32,.375	837856	55566	7229-B-A-6	2	
L	1, 2		CHOKE,6TURN	320911	89536	320911	2	
MP	1- 8		FOOT,ADHESIVE,RUBBER,BLACK,.50X.12	543488	28213	SJ-5008	8	
MP	11- 64		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	54	
MP	65		HEADER,1 ROW,.100CTR,RT ANG,36 PIN	5[illegible]3403	22526	65524-136	1	
Q	1	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	1	
R	1		RES,CC,1.5K,+-10%,1W	109413	01121	GB1521	1	
R	2		RES,CF,100K,+-5%,0.25W	573584	59124	CF1-4 104 J B	1	
R	3		RES,CF,620,+-5%,0.25W	641092	59124	CF1-4 621 J B	1	
R	4, 5		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4 103 J B	2	
R	6, 7		RES,CF,20K,+-5%,0.25W	573444	59124	CF1-4 203 J B	2	
R	8, 9		RES,CF,180,+-5%,0.25W	573048	59124	CF1-4 181 J B	2	
S	1		SWITCH,PUSHBUTTON,DPDT,PUSH-PUSH	836361	31918	NE182UEESP	1	
U	1- 4	*	IC,CMOS,OCTAL D F/F W/RESET	743286	18324	N74HCT273N	4	
U	5, 18, 19	*	IC,CMOS,DUAL D F/F,+EDG TRG,W/CLR	741702	04713	SN74HC74N	3	
U	6- 10	*	IC,BIPLR,8CHNL FLOURESCNT DISPLY DRVR	535799	56289	UDN-6118A	5	
U	11	*	IC,CMOS,RETRG MONOSTAB MULTIVB W/CLR	741496	27014	MM74HC123AN	1	
U	12	*	IC,CMOS,HEX SCHMITT TRIGGER	723320	04713	MC74HC14N	1	
U	13, 15	*	IC,74HC05,HEX INVERTER W/OPEN DRAIN	854018	01295	SN74HC05N	2	
U	14	*	IC,CMOS,OCTL LINE DRVR W/3-ST OUT	741892	01295	SN74HCT244N	1	
U	16	*	IL,CMOS,QUAD 2 INPUT AND GATE	741801	01295	SN74HC08N	1	
U	17	*	IC,CMOS,QUAD 2 IN NAND W/SCHMT	740852	18324	74HCT132N	1	
U	20	*	IC,CMOS,3-8 LINE DCDR W/ENABLE	773036	01295	SN74HC138N	1	
XCR	1		SPACER LED	471094	89536	471094	1	
Z	1- 3		RES,CERM,SIP,10 PIN,9 RES,100K,+-2%	461038	91637	CSC10A-01-104G	3	
Z	4		RES,CERM,SIP,6 PIN,5 RES,10K,+-2%	500876	91637	CSC06A-01-103G	1	
Z	5		RES,CERM,SIP,6 PIN,5 RES,4.7K,+-2%	494690	91637	CSC06A-01-472G	1	

An * in 'S' column indicates a static-sensitive part.


R1
R5
R4
Q1
CR1
C24
C23
J2
C25
C21
L2
C1
C22
L1
C2
C17
U13
DS2
J6
S1
J1
C7
R6
R9
R8
R7
U15
U14
Z1
U17
C16
C15
R3
U6
U1
U18
C8
C3
U9
U4
Z2
U16
C11
C6
Z5
U12
U8
U3
DS1
C10
C5
Z4
U11
C19
R2
U7
U2
C9
C4
Z3
U20
U5
U19
C12
C20
C14
J4
J3
U10

6082A-1650

Figure 8-2. A1 Display PCA

Table 8-3. A2 Coarse Loop PCA
(See Figure 8-3.)

REFERENCE DESIGNATOR -A>	NUMERICS	S	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTE
C	101,218		CAP,POLYES,0.47UF,+-10%,50V	697409	60935	185-2/0.47/K/0050/RAB	2	
C	102,107,206,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	74	
C	207,217,219,			837526				
C	221,222,226,			837526				
C	227,230,236-			837526				
C	238,245,249,			837526				
C	253-263,265,			837526				
C	266,270,305-			837526				
C	312,410,411,			837526				
C	415,417,424,			837526				
C	427,429,507,			837526				
C	508,510-512,			837526				
C	517,520-522,			837526				
C	526-528,531-			837526				
C	536,539,540,			837526				
C	543,548,619,			837526				
C	630,638,639,			837526				
C	642,651			837526				
C	103,605		CAP,CER,220PF,+-2%,100V,C0G	812131	04222	SR291A221GAATR1A	2	
C	104,231,232		CAP,POLYES,0.022UF,+-10%,50V	715268	60935	185-2/.022/K/0050/RAB	3	
C	105,106,239,		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	62643	KME50VB47RM6X11RP	18	
C	240,242,243,			822403				
C	246,247,250,			822403				
C	251,274,502,			822403				
C	506,541,542,			822403				
C	601,603,613			822403				
C	201,302,401,		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	11	
C	402,404,413,			837609				
C	414,611,614,			837609				
C	653,654			837609				
C	204,210,273,		CAP,CER,0.01UF,+-20%,50V,X7R	816249	04222	SR075C103MAATR1A	26	
C	406-409,501,			816249				
C	513,516,518,			816249				
C	544,602,606,			816249				
C	609,610,612,			816249				
C	615,620,624,			816249				
C	625,640,641,			816249				
C	646,647,652			816249				
C	211		CAP,CER,470PF,+-20%,100V,X7R	837617	04222	SR151C471MATR2A	1	
C	212		CAP,POLYPR,2200PF,+-5%,100V	854505	68919	FKP2222J100V	1	
C	213		CAP,CER,150PF,+-2%,100V,C0G	512988	04222	SR151A151JAT	1	
C	214,216,234		CAP,POLYPR,4700PF,+-5%,63V	854513	68919	FKP2472J63V	3	
C	215		CAP,CER,390PF,+-2%,50V,C0G	820530	04222	SR595A391GAATR1A	1	
C	220		CAP,POLYES,1UF,+-10%,50V	733089	60935	185-2/1/K/0050/R/A/B	1	
C	223,224		CAP,POLYES,0.22UF,+-10%,50V	706028	60935	185-2/0.22/K/0050/RCB	2	
C	225		CAP,POLYES,0.1UF,+-10%,50V	649913	60935	185-2/0.1/K/0050/R/A/B	1	
C	228,229		CAP,POLYES,2.2UF,+-10%,50V	854500	40402	MKT1826225055	2	
C	233,267		CAP,POLYES,0.01UF,+-10%,50V	715037	60935	185-2/0.01/K/0050/RAB	2	
C	235		CAP,POLYES,2200PF,+-10%,50V	832683	60935	185-2/222/K/0050/R/A/B	1	
C	264		CAP,TA,1UF,+-20%,35V	697417	56289	199D105X0035AG2	1	
C	301,303,304,		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	5	
C	313,314			837542				
C	403		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	1	
C	405		CAP,CER,27PF,+-2%,100V,C0G	812107	04222	SR291A270GAATR1A	1	
C	412		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	1	
C	421		CAP,CER,1.5PF,+-0.25PF,100V,C0K	812164	04222	SR071A1R5CAATR1A	1	
C	422		CAP,CER,2.2PF,+-0.25PF,100V,C0J	812099	04222	SR071A2R2CAATR1A	1	
C	423		CAP,CER,1.8PF,+-0.25PF,100V,C0K	512897	51406	RPE110C0K1R8C1	1	
C	425,426		CAP,CER,1.2PF,+-0.25PF,100V,C0K	543256	51406	RPE110C0K1R2C1	2	
C	428		CAP,AL,470UF,+-20%,16V,SOLV PROOF	875497	62643	KME16VB471M10X12FT	1	
C	430		CAP,CER,3.9PF,+-0.25PF,50V,C0G,0805	493874	04222	08055A3R9CAT065B	1	
C	509,547,549		CAP,TA,10UF,+-20%,10V	714766	56289	199D106X0010BG2	3	
C	514		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	1	
C	519,550		CAP,CER,270PF,+-5%,50V,C0G	658898	04222	SR595A271JAATR1A	2	
C	523-525,537,		CAP,CER,4700PF,+-20%,100V,X7R	866426	04222	SR151C472MAATR2A	5	
C	538			866426				
C	529		CAP,TA,2.2UF,+-10%,35V	697433	56289	199D225X9035BG2	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-3. A2 Coarse Loop PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C 530		CAP,POLYES,0.047UF,+-10%,50V	820548	60935	185-2/.047/K/0050/R/A/B	1	
C 545		CAP,CER,12PF,+-2%,50V,C0G	715169	04222	SR591A120GAATR1A	1	
C 546		CAP,TA,39UF,+-20%,20V	358234	56289	199D396X0020EA2	1	
C 604		CAP,CER,33PF,+-2%,100V,C0G	838466	04222	SR071A330GAATR1A	1	
C 607		CAP,CER,4.7PF,+-0.25PF,100V,C0H	875455	04222	SR151A4R7CAATR2A	1	
C 616,617,622,		CAP,CER,82PF,+-2%,100V,C0G	512350	04222	SR291A820GAATR1A	6	
C 623,643,649			512350				
C 644		CAP,CER,10PF,+-2%,100V,C0G	875450	04222	SR151A100GAATR2A	1	
C 650		CAP,CER,10PF,+-2%,50V,C0G	713875	04222	SR595A100GAATR1A	1	
CR 101,102,202,	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	6	
CR 203,601,602	*		313247				
CR 103,204,205,	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	7	
CR 501,505-507	*		698720				
CR 201	*	ZENER,UNCOMP,3.9V,10%,20.0MA,0.4W	698654	04713	IN748-SR4348RL	1	
CR 206	*	ZENER,UNCOMP,5.1V,5%,20MA,0.4W	722926	04713	1N751A	1	
CR 207	*	ZENER,UNCOMP,10.0V,10%,20.0MA,0.4W	180406	04713	1N758	1	
CR 402,403	*	DIODE,SI,PIN, RF ATTENUATING	508077	33025	MA 4P523	2	
CR 503	*	ZENER,UNCOMP,9.1V,5%,14.0MA,0.4W	386557	04713	1N960B	1	
CR 508	*	ZENER,UNCOMP,12.0V,5%,10.5MA,0.4W	249052	04713	IN963B	1	
CR 603-605		DIODE,SI,VARACTOR,PIV= 28V	741504	25403	BB405B	3	
J 4, 11- 16,		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	37	
J 18			866764				
J 5- 8		CONN,COAX,SMB(M),PWB OR PANEL	512095	98291	051-051-0429-220	4	
J 9, 17		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	2	
L 201,202,503-		INDUCTOR,0.68UH,+-10%,221MHZ,SHLD	320937	24759	MR-0.68	8	
L 506,609,614			320937				
L 203		INDUCTOR,2.2UH,+-5%,108MHZ,SHLD	806547	24759	MR-2.2	1	
L 204,502		INDUCTOR,10UH,+-10%,53MHZ,SHLD	249078	24759	MR-10	2	
L 205		INDUCTOR, VARIABLE, 14UH	812792	89536	812792	1	
L 206-211,301,		CHOKE,6TURN	320911	89536	320911	10	
L 507,508,602			320911				
L 401,402,405,		INDUCTOR,10 TURNS	463448	89536	463448	4	
L 406			463448				
L 501		INDUCTOR,0.82UH,+-10%,200MHZ,SHLD	320945	24759	MR-0.82	1	
L 510		INDUCTOR,5.6UH,+-5%,69MHZ,SHLD	867056	24759	MR-5.6	1	
L 601		VAR. 0.402UH INDUCTOR, MODIFIED	854646	02113	142-10J08S	1	
L 603		INDUCTOR,1.5UH,+-10%,140MHZ	854612	91637	IM-21.5UH10%	1	
L 604,605		INDUCTOR,0.22UH,+-10%,510MHZ	854604	91637	IM-2.22UH10%	2	
L 606		INDUCTOR,VAR,0.342,+-20%	875559	02113	146-08J08	1	
L 607		CORE,TOROID,FERRITE,.047X.138X.118	321182	88978	56-590-65-4B	1	
L 611,615		INDUCTOR,0.39UH,+-10%,365MHZ	854596	91637	IM-2.39UH10%	2	
L 612,613		INDUCTOR,VAR,0.070UH,+-11%	854591	02113	150-02J08	2	
MP 31, 32		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	11	
P 2		PIN FEED THRU	812735	20584	812735	1	
P 3- 6		JUMPER,REC,2 POS,.100CTR,.025 SQ POST	530253	00779	530153-2	4	
Q 101,105,106	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	832170	04713	MPS6520RLRA	3	
Q 102	*	TRANSISTOR,SI,NPN,DUAL,TO-5	640656	27014	LM394CH	1	
Q 103,104	*	TRANSISTOR,SI,PNP,40V,.2W,TO-92	875380	12040	SX-68061	2	
Q 201-204,502	*	TRANSISTOR,SI,NMOS,1W,TO-237	875419	17856	VE0091-TR5	5	
Q 205,206,607-	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	535013	04713	BFR91	6	
Q 610	*		535013				
Q 403,404	*	TRANSISTOR,SI,PNP,T092	698233	04713	2N3906RLRA	2	
Q 405,406	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	722256	04713	MRF581	2	
Q 501	*	TRANSISTOR,SI,PNP,T092	698290	04713	MPS6562RLRA	1	
Q 504,505	*	TRANSISTOR,SI,PNP,HI-SPEED SWTICH	875385	04713	2N5771RLRA	2	
Q 506	*	TRANSISTOR,SI,N-DMOS FET,TO-72	783308	17856	SD215DE	1	
Q 606	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	248351	04713	MPS918	1	
Q 611	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	1	
R 101		RES,MF,90.9K,+-1%,0.125W,100PPM	720581	91637	CMF55 9092 F T-1	1	
R 102		RES,VAR,CERM,10K,+-10%,0.5W	309674	32997	3386R-1-103	1	
R 103,245,246		RES,MF,4.99K,+-1%,0.125W,100PPM	714923	91637	CMF55 4991 F T-1	3	
R 104		RES,MF,200K,+-1%,0.125W,100PPM	719831	91637	CMF55 2003 F T-1	1	
R 105,244,247,		RES,MF,10K,+-1%,0.125W,100PPM	719476	91637	CMF55 1002 F T-1	4	
R 252			719476				
R 106		RES,MF,3.32K,+-1%,0.125W,100PPM	866269	91637	CMF55 3321 F T-1	1	
R 107,110,115,		RES,MF,499,+-1%,0.125W,100PPM	816462	91637	CMF55 4990 F T-1	6	
R 229,271,530			816462				
R 108		RES,MF,1.5K,+-1%,0.125W,100PPM	719682	91637	CMF55 1501 F T-1	1	
R 109		RES,MF,3.16K,+-1%,0.125W,100PPM	866264	91637	CMF55 3161 F T-1	1	
R 111		RES,MF,10,+-1%,0.125W,100PPM	719443	91637	CMF5S5 10R0 F T-1	1	
R 112,117		RES,MF,49.9,+-1%,0.125W,100PPM	720318	91637	CMF55 49R9 F T-1	2	
R 113		RES,MF,100,+-1%,0.125W,100PPM	719450	91637	CMF55 1000 F T-1	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-3. A2 Coarse Loop PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE
R	114,116		RES,MF,2.32K,+-1%,0.125W,100PPM	719914	91637	CMF55 2321 F T-1	2	
R	118,124		RES,MF,301,+-1%,0.125W,100PPM	720029	91637	CMF55 3010 F T-1	2	
R	119		RES,MF,127,+-1%,0.125W,100PPM	866199	91637	CMF55 1270 F T-1	1	
R	120,220		RES,MF,698,+-1%,0.125W,100PPM	866228	91637	CMF55 6980 F T-1	2	
R	121,122		RES,MF,30.1,+-1%,0.125W,100PPM	855242	91637	CMF55 30R1 F T-1	2	
R	123		RES,MF,154,+-1%,0.125W,100PPM	866202	91637	CMF55 1540 F T-1	1	
R	125		RES,MF,374,+-1%,0.125W,100PPM	866335	91637	CMF55 3740 F T-1	1	
R	201,202		RES,CF,18,+-5%,0.125W	740035	59124	CF1-8RDS2 180 J B	2	
R	203-208,213,		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	11	
R	413,417,421,			573170				
R	612			573170				
R	209,214,217		RES,MF,196,+-1%,0.125W,100PPM	866210	91637	CMF55 1960 F T-1	3	
R	210,260,308,		RES,MF,51.1,+-1%,0.25W,100PPM	799650	91637	CCF-5051R1F	6	
R	408,610,618			799650				
R	211		RES,MF,33.2,+-1%,0.25W,100PPM	799676	91637	CCF-5033R2F	1	
R	212,528		RES,CF,100K,+-5%,0.25W	573584	59124	CF1-4 104 J B	2	
R	215		RES,MF,453,+-1%,0.125W,100PPM	720268	91637	CMF55 4530 F T-1	1	
R	216		RES,MF,1.47K,+-1%,0.125W,100PPM	719658	91637	CMF55 1471 F T-1	1	
R	218		RES,MF,825,+-1%,0.125W,100PPM	866251	91637	CMF55 8250 F T-1	1	
R	219,223,225,		RES,MF,1K,+-1%,0.125W,100PPM	719468	91637	CMF55 1001 F T-1	8	
R	226,238,508,			719468				
R	509,529			719468				
R	221		RES,VAR,CERM,100,+-10%,0.5W	275735	80294	3386R-1-101	1	
R	222		RES,MF,1.37K,+-1%,0.125W,100PPM	866256	91637	CMF55 1371 F T-1	1	
R	224		RES,MF,3.01K,+-1%,0.125W,100PPM	720037	91637	CMF55 3011 F T-1	1	
R	227		RES,VAR,CERM,500,+-10%,0.5W	325613	80294	3386R-1-501	1	
R	228		RES,MF,249,+-1%,0.125W,100PPM	816454	91637	CMF55 2490 F T-1	1	
R	230		RES,CF,3,+-5%,0.25W	640961	59124	CF1-4 3R0 J B	1	
R	231		RES,MF,86.6,+-1%,0.125W,100PPM	866181	91637	CMF55 86R6 F T-1	1	
R	232		RES,MF,178,+-1%,0.125W,100PPM	866207	91637	CMF55 1780 F T-1	1	
R	233		RES,CF,6.2,+-5%,0.25W	641001	59124	CF1-4 6R2 J B	1	
R	234		RES,MF,365,+-1%,0.125W,100PPM	459859	91637	CMF55 3650 F T-1	1	
R	235		RES,CF,12,+-5%,0.25W	641035	59124	CF1-4 120 J B	1	
R	236		RES,MF,715,+-1%,0.125W,100PPM	866249	91637	CMF55 7150 F T-1	1	
R	237		RES,CF,24,+-5%,0.25W	572974	59124	CF1-4 240 J B	1	
R	242,524,527		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	3	
R	243		RES,CF,13K,+-5%,0.25W	573410	59124	CF1-4 133 J B	1	
R	248,250,301		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	3	
R	249,251		RES,CF,4.7K,+-5%,0.25W	721571	59124	CF1-4 VT 472 J B	2	
R	261		RES,MF,845,+-1%,0.25W,100PPM	854398	91637	CCF-508450F	1	
R	262,636,648		RES,MF,100,+-1%,0.25W,100PPM	799668	91637	CCF-501000F	3	
R	264,634		RES,MF,392,+-1%,0.25W,100PPM	854419	91637	CCF-503920F	2	
R	266,270,304,		RES,MF,68.1,+-1%,0.25W,100PPM	830679	91637	CCF-5068R1F	5	
R	607,613			830679				
R	268		RES,MF,40.2,+-1%,0.25W,100PPM	854393	91637	CCF-5040R2F	1	
R	302		RES,CF,510,+-5%,0.25W	573139	59124	CF1-4 511 J B	1	
R	305		RES,MF,182,+-1%,0.25W,100PPM	799726	91637	CCF-501820F	1	
R	309,310		RES,CF,180,+-5%,0.25W	573048	59124	CF1-4 181 J B	2	
R	401		RES,CF,270,+-5%,0.125W	557231	59124	RDS21-8 271 J B	1	
R	402		RES,CF,150,+-5%,0.125W	854786	59124	RDS21-8151J	1	
R	403		RES,CF,68,+-5%,0.125W	830893	59124	RDS21-8 680 J B	1	
R	404		RES,CF,75,+-5%,0.125W	740068	59124	CF1-8RDS2 750 J B	1	
R	405,411		RES,CF,330,+-5%,0.25W	830596	59124	CF1-4 VT 331 J B	2	
R	406		RES,CF,240,+-5%,0.25W	573063	59124	CF1-4 241 J B	1	
R	407,409		RES,MF,121,+-1%,0.25W,100PPM	799734	91637	CCF-501210F	2	
R	410		RES,CF,91,+-5%,0.125W	854380	59124	RDS21-8910J	1	
R	412		RES,MF,3.65K,+-1%,0.125W,100PPM	720144	91637	CMF55 3651 F T-1	1	
R	414		RES,MF,31.6,+-1%,0.5W,100PPM	772152	91637	CMF65 31R6 F T-1	1	
R	415		RES,MF,4.87K,+-1%,0.125W,100PPM	720292	91637	CMF55 4871 F T-1	1	
R	416		RES,MF,4.64K,+-1%,0.125W,100PPM	866272	91637	CMF55 4641 F T-1	1	
R	422,425		RES,MF,301,+-1%,0.25W,100PPM	799916	91637	CCF-503010F	2	
R	423,424,426,	*	RES,CERM,12,+-5%,.125W,200PPM,1206	845458	91637	CRCW1206-12R0JB02	4	
R	427	*		845458				
R	428		RES,CF,7.5,+-5%,0.25W	641019	59124	CF1-4 7R5 B	1	
R	501		RES,MF,15K,+-1%,0.125W,100PPM	719690	91637	CMF55 1502 F T-1	1	
R	502		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	
R	503,521,523		RES,CF,270,+-5%,0.25W	573071	59124	CF1-4 271 J B	3	
R	504		RES,CF,2K,+-5%,0.25W	573238	59124	CF1-4 202 J B	1	
R	505		RES,MF,25.5K,+-1%,0.125W,25PPM	851212	91637	CMF55 2552 F T-9	1	
R	510		RES,MF,4.53K,+-1%,0.125W,25PPM	851238	91637	CMF55 4531 F T-9	1	
R	511,532		RES,MF,2K,+-1%,0.125W,100PPM	719815	91637	CMF55 2001 F T-1	2	
R	512		RES,MF,5.49K,+-1%,0.125W,100PPM	720383	91637	CMF55 5491 F T-1	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-3. A2 Coarse Loop PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R 513		RES,MF,30.1K,+-1%,0.125W,100PPM	720045	91637	CMF55 3012 F T-1	1	
R 517		RES,CF,200,+-5%,0.25W	573055	59124	CF1-4 201 J B	1	
R 518		RES,CF,270,+-5%,0.25W	810424	59124	CF1-4 VT 271 J B	1	
R 519,536		RES,CF,30,+-5%,0.25W	866343	59124	CF1-4 300 J B	2	
R 522		RES,CF,18,+-5%,0.25W	658773	59124	CF1-4 180 J B	1	
R 525,526		RES,CF,51,+-5%,0.25W	572990	59124	CF1-4 510 J B	2	
R 537		RES,MF,3.48K,+-1%,0.125W,100PPM	832071	91637	CMF55 3481 F T-1	1	
R 538		RES,CF,240,+-5%,0.25W	830588	59124	CF1-4 VT 241 J B	1	
R 539		RES,CF,1K,+-5%,0.25W	780585	59124	CF1-4 VT 102 J B	1	
R 601,603,604		RES,MF,3.01K,+-1%,0.25W,100PPM	854356	91637	CCF-503011F	3	
R 602		RES,MF,2.15K,+-1%,0.25W,100PPM	854364	91637	CCF-502151F	1	
R 605		RES,MF,110,+-1%,0.25W,100PPM	799809	91637	CCF-501100F	1	
R 606,614,615		RES,MF,82.5,+-1%,0.25,100PPM	799783	91637	CCF-5082R5F	3	
R 608		RES,MF,2.74K,+-1%,0.25W,100PPM	854427	91637	CCF-502741F	1	
R 609		RES,MF,1K,+-1%,0.25W,100PPM	799791	91637	CCF-501001F	1	
R 611,633		RES,CF,2.2K,+-5%,0.25W	573246	59124	CF1-4 222 J B	2	
R 616		RES,MF,18.2,+-1%,0.25W,100PPM	799817	91637	CCF-5018R2F	1	
R 617		RES,VAR,CERM,100,+-20%,0.5W	193052	80294	3329H-1-101	1	
R 630		RES,MF,3.65K,+-1%,0.25W,100PPM	854443	91637	CCF-503651F	1	
R 631		RES,CF,5.1,+-5%,0.125W	854372	59124	RDS21-85R1J	1	
R 632,644		RES,MF,200,+-1%,0.25W,100PPM	799759	91637	CCF-502000F	2	
R 635		RES,MF,2.26K,+-1%,0.25W,100PPM	854422	91637	CCF-502261F	1	
R 637		RES,MF,15,+-1%,0.25W,100PPM	799767	91637	CCF-5015R0F	1	
R 638		RES,MF,2.87K,+-1%,0.25W,100PPM	854430	91637	CCF-502871F	1	
R 639		RES,MF,221,+-1%,0.25W,100PPM	799908	91637	CCF-502210F	1	
R 640		RES,MF,2.94K,+-1%,0.25W,100PPM	854435	91637	CCF-502941F	1	
R 641		RES,MF,249,+-1%,0.25W,100PPM	854414	91637	CCF-502490F	1	
R 642		RES,CF,8.2,+-5%,0.125W	854377	59124	RDS21-88R2J	1	
R 643		RES,MF,150,+-1%,0.25W,100PPM	838508	91637	CCF-501500F	1	
S 502		SWITCH,MODULE,SPST,DIP,SEALED,6 POS	831909	00779	5-435166-1	1	
T 601		TRANSFORMER,RF,70KHZ-200MHZ,2:1	851634	1AV65	T2-1T-X65	1	
TP 1, 2, 4-		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	14	
TP 7, 10- 12,			816090				
TP 15- 19			816090				
TP 3, 8, 9,		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	4	
TP 14			512889				
U 203		MIXER,DOUBLE BALANCED,1 - 500 MHZ	733105	1AV65	SBL-1-27	1	
U 204,512	*	IC,CMOS,RETRG MONOSTAB MULTIVB W/CLR	741496	27014	MM74HC123AN	2	
U 205-207	*	IC,OP AMP,LO-NOISE,8 PIN DIP	477745	18324	NE5534AN	3	
U 208,509	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	2	
U 209,508	*	IC,OP AMP,JFET INPUT,8 PIN DIP	472779	27014	LF356N	2	
U 210	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	
U 301	*	IC,DIVIDE BY 4 PRESCALER	854690	33297	UPB582C	1	
U 302,308,309	*	IC,ECL,QUAD 2 INPUT NOR GATE	851613	04713	MC10H102P	3	
U 303,304	*	IC,ECL,QUAD 2 INPUT AND GATE	851618	04713	MC10H104P	2	
U 305,310	*	IC,ECL,HEX M/S D F/F,+EDG TRG	851782	04713	MC10H176L	2	
U 306	*	IC,ECL,QUAD 2 INPUT OR/NOR GATE	851621	04713	MC10H107P	1	
U 307	*	IC,ECL,TRIPLE 2-3-2 INPUT OR/NOR GATE	851626	04713	MC10H105P	1	
U 311	*	IC,BPLR,WIDEBAND AMPLIFIER,1200 MHZ	866439	33297	UPC1651G	1	
U 401,402,405,	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	4	
U 601	*		867049				
U 501		OSCILLATOR,10MHZ,TCXO,1PPM	866475	57693	5351	1	
U 502,511	*	IC,CMOS,QUAD 2 INPUT NAND GATE	854468	07263	74ACT00PC	2	
U 503	*	IC,CMOS,DUAL D F/F,+EDG TRG	854471	07263	74ACT74PC	1	
U 504	*	IC,FTTL,QUAD 2-1 LINE MUX	854455	27014	74F157PC	1	
U 505	*	IC,STTL,100MHZ DIV BY 2,DIV BY 5 CNTR	473835	01295	SN74S196N	1	
U 506	*	IC,ECL,DUAL D M/S F/F,W/SET&RESET	454959	04713	MC10131P	1	
U 507	*	IC,FTTL,HEX INVERTER	634444	04713	MC74F04N	1	
U 510	*	IC,COMPARATOR,HI-SPEED,14 PIN DIP	386920	18324	NE529N	1	
U 513,602	*	IC,ECL,TRIPLE LINE RECEIVER	369702	04713	MC10116P	2	
U 514	*	IC,CMOS,QUAD INPUT NOR GATE	851691	18324	74HCT02	1	
U 515	*	IC,CMOS,TRIPLE 3 INPUT AND	854781	18324	74HCT11N	1	
W 1		CABLE ASSY, RF JUMPER	861075	89536	861075	1	
Y 601		CRYSTAL,39.999MHZ,+-0.0005%,HC-35/U	855064	71034	BK-1B	1	
Z 201		RES,CERM,SIP,6 PIN,5 RES,10K,+-2%	500876	91637	CSC06A-01-103G	1	
Z 301-304		RES,CERM,SIP,8 PIN,7 RES,510,+-2%	447482	91637	CSC08A-01-511G	4	
Z 501		RES,CERM,DIP,16 PIN,8 RES,10K,+-5%	500710	91637	MDP16-03-103J	1	
Z 502,601,602		RES,CERM,SIP,6 PIN,5 RES,510,+-2%	459974	91637	CSC06A-01-511G	3	

An * in 'S' column indicates a static-sensitive part.

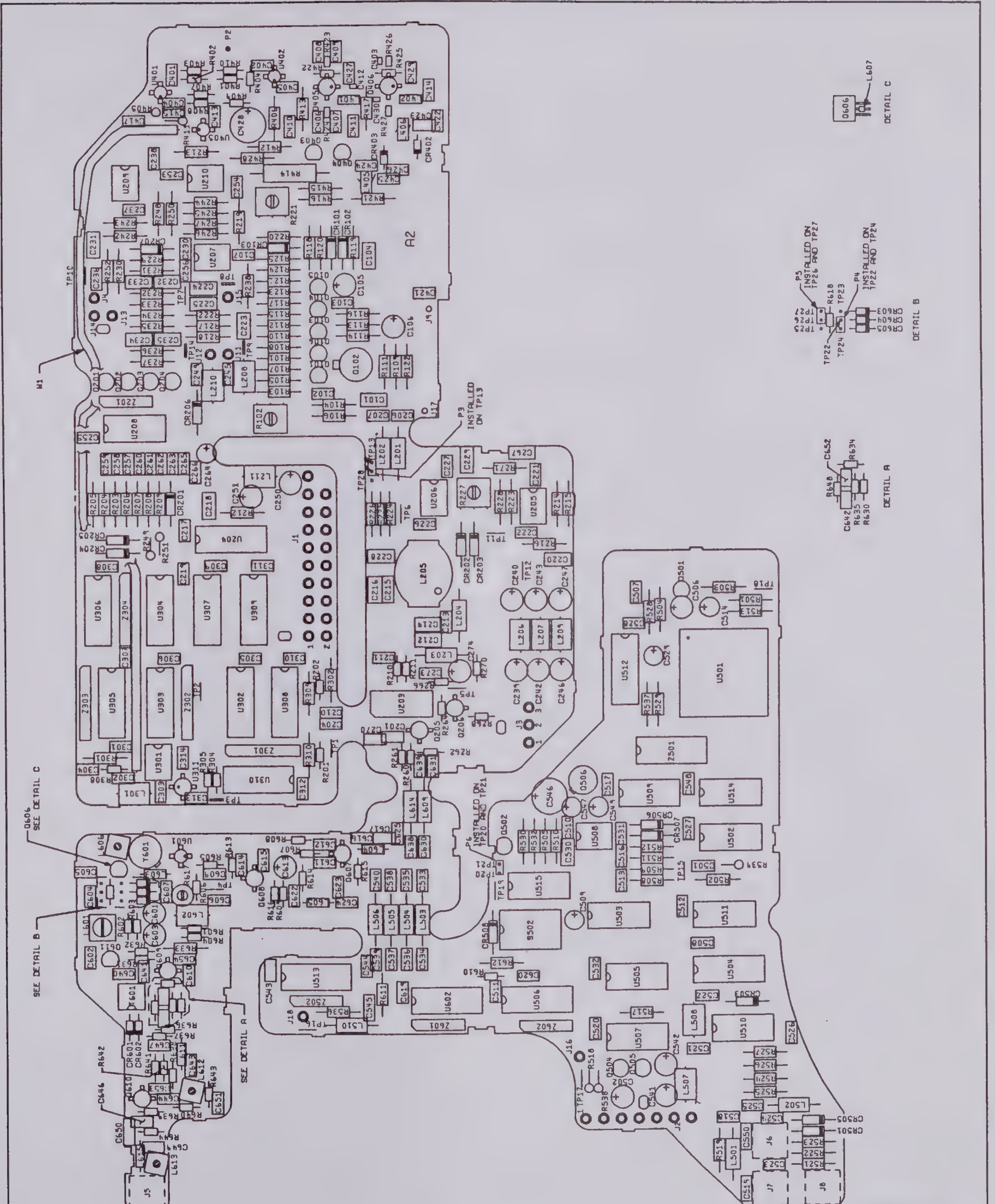
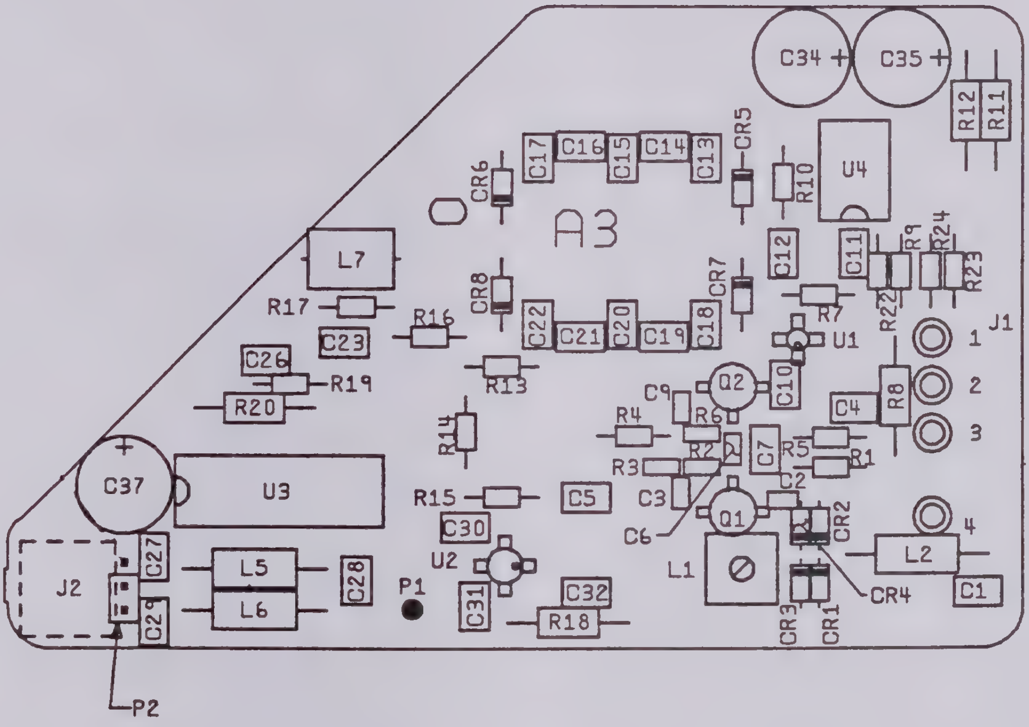

A2
W1
TP10
SEE DETAIL C
SEE DETAIL B
SEE DETAIL A
DETAIL A
DETAIL B
DETAIL C
P3 INSTALLED ON TP13
P4 INSTALLED ON TP22 AND TP24
P5 INSTALLED ON TP26 AND TP27
P6 INSTALLED ON TP20 AND TP21
J1
J5
J6
J7
J8
U501
6082A-1660

Figure 8-3. A2 Coarse Loop PCA

Table 8-4. A3 Subsynthesizer VCO PCA
(See Figure 8-4.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	1	
C	2, 6		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	2	
C	3, 9		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	2	
C	4, 5, 11,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	5	
C	26, 32			837526				
C	7		CAP,CER,1.0PF,+-0.25PF,100V,C0K	512145	51406	RPE110C0K105C1	1	
C	10, 12, 23,		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	7	
C	27, 29- 31			837609				
C	13		CAP,CER,12PF,+-2%,100V,C0G	876156	04222	SR151A120GAATR2A	1	
C	14		CAP,CER,3.3PF,+-0.25PF,100V,C0J	519330	51406	RPE110C0J3R3C1	1	
C	15		CAP,CER,18PF,+-2%,100V,C0G	876131	04222	SR151A180GAATR2A	1	
C	16		CAP,CER,12PF,+-2%,100V,C0G	376871	59660	8101-100-C0G-126G	1	
C	17		CAP,CER,8.2PF,+-0.25PF,100V,C0H	876164	04222	SR151A8R2CAATR2A	1	
C	18		CAP,CER,10PF,+-2%,100V,C0G	875450	04222	SR151A100GAATR2A	1	
C	19		CAP,CER,2.2PF,+-0.25PF,100V,C0G	362731	04222	SR15A2R2CAT	1	
C	20		CAP,CER,15PF,+-2%,100V,C0G	876169	04222	SR151A150GAATR2A	1	
C	21, 22		CAP,CER,6.8PF,+-0.25PF,100V,C0H	866553	04222	SR151A6R8CAA	2	
C	28		CAP,CER,180PF,+5%,100V,C0G	837625	04222	SR151A181JATR2A	1	
C	34, 35, 37		CAP,AL,470UF,+-20%,16V,SOLV PROOF	875497	62643	KME16VB471M10X12FT	3	
CR	1- 4		DIODE,SI,VARACTOR,PIV= 28V	741504	25403	BB405B	4	
CR	5- 8	*	DIODE,SI,PIN,SMALL SIGNAL,UHF & VHF	402776	28480	5082-3379 T-25	4	
J	2		CONN,COAX,SMB(M),PWB OR PANEL	512095	98291	051-051-0429-220	1	
L	1		INDUCTOR,.0825UH,+-5%,SHLD	845086	02113	150-04XXX-S	1	
L	2		INDUCTOR,0.68UH,+-10%,221MHZ,SHLD	320937	24759	MR-O.68	1	
L	5, 6		INDUCTOR,0.33UH,+-10%,300MHZ,SHLD	261743	24759	MR-0.33	2	
L	7		CHOKE,6TURN	320911	89536	320911	1	
MP	1- 4		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	4	
MP	6- 8		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	3	
P	1		PIN FEED THRU	812735	20584	812735	1	
P	2		JUMPER,REC,2 POS,.100CTR,.025 SQ POST	530253	00779	530153-2	1	
Q	1, 2	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	535013	04713	BFR91	2	
R	1, 4, 10		RES,MF,1K,+-1%,0.25W,100PPM	799791	91637	CCF-501001F	3	
R	2, 6	*	RES,CERM,15,+-5%,.125W,200PPM,1206	756940	91637	CRCW1206-150JB02	2	
R	3	*	RES,CERM,3K,+-5%,.125W,200PPM,1206	746511	91637	CRCW1206-3001JB02	1	
R	5		RES,MF,464,+-1%,0.25W,100PPM	801282	91637	CCF-504640F	1	
R	7		RES,MF,357,+-1%,0.25W,100PPM	782045	91637	CCF-503570F	1	
R	8		RES,MF,30.1K,+-1%,0.125W,100PPM	720045	91637	CMF55 3012 F T-1	1	
R	9		RES,MF,10K,+-1%,0.25W,100PPM	799635	91637	CCF-501002F	1	
R	11, 12		RES,CF,20,+-5%,0.25W	572958	59124	CF1-4 200 J B	2	
R	13		RES,MF,221,+-1%,0.25W,100PPM	799908	91637	CCF-502210F	1	
R	14		RES,MF,182,+-1%,0.25W,100PPM	799726	91637	CCF-501820F	1	
R	15		RES,MF,82.5,+-1%,0.25,100PPM	799783	91637	CCF-5082R5F	1	
R	16		RES,MF,33.2,+-1%,0.25W,100PPM	799676	91637	CCF-5033R2F	1	
R	17		RES,MF,200,+-1%,0.25W,100PPM	799759	91637	CCF-502000F	1	
R	18		RES,CF,300,+-5%,0.25W	643502	59124	CF1-4 301 J B	1	
R	19		RES,MF,51.1,+-1%,0.25W,100PPM	799650	91637	CCF-5051R1F	1	
R	20		RES,MF,200,+-1%,0.125W,100PPM	832063	91637	CMF55 2000 F T-1	1	
R	22		RES,MF,1.62M,+-1%,0.25W,100PPM	782060	19701	5063JD1624F	1	
R	23, 24		RES,CF,1M,+-5%,0.125W	556829	59124	RDS21-8 105 J B	2	
U	1	*	IC,BPLR,MONOLITHIC MICROWAVE IC AMP	836593	7E751	MSA-0885	1	
U	2	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	1	
U	3	*	IC,ECL,DIV BY 10,DIV BY 11 COUNTER	454900	04713	SC62844L	1	
U	4	*	IC,OP AMP,JFET IN,COMPENSTD,8 PIN DIP	418780	04713	MC34001P	1	

An * in 'S' column indicates a static-sensitive part.


A3
C34
C35
R12
R11
U4
C17
C16
C15
C14
C13
CR5
R10
CR6
L7
C12
C11
R9
R24
R22
R23
CR8
CR7
R17
R16
C22
C21
C20
C19
C18
R7
U1
J1
1
2
3
4
C23
C26
R19
R13
C9
Q2
C10
C4
R8
R20
R4
R6
R14
R2
C7
R5
R1
R3
C37
U3
R15
C5
C3
C2
Q1
CR2
C6
C30
L2
U2
L1
CR4
C1
J2
C27
L5
C28
P1
C32
L6
C31
R18
C29
CR3
CR1
P2

6082A-1661

Figure 8-4. A3 Subsynthesizer VCO PCA

Table 8-5. A4 Subsynthesizer PCA
(See Figure 8-5.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	NOTE
C	1, 2, 4,		CAP,AL,10UF,+-20%,50V,SOLV PROOF	799437	62643	KMC50VB10RM5X11RP	6	
C	5, 7, 8			799437				
C	6, 9		CAP,TA,82UF,+-20%,20V	357392	56289	199D826X0020FA2	2	
C	10, 11, 31		CAP,AL,10UF,+-20%,16V	614859	62643	LL16VB10RM5X11CS	3	
C	12, 50		CAP,TA,150UF,+-20%,15V	422576	56289	199D157X0015FA1	2	
C	17, 19, 25,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	31	
C	26, 28, 29,			837526				
C	32, 36, 40,			837526				
C	72- 75, 80,			837526				
C	90- 94, 99,			837526				
C	102,116,117,			837526				
C	149,151,152,			837526				
C	154,163,168,			837526				
C	172,177			837526				
C	27, 33, 34,		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	10	
C	70, 71, 97,			837542				
C	101,148,150,			837542				
C	153			837542				
C	76- 78		CAP,CER,22PF,+-2%,100V,C0G	866421	04222	SR151A220GAATR1A	3	
C	79,171,174		CAP,TA,39UF,+-20%,6.3V	836890	56289	199D396X06R3DG2	3	
C	98		CAP,POLYES,0.47UF,+-10%,50V	697409	60935	185-2/0.47/K/0050/R/A/B	1	
C	103		CAP,POLYCA,0.022UF,+-5%,63V	854492	68919	MKC2223J63V	1	
C	104		CAP,POLYPR,7500PF,+-2.5%,63V	854489	68919	FKP27522.563V	1	
C	105		CAP,POLYPR,1500PF,+-2.5%,100V	854641	68919	FKP2152J2.5100V	1	
C	106		CAP,POLYCA,0.056UF,+-5%,63V	854497	68919	MKC2563J63V	1	
C	107		CAP,POLYCA,0.027UF;+-10%,63V	720979	68919	MKC2-272-K-63V	1	
C	109,173,176,		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	4	
C	179			714774				
C	110,111		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	2	
C	112,180,181		CAP,CER,0.01UF,+-20%,100V,X7R	407361	04222	SR201C103MAT	3	
C	114,115		CAP,TA,10UF,+-20%,35V	816512	56289	199D106X0035DG2	2	
C	118,119		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	62643	KME50VB47RM6X11RP	2	
C	120		CAP,AL,47UF,+-20%,10V	613984	62643	LL10VB47RM6X11C3	1	
C	140,142		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	2	
C	141		CAP,CER,18PF,+-5%,50V,C0G,0805	514224	51406	GRM708C0G180J200VPB	1	
C	143-147,175		CAP,CER,1000PF,+-20%,50V,X7R,0805	514059	04222	08055C102MAT060B	6	
C	155,158,164,		CAP,POLYES,0.22UF,+-10%,50V	706028	60935	185-2/0.22/K/0050/R/C/B	4	
C	169			706028				
C	156		CAP,POLYES,0.15UF,+-10%,50V	714790	60935	185-2/.15/K/0050/R/C/B	1	
C	157		CAP,POLYES,0.033UF,+-10%,50V	715276	60935	185-2/.033/K/0050/R/A/B	1	
C	159,160		CAP,POLYES,0.1UF,+-10%,50V	649913	60935	185-2/0.1/K/0050/R/A/B	2	
C	161		CAP,POLYPR,100PF,+-1%,100V	844803	68919	FKP2 101F 100V	1	
C	162		CAP,POLYPR,470PF,+-1%,100V	844811	68919	FKP2 471F 100V	1	
C	165,170		CAP,CER,47PF,+-2%,100V,C0G	812123	04222	SR291A470GAATR1A	2	
C	166		CAP,POLYPR,330PF,+-1%,100V	844808	68919	FKP2 331F 100V	1	
C	167		CAP,POLYPR,1000PF,+-1%,100V	844816	68919	FKP2 102F 100V	1	
C	178		CAP,TA,2.2UF,+-10%,35V	697433	56289	199D225X9035BG2	1	
CR	1	*	ZENER,COMP,6.3V,3%,10PPM,2MA	357848	04713	SZF2018	1	
CR	11	*	ZENER,UNCOMP,10.0V,10%,20.0MA,0.4W	180406	04713	1N758	1	
CR	12, 13	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	2	
CR	14- 16, 20,	*	DIODE,SI,BV= 75.0V,RADIAL INSERTED	659516	03508	1N4448	5	
CR	21	*		659516				
CR	18, 19, 22,	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	4	
CR	23	*		313247				
J	2, 6		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	56	
J	7		SOCKET,SINGLE,PWB,FOR 0.034-0.037 PIN	732826	00779	2-332070-7	1	
L	1, 3- 8,		CHOKE,6TURN	320911	89536	320911	15	
L	13, 33, 74,			320911				
L	77, 81- 84			320911				
L	51- 55, 58,		INDUCTOR,0.68UH,+-10%,221MHZ,SHLD	320937	24759	MR-O.68	7	
L	59			320937				
L	56		INDUCTOR, ADJ 33.8MH	774299	89536	774299	1	
L	57		INDUCTOR, ADJ 44.2MH	774307	89536	774307	1	
L	60- 62		INDUCTOR,100UH,+-10%,12MHZ,SHLD	249102	24759	MR-100	3	
L	70, 71		INDUCTOR,0.033UH,+-10%,1000MHZ	866632	52763	5087226-323	2	
L	72, 73, 79,		INDUCTOR,10 TURNS	463448	89536	463448	4	
L	80			463448				
L	75		INDUCTOR,390UH,+-5%,6.9MHZ,SHLD	186288	24759	MR-390	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-5. A4 Subsynthesizer PCA (cont.)

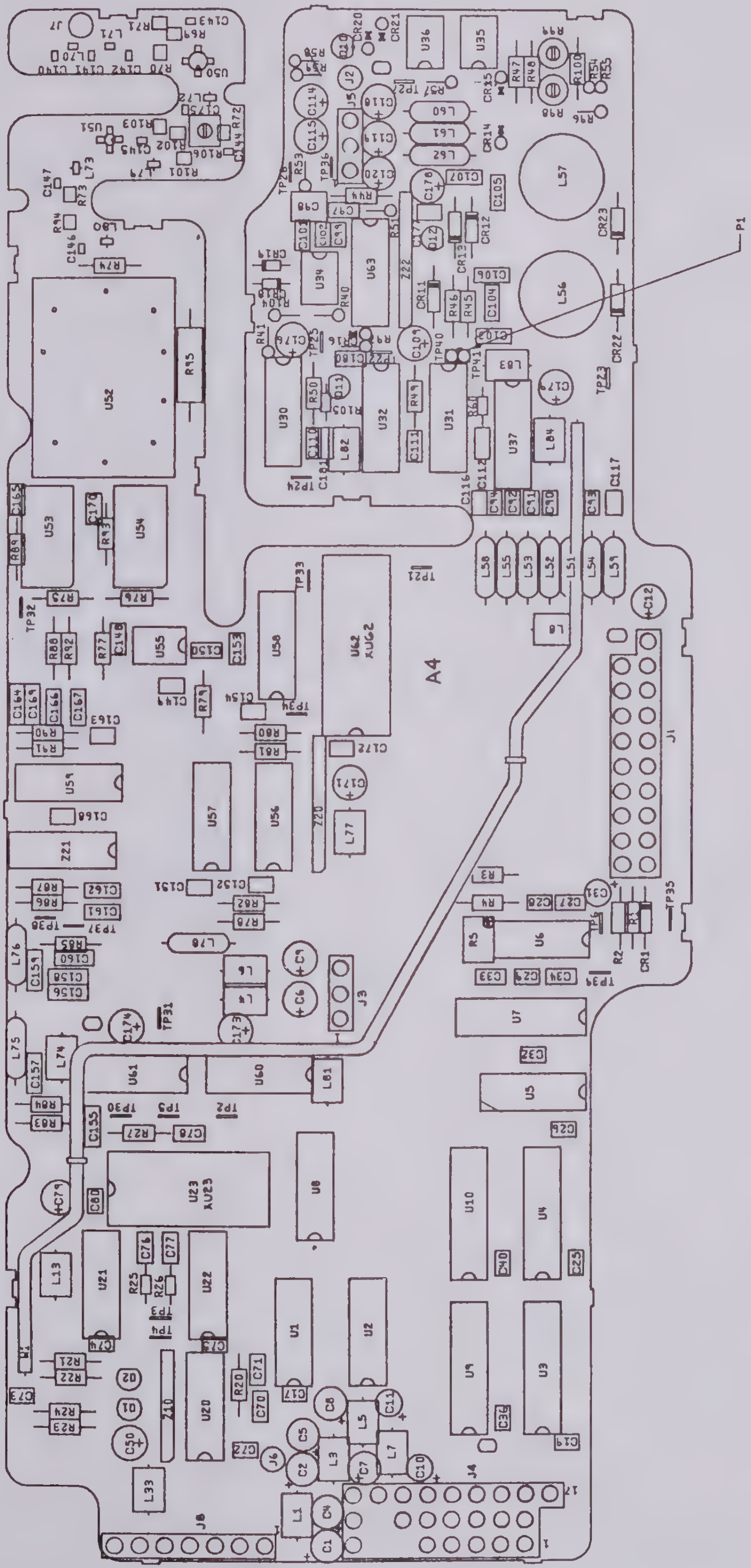
REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
L	76		INDUCTOR,270UH,+-5%,8MHZ,SHLD	186270	24759	MR-270	1	
L	78		INDUCTOR,470UH,+-5%,6.5MHZ,SHLD	147827	24759	MR-270	1	
MP	62, 63		COMPONENT HOLDER	422865	98159	2829-75-2	2	
MP	64- 72		PIN,SINGLE,PWB,0.025 SQ	277418	00779	1-87022-3	9	
P	1		JUMPER,REC,2 POS,.100CTR,.025 SQ POST	530253	00779	530153-2	1	
Q	1, 2	*	TRANSISTOR,SI,PNP,HI-SPEED SWTICH	875385	04713	2N5771RLRA	2	
Q	10	*	TRANSISTOR,SI,NMOS,1W,TO-237	875419	17856	VE0091-TR5	1	
Q	11	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	875401	04713	MPS918RLRA	1	
Q	12	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	1	
R	1		RES,MF,4.32K,+-1%,.125W,100PPM	851535	91637	CMF55 4321 F T-1	1	
R	2		RES,MF,10K,+-1%,0.125W,100PPM	719476	91637	CMF55 1002 F T-1	1	
R	3, 45, 48		RES,MF,1K,+-1%,0.125W,100PPM	719468	91637	CMF55 1001 F T-1	3	
R	4		RES,MF,1.37K,+-1%,0.125W,100PPM	866256	91637	CMF55 1371 F T-1	1	
R	5		RES,VAR,CERM,500,+-10%,0.5W	520783	80294	3299W-1-501	1	
R	20, 74, 85,		RES,CF,51,+-5%,0.125W	740050	59124	CF1-8RDST 510 J B	5	
R	89, 93			740050				
R	21		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	
R	22		RES,CF,510,+-5%,0.25W	573139	59124	CF1-4 511 J B	1	
R	23, 24, 83		RES,CF,200,+-5%,0.25W	573055	59124	CF1-4 201 J B	3	
R	25- 27, 60,		RES,CF,100,+-5%,0.125W	557223	59124	RDS21-8 101 J B	6	
R	79,105			557223				
R	40		RES,CF,36,+-5%,0.25W	643817	59124	CF1-4 360 J B	1	
R	41,104		RES,CF,270,+-5%,0.25W	810424	59124	CF1-4 VT 271 J B	2	
R	44		RES,MF,6.04K,+-1%,0.125W,100PPM	844667	91637	CMF55 6041 F T-1	1	
R	46, 47, 78		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	3	
R	49, 50		RES,CF,220,+-5%,0.25W	574244	59124	CF1-4 221 J B	2	
R	51		RES,MF,10K,+-1%,0.125W,100PPM	658914	59124	MF50DVT1002F REEL	1	
R	53, 57		RES,CF,10K,+-5%,0.25W	697102	59124	CF1-4 VT 103 J B	2	
R	54		RES,MF,4.12K,+-1%,0.125W,100PPM	820381	59124	MF50DVT4121F REEL	1	
R	55		RES,MF,19.1K,+-1%,0.125W,100PPM	234963	91637	CMF55 1912 F T-1	1	
R	58		RES,MF,49.9,+-1%,0.125W,100PPM	820266	59124	MF50DVT49R9F REEL	1	
R	59		RES,MF,47.5,+-1%,0.125W,100PPM	306076	91637	CMF55 47R5 F T-1	1	
R	69	*	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	1	
R	70, 71	*	RES,CERM,75,+-5%,.125W,200PPM,1206	811323	91637	CRCW1206-75R0JB02	2	
R	72	*	RES,CERM,180,+-5%,.125W,200PPM,1206	746321	91637	CRCW1206-1800JB02	1	
R	73, 94	*	RES,CERM,27,+-5%,.125W,200PPM,1206	807735	91637	CRCW1206-27R0JB02	2	
R	75, 76		RES,CF,15,+-5%,0.125W	740027	59124	CF1-8RDS2 150 J B	2	
R	77, 80		RES,CF,270,+-5%,0.25W	573071	59124	CF1-4 271 J B	2	
R	81		RES,CF,180,+-5%,0.25W	573048	59124	CF1-4 181 J B	1	
R	82		RES,CF,91,+-5%,0.25W	641076	59124	CF1-4 910 J B	1	
R	84		RES,CF,56,+-5%,0.25W	641068	59124	CF1-4 560 J B	1	
R	86		RES,MF,21.5K,+-1%,0.125W,100PPM	866298	91637	CMF55 2152 F T-1	1	
R	87		RES,MF,36.5K,+-1%,0.125W,100PPM	720169	91637	CMF55 3652 F T-1	1	
R	88, 92		RES,MF,100,+-1%,0.125W,100PPM	719450	91637	CMF55 1000 F T-1	2	
R	90		RES,MF,22.6K,+-1%,0.125W,100PPM	866301	91637	CMF55 2262 F T-1	1	
R	91		RES,MF,57.6K,+-1%,0.125W,100PPM	866319	91637	CMF55 5762 F T-1	1	
R	95		RES,MF,59.0,+-1%,0.5W,100PPM	150920	91637	CMF65 59R0 F T-1	1	
R	96		RES,CF,47K,+-5%,0.25W	721787	59124	CF1-4 VT 473 J B	1	
R	97		RES,CF,2K,+-5%,0.25W	810457	59124	CF1-4 VT 202 J B	1	
R	98		RES,VAR,CERM,5K,+-20%,0.5W	226084	80294	3329H-1-502	1	
R	99		RES,VAR,CERM,1K.+-30%,0.5W	193060	80294	3329H-1-102	1	
R	100		RES,MF,750,+-1%,0.125W,100PPM	720516	91637	CMF55 7500 F T-1	1	
R	101,103	*	RES,CERM,62,+-5%,.125W,200PPM,1206	854674	91637	CRCW1206-62R0JB02	2	
R	102	*	RES,CERM,220,+-5%,.125W,200PPM,1206	746347	91637	CRCW1206-2200JB02	1	
R	106		RES VAR,CERM,500,+-20%	867130	80294	3335B-1-501E	1	
TP	2- 6, 21-		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	22	
TP	27, 30- 39			816090				
TP	40, 41		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	2	
U	1, 2	*	IC,CMOS,3-8 LINE DCDR W/ENABLE	773036	01295	SN74HC138N	2	
U	3, 4, 9,	*	IC,CMOS,OCTAL D F/F W/RESET	743286	18324	N74HCT273N	4	
U	10	*		743286				
U	5	*	CMOS 7533L TESTED	802280	89536	802280	1	
U	6	*	IC,OP AMP,QUAD,LOW NOISE	851829	06665	OP470FY	1	
U	7	*	IC,CMOS,DUAL 8-BIT MULTIPLYING DAC	854448	24355	AD7628KN	1	
U	8	*	IL,CMOS,QUAD 2 INPUT AND GATE	741801	01295	SN74HC08N	1	
U	20	*	IC,ECL,TRIPLE LINE RECEIVER	369702	04713	MC10116P	1	
U	21	*	IC,FTTL,DUAL D F/F,+EDG TRG,W/CL&SET	659508	04713	MC74F74N	1	
U	22	*	IC,FTTL,QUAD 2 INPUT NAND GATE	654640	04713	MC74F00N	1	
U	23	*	IC,STTL, 360 CELL GATE ARRAY	723700	61271	MB112T302	1	
U	30, 31	*	IC,STTL,DUAL D F/F,+EDG TRG,W/SET&CLR	418269	01295	SN74S74N	2	
U	32	*	IC,STTL,QUAD 2 INPUT NAND GATE	363580	01295	SN74S00N	1	
U	34	*	IC,OP AMP,JFET INPUT,8 PIN DIP	472779	27014	LF356N	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-5. A4 Subsynthesizer PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
U 35	*	IC,OP AMP,DUAL,JFET INPUT,8 PIN DIP	495192	27014	LF353N	1	
U 36	*	ISOLATOR,OPTO,LED TO TRANSISTOR,DUAL	454330	50579	ILCT-6-254	1	
U 37, 60	*	IC,FTTL,SYNC PRESET DECADE COUNTER	854450	18324	74F160AN	2	
U 50	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	1	
U 51	*	IC,BPLR,MONOLITHIC MICROWAVE IC AMP	836593	7E751	MSA-0885	1	
U 52	*	3DB COUPLER FOR SUBSYNTH	860648	89536	860648	1	
U 53, 54		MIXER,DOUBLE BALANCED,1 - 500 MHZ	733105	1AV65	SBL-1-27	2	
U 55	*	IC,BPLR,WIDEBAND AMPLIFIER,600 MHZ	854542	18324	NE5205N	1	
U 56	*	IC,ECL,QUAD 2 INPUT NOR GATE	380881	04713	MC10102P	1	
U 57	*	IC,ECL,DUAL D M/S F/F,W/SET&RESET	454959	04713	MC10131P	1	
U 58	*	IC,ECL,TWO-MODULUS PRESCALER	722298	04713	MC12011L	1	
U 59	*	IC,OP AMP,QUAD,JFET INPUT,14 PIN DIP	483438	01295	TL084CN	1	
U 61	*	IC,CMOS,DUAL DECADE RIPPLE COUNTER	854349	18324	74HCT390N	1	
U 62	*	IC,STTL, 360 CELL GATE ARRAY	723718	61271	MB112T301	1	
U 63	*	IC,ARRAY,5 TRANS,5 ISO: 2-PNP,3-NPN	418954	34371	CA3096E	1	
W 1		CABLE ASSY, RF JUMPER	861083	89536	861083	1	
XU 23		SOCKET,IC,24 PIN	376236	00779	2-640361-1	1	
XU 62		SOCKET,IC,28 PIN	448217	91506	228-AG39D	1	
Z 10		RES,CERM,SIP,8 PIN,7 RES,560,+-2%	484451	91637	CSC08A-01-561G	1	
Z 20		RES,CERM,SIP,10 PIN,9 RES,510,+-2%	478800	91637	CSC10A-01-511G	1	
Z 21		RES,CERM,DIP,16 PIN,8 RES,10K,1%	501841	01121	316B103F	1	
Z 22		RES,CERM,SIP,10 PIN,5 RES,1K,+-2%	655209	91637	CSC10A-03-102G	1	

An * in 'S' column indicates a static-sensitive part.


J7
R71
C143
R69
L71
L70
U50
R70
C142
C141
C140
L72
C175
R72
C144
U51
R103
R102
C145
R106
R101
L79
L73
C147
R73
R94
L80
C196
R74
U52
R95
C165
U53
R89
C170
R93
U54
R75
R76
TP32
R88
R92
R77
C148
U55
C150
C153
U58
U62
XU62
TP33
TP21
A4
C164
C161
C166
C167
C163
C149
R79
C154
TP34
R90
R91
R80
R81
C172
U59
C171
U57
U56
Z20
L77
C168
Z21
C151
C152
R87
R86
C162
R82
R78
TP38
TP37
R85
C160
L78
L76
C159
C158
C156
L6
L4
C9
C6
J3
C174
TP31
C173
L75
L74
C157
U61
U60
L81
R84
R83
TP30
TP3
TP2
C135
R27
C78
U23
XU23
U8
C79
C80
L13
U21
R25
C76
R26
C77
U22
TP3
TP4
C74
C75
W1
R21
R22
Q2
C73
R24
R23
Q1
Z10
U20
R20
C71
C70
C50
C72
L33
J8
J6
C2
L3
C5
C8
L5
C11
C7
L7
C10
J4
L1
C4
C1
U1
U2
C17
U10
U4
C40
C25
U9
U3
C36
C19
U7
C32
U5
C26
C33
C29
C34
TP39
R5
U6
TP6
R2
R1
CR1
TP35
R3
R4
C28
C27
C31
J1
L8
C12
L58
L55
L53
L52
L51
L54
L59
C116
C112
C117
U30
R50
Q11
R105
C110
L82
TP24
U32
R49
C111
U31
R60
U37
L84
L83
TP23
TP41
TP40
C103
R42
R16
C180
C122
C178
R41
TP25
U34
R40
U63
Z22
CR11
R46
R45
C104
C106
CR13
CR12
L56
CR22
CR23
L57
R104
CR18
CR19
C102
C101
C99
C98
C97
R44
R51
C176
Q12
C107
C105
TP26
R53
TP36
J5
C115
C114
C118
C119
C120
L60
L61
L62
CR14
CR15
R47
R48
R98
R96
R99
R100
R54
R55
U36
U35
CR20
CR21
Q10
R58
R59
J2
TP22
R57
P1

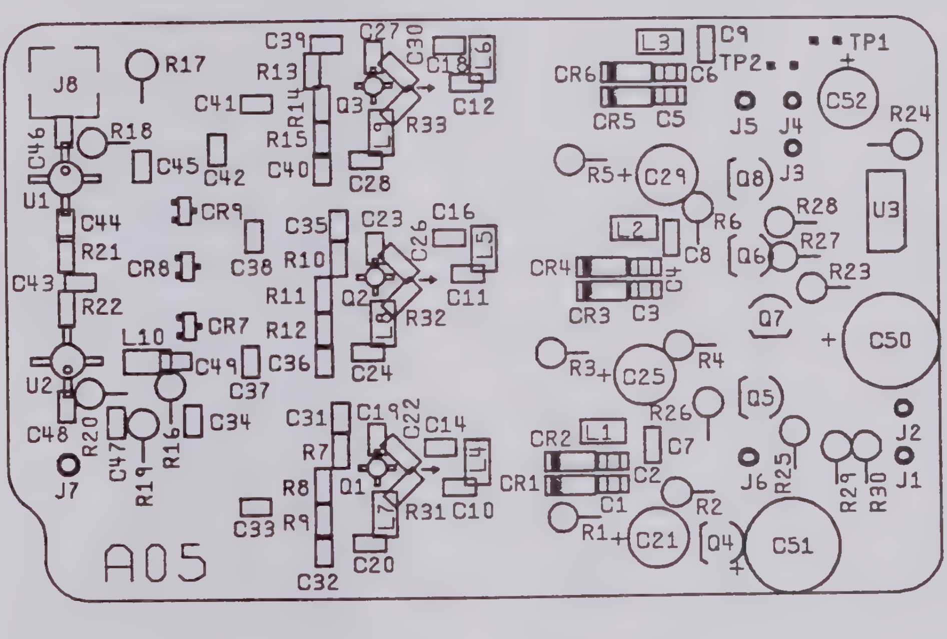
6082A-1662

Figure 8-5. A4 Subsynthesizer PCA

Table 8-6. A5 Coarse Loop VCO PCA
(See Figure 8-6.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
C	1- 4		CAP,PORC,1.8PF,+-0.1PF,50V,0505	800854	51406	MA181R8B	4	
C	5, 6		CAP,PORC,2.7PF,+-0.1PF,50V,0505	800862	51406	MA182R7B	2	
C	7- 9		CAP,CER,22PF,+-10%,50V,C0G,1206	740563	04222	12065A220KAT060B	3	
C	10- 12, 14,		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	24	
C	16, 18- 20,			514133				
C	23, 24, 28,			514133				
C	31, 32, 35,			514133				
C	36, 39, 40,			514133				
C	43- 49			514133				
C	21, 25, 29		CAP,TA,2.2UF,+-20%,25V	697425	56289	199D225X0025AG2	3	
C	22, 37, 41		CAP,CER,4.7PF,+-0.25PF,50V,C0G,0805	806760	04222	08055A4R7CAT1.3B	3	
C	26		CAP,CER,5.6PF,+-0.25PF,50V,C0G,0805	806778	04222	08055A5R6CAT1.3B	1	
C	27		CAP,CER,330PF,+-20%,50V,X7R,0805	650093	04222	08055C331MAT060B	1	
C	30		CAP,CER,8.2PF,+-0.5PF,50V,C0G,0805	713982	95275	VJ0805Q8R2DXAT	1	
C	33, 38, 42		CAP,CER,3.6PF,+-0.25PF,50V,C0G,0805	845169	04222	08055A3R6CAT051B	3	
C	34		CAP,CER,2.7PF,+-0.25PF,50V,C0G,0805	806752	04222	08055A2R7CAT1.3B	1	
C	50, 51		CAP,AL,470UF,+-20%,16V,SOLV PROOF	875497	62643	KME16VB471M10X12FT	2	
C	52		CAP,AL,10UF,+-20%,63V,SOLV PROOF	816843	62643	KME63VB10RM5X11RP	1	
CR	1- 6		DIODE,SI,VARACTOR,PIV=30V,18PF,MLF	866587	25403	BB215	6	
CR	7- 9	*	DIODE,SI,50V,PIN,RF SWITCHING,SOT23	854588	25088	BA885	3	
J	1- 6		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	6	
J	7		SOCKET,SINGLE,PWB,FOR 0.034-0.037 PIN	732826	00779	2-332070-7	1	
J	8		CONN,COAX,SMA(M),PWB OR PANEL	512087	21845	2985-6011	1	
L	1- 10		INDUCTOR,0.18UH,+-10%,770MHZ	800920	52763	S-5087227-213	10	
MP	1- 4		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	4	
Q	1, 2	*	TRANSISTOR,SI,NPN,SM SIGNAL,HI FT	535153	33297	NE21935	2	
Q	3	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	483156	33297	NE02135	1	
Q	4- 8	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	5	
R	1, 3, 5		RES,CF,470,+-5%,0.25W	854567	59124	CF1-4 VT 471 J B	3	
R	2, 4, 6,		RES,CF,200,+-5%,0.25W	810390	59124	CF1-4 VT 201 J B	4	
R	16			810390				
R	7, 9, 10,	*	RES,CERM,120,+-5%,.125W,200PPM,1206	746305	91637	CRCW1206-1200JB02	6	
R	12, 13, 15	*		746305				
R	8, 11, 14,	*	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	91637	CRCW1206-47R0JB02	5	
R	21, 22	*		746263				
R	17, 19		RES,CF,100,+-5%,0.25W	810465	59124	CF1-4 VT 101 J B	2	
R	18, 20		RES,CF,160,+-5%,0.25W	854724	59124	CF1-4 VT 161 J B	2	
R	23, 25- 28		RES,MF,10K,+-1%,0.125W,100PPM	658914	59124	MF50DVT1002F REEL	5	
R	24		RES,CF,680,+-5%,0.25W	854570	59124	CF1-4 VT 681 J B	1	
R	29, 30		RES,CF,15,+-5%,0.25W	854562	59124	CF1-4 VT 150 J B	2	
R	31- 33	*	RES,CERM,150,+-5%,.125W,200PPM,1206	746313	91637	CRCW1206-1500JB02	3	
U	1, 2	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	2	
U	3	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LM339DT	1	

An * in 'S' column indicates a static-sensitive part.


J8
R17
C39
R13
C27
C30
C18
L6
L3
C9
TP1
TP2
CR6
C6
C52
C41
R14
Q3
C12
R33
L9
R15
C40
C28
CR5
C5
J5
J4
R24
C46
R18
C45
C42
U1
R5
C29
Q8
J3
U3
C44
CR9
C35
C23
C16
C26
L5
L2
R6
R28
R21
CR8
C38
R10
C11
CR4
C8
Q6
R27
C43
R22
R11
Q2
R32
L8
C4
R23
CR7
R12
CR3
C3
Q7
L10
C49
C36
C24
R3
C25
R4
C50
U2
C37
R26
Q5
C48
R20
C47
R19
R16
C34
C31
C19
C22
C14
CR2
L1
C7
J2
R7
L4
J6
R25
J7
R8
Q1
CR1
C2
R29
R30
J1
C33
R9
R31
C10
L7
C1
R2
R1
C21
Q4
C51
A05
C20
C32

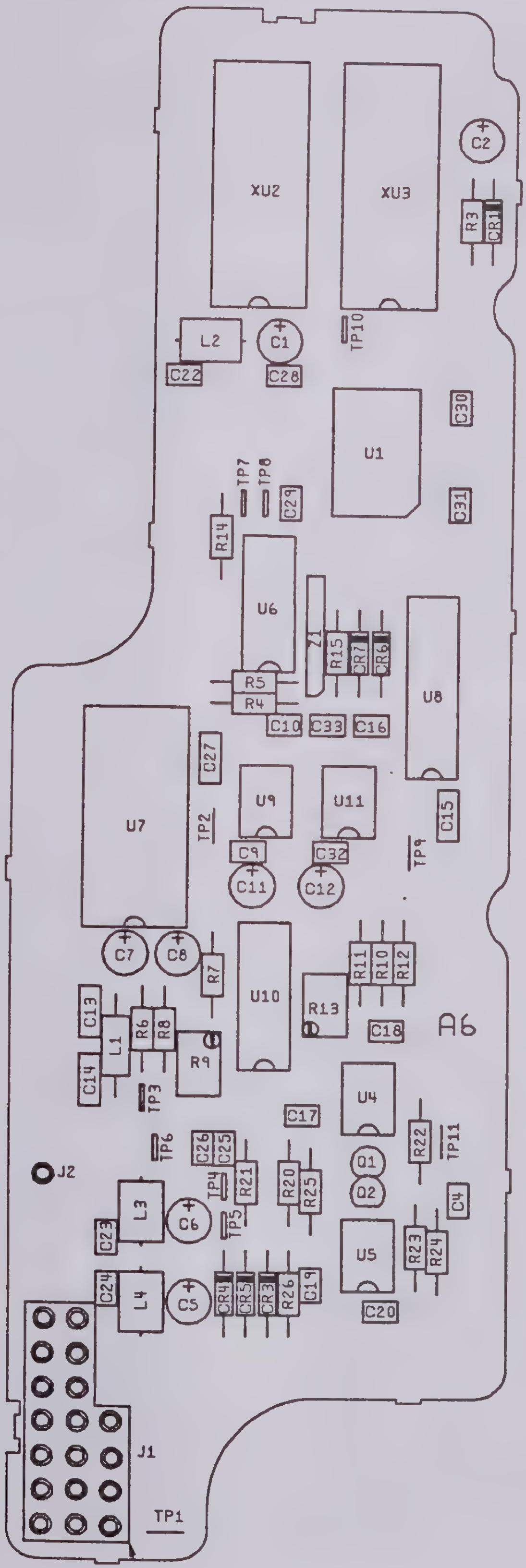
6082A-1663

Figure 8-6. A5 Coarse Loop VCO PCA

Table 8-7. A6 Mod Oscillator PCA
(See Figure 8-7.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1		CAP,TA,22UF,+-20%,10V	658971	56289	199D226X0010CG2	1	
C	2, 5- 8,		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	7	
C	11, 12			714774				
C	4, 9, 10,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	17	
C	16- 20, 22-			837526				
C	24, 28- 33			837526				
C	13, 14		CAP,CER,680PF,+-5%,50V,C0G	743351	04222	SR595A681JAATR1A	2	
C	15		CAP,CER,15PF,+-2%,100V,C0G	832287	04222	SR591A150GAATR1A	1	
C	25, 26		CAP,CER,150PF,+-2%,100V,C0G	512988	04222	SR151A151JAT	2	
C	27		CAP,CER,10PF,+-2%,50V,C0G	713875	04222	SR595A100GAATR1A	1	
CR	1, 3- 7	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	6	
L	1		INDUCTOR,1000UH,+-5%,4.5MHZ,SHLD	147819	24759	MR-1000	1	
L	2- 4		CHOKE,6TURN	320911	89536	320911	3	
MP	1- 19		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	19	
Q	1, 2	*	TRANSISTOR,SI,N-JFET,TO-92	723734	17856	J27138TR	2	
R	3, 14, 15		RES,CF,33K,+-5%,0.25W	573485	59124	CF1-4 333 J B	3	
R	4, 5		RES,MF,49.9,+-1%,0.125W,100PPM	720318	91637	CMF55 49R9 F T-1	2	
R	6, 7, 23,		RES,MF,1K,+-0.1%,0.125W,50PPM	706051	91637	CMF55 1001 B T-2	4	
R	25			706051				
R	8		RES,MF,374,+-1%,0.125W,100PPM	866335	91637	CMF55 3740 F T-1	1	
R	9		RES,VAR,CERM,100,+-10%,0.5W	381913	80294	3299W-1-101	1	
R	10		RES,MF,604,+-1%,0.125W,100PPM	832030	91637	CMF55 6040 F T-1	1	
R	11		RES,MF,8.87K,+-1%,.125W,100PPM	851472	91637	CMF55 8871 F T-1	1	
R	12		RES,MF,3.48K,+-1%,0.125W,100PPM	832071	91637	CMF55 3481 F T-1	1	
R	13		RES,VAR,CERM,500,+-10%,0.5W	520783	80294	3299W-1-501	1	
R	20, 26		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4 103 J B	2	
R	21		RES,CF,51,+-5%,0.25W	572990	59124	CF1-4 510 J B	1	
R	22		RES,MF,2.05K,+-1%,0.125W,100PPM	719849	91637	CMF55 2051 F T-1	1	
R	24		RES,MF,5.11K,+-1%,0.125W,100PPM	720342	91637	CMF55 5111 F T-1	1	
TP	1, 2, 9,		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	4	
TP	11			816090				
TP	3- 8, 10		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	7	
U	1	*	IC,CMOS,CUSTOM GATE ARRAY,80PN QFP	851324	33297	851324	1	
U	2		PROM, MOD OSC, MS	861112	89536	861112	1	
U	3		PROM, MOD OSC, LS	861117	89536	861117	1	
U	4, 5	*	IC,OP AMP,HIGH SPEED,200V/US,35MHZ	845466	27014	LM6361N	2	
U	6	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	1	
U	7	*	IC,CMOS,12 BIT,1/4 LSB,ON BOARD REF	851642	24355	AD565AJD	1	
U	8	*	IC,CMOS,12 BIT,1/2 BIT,UP COMPATIBLE	851647	24355	AD7548KN	1	
U	9, 11	*	IC,OP AMP,DUAL,LO OFFST VOLT,LO-DRIFT	851704	27014	LF412ACN	2	
U	10	*	IC,CMOS,QUAD SPST ANALOG SWITCH	680744	17856	DG308ACJ	1	
XU	2, 3		SOCKET,IC,28 PIN	448217	91506	228-AG39D	2	
Z	1		RES,CERM,SIP,6 PIN,5 RES,22K,+-2%	520122	91637	CSC06A-01-223G	1	

An * in 'S' column indicates a static-sensitive part.


XU2
XU3
C2
R3
CR1
L2
C1
TP10
C22
C28
C30
U1
TP7
TP8
C29
C31
R14
U6
Z1
R15
CR7
CR6
U8
R5
R4
C10
C33
C16
U7
C27
U9
U11
TP2
C15
C9
C32
TP9
C11
C12
C7
C8
R7
U10
R11
R10
R12
C13
R13
A6
R6
R8
C18
L1
R9
C14
TP3
C17
U4
TP6
C26
C25
R22
TP11
J2
R21
Q1
TP4
R20
R25
Q2
L3
C6
C4
TP5
C23
U5
R23
R24
C24
L4
C5
CR4
CR5
CR3
R26
C19
C20
J1
TP1

6082A-1667

Figure 8-7. A6 Mod Oscillator PCA

Table 8-8. A8 Output PCA
(See Figure 8-8.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	2,176		CAP,CER,2700PF,+-20%,100V,X7R	362889	04222	SR151C272MAA	2	
C	4, 7, 11,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	28	
C	41, 46- 49,			837526				
C	58, 63, 64,			837526				
C	71, 76- 78,			837526				
C	85- 87, 92,			837526				
C	108,112,113,			837526				
C	118,123,125,			837526				
C	127-129			837526				
C	5, 6, 12,		CAP,CER,4700PF,+-20%,100V,X7R	866426	04222	SR151C472MAATR2A	15	
C	14- 17, 43,			866426				
C	51, 53,178,			866426				
C	180,198,199,			866426				
C	206			866426				
C	18, 22		CAP,CER,180PF,+5%,100V,C0G	837625	04222	SR151A181JATR2A	2	
C	19, 21,101,		CAP,CER,270PF,+-5%,100V,C0G	876151	04222	SR151A271JAATR2A	4	
C	102			876151				
C	20		CAP,CER,330PF,+-5%,100V,C0G	838474	04222	SR071A331JAATR1A	1	
C	23, 27, 29,		CAP,CER,120PF,+-2%,100V,C0G	543819	04222	SR151A121JAT	7	
C	31, 65,100,			543819				
C	106			543819				
C	24- 26		CAP,CER,200PF,+-5%,50V,C0G	851266	04222	SR595A201JAATR1A	3	
C	28, 32		CAP,CER,82PF,+-2%,100V,C0G	512350	04222	SR291A820GAATR1A	2	
C	30, 50,205		CAP,CER,150PF,+-2%,100V,C0G	512988	04222	SR151A151JAT	3	
C	33, 37, 91		CAP,CER,56PF,+-2%,100V,C0G	876136	04222	SR151A560GAATR2A	3	
C	34- 36,104		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	4	
C	38, 40, 57,		CAP,CER,1000PF,+-10%,50V,C0G,1206	747378	04222	12065A102KAT060B	9	
C	60- 62,191,			747378				
C	193,202			747378				
C	39,184,217		CAP,CER,3.3PF,+-0.5PF,50V,C0G,0805	514208	51406	GRH708C0G3R3D200VPT	3	
C	44, 55,107		CAP,CER,47PF,+-2%,100V,C0G	512368	04222	SR151A470GAA	3	
C	45,177,211-		CAP,CER,150PF,+-5%,50V,C0G,0805	866533	04222	08055A151JAT050R	5	
C	213			866533				
C	52		CAP,CER,1.2PF,+-0.25PF,100V,C0K	543256	51406	RPE110C0K1R2C1	1	
C	54, 56,207-		CAP,CER,22PF,+-2%,100V,C0G	866421	04222	SR151A220GAATR1A	5	
C	209			866421				
C	66		CAP,CER,27PF,+-2%,100V,C0G	812107	04222	SR291A270GAATR1A	1	
C	67		CAP,CER,180PF,+-5%,100V,C0G	603506	04222	SR151A181JAT	1	
C	68, 69,172,		CAP,CER,12PF,+-5%,50V,C0G,0805	514232	51406	GRM708C0G120J200VPB	6	
C	173,179,214			514232				
C	73, 82,132,		CAP,TA,2.2UF,+-20%,20V	854760	56289	195D225X0020D2B	5	
C	134,135			854760				
C	74, 75, 84,		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	4	
C	88			837542				
C	79		CAP,TA,0.47UF,+-20%,35V	161349	56289	199D474X0035AA2	1	
C	80		CAP,CER,1.5PF,+-0.25PF,100V,C0K	529909	51406	RPE110C0K1R5C1	1	
C	83		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12065C103KAT060R	1	
C	89, 90		CAP,TA,39UF,+-20%,6V	163915	56289	199D396X0006DA2	2	
C	93		CAP,CER,10PF,+-2%,100V,C0G	875450	04222	SR151A100GAATR2A	1	
C	94		CAP,CER,15PF,+-2%,100V,C0G	876169	04222	SR151A150GAATR2A	1	
C	95, 97, 98		CAP,CER,6.8PF,+-0.25PF,100V,C0H	866553	04222	SR151A6R8CAA	3	
C	96		CAP,CER,33PF,+-2%,50V,C0G	715292	04222	SR595A330GAATR1A	1	
C	99		CAP,CER,68PF,+-2%,100V,C0G	362756	04222	SR291A680GAATR1A	1	
C	103		CAP,CER,220PF,+-2%,100V,C0G	812131	04222	SR291A221GAATR1A	1	
C	105		CAP,CER,18PF,+-2%,100V,C0G	512335	51406	RPE110A184G1	1	
C	109-111,114,		CAP,TA,2.2UF,+-20%,20V	161927	56289	199D225X0020BA2	5	
C	140			161927				
C	116,126,130		CAP,CER,470PF,+-20%,100V,X7R	358275	04222	SR151C471MAA	3	
C	117,189		CAP,CER,1.8PF,+-0.25PF,50V,C0G,0805	806745	04222	08055A1R8CAT1.3B	2	
C	120		CAP,CER,8.2PF,+-0.25PF,100V,C0H	715359	51406	RPE110-C0H8R2C1	1	
C	121		CAP,CER,22PF,+-5%,50V,C0G	448449	04222	SR211A220JAA	1	
C	122		CAP,CER,12PF,+-2%,100V,C0G	376871	59660	8101-100-C0G-126G	1	
C	124		CAP,CER,5.6PF,+-0.25PF,63V,U2J	853403	19701	R569C13U2JHWHAP	1	
C	168		CAP,CER,39PF,+-2%,100V,C0G	816207	04222	SR291A390GAATR1A	1	
C	170,171,174,		CAP,CER,1000PF,+-10%,50V,X7R,0805	484378	04222	08055C102KAT060B	4	
C	210			484378				
C	188,218		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	2	
C	194		CAP,AL,100UF,+-20%,16V,SOLV PROOF	816850	62643	KME16VB101M6.3X11RP	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-8. A8 Output PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE
C 196		CAP,PORC,0.4PF,+-0.1PF,50V	807206	51406	MA180R4BPT	1	
C 200		CAP,CER,4.7PF,+-0.25PF,100V,COH	362772	72982	RPE110C0H4R7C1	1	
C 201		CAP,VAR,0.5-1.3PF,250V,CER	783548	91293	9401-1	1	
C 204		CAP,CER,680PF,+-5%,50V,C0G	743351	04222	SR595A681JAATR1A	1	
C 215		CAP,CER,22PF,+-5%,50V,C0G,0805	855101	95275	VJ0805Q220JXAT	1	
C 216		CAP,CER,1.0PF,+-0.5PF,50V,C0G,0805	512129	95275	VJ0805Q1R0DXAT	1	
C 219		CAP,VAR,9-90PF,50V,CER	643130	51406	TZ03R900FR174	1	
CR 4, 5, 16-	*	DIODE,SI,PIN, RF ATTENUATING	508077	33025	MA 4P523	6	
CR 18, 24	*		508077				
CR 6- 13	*	DIODE,SI,50V,PIN,RF SWITCHING,SOT23	854588	25088	BA885	8	
CR 14, 15	*	DIODE,SI,PIN,EPOXY STRIPLINE	773176	59365	MPN-7484-E26	2	
CR 19, 20	*	DIODE,SI,SCHOTTKY,MATCHED SET OF 2	722470	28480	QSCH3842	1	
CR 21- 23, 41	*	DIODE,SI,PIN,SELECTED CT & RS 7402-CT	773192	59365	MX2636	4	
CR 26, 36- 40	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	6	
CR 27- 33	*	DIODE,SI,PIN,MATCHED SET OF 7	879192	59365	MX2070-SELECTED	1	
CR 35	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	1	
FL 1, 21, 22		FILTER,RF,PIN-SLEEVE STYLE,175PF	807289	00779	859653-1	3	
FL 2- 4, 8,		FILTER,RF,PIN-SLEEVE STYLE,2000PF	807271	00779	859612-1	13	
FL 13- 19, 23,			807271				
FL 25			807271				
H 1, 3- 6		SCREW,PH,P,SS,LOCK,4-40,.250	256156	COMMERCIAL		5	
H 2		NUT,HEX,STL,8-32	281113	COMMERCIAL		1	
J 1, 2, 4		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	3	
J 3		CONN,COAX,SMB(M),PWB OR PANEL	512095	98291	051-051-0429-220	1	
L 3, 6- 8,		INDUCTOR,5.6UH,+-20%,130MHZ	844881	52763	5087230-723	20	
L 13, 16, 34,			844881				
L 35, 38- 40,			844881				
L 50, 69, 79-			844881				
L 84, 93			844881				
L 4, 15, 33,		CHOKE,6TURN	320911	89536	320911	12	
L 41, 47, 51,			320911				
L 56, 68, 72,			320911				
L 74, 76, 77			320911				
L 17, 20		INDUCTOR,0.47UH,+-5%,330MHZ	855002	91637	IM2-31-.47UH5%	2	
L 18, 19		INDUCTOR,0.56UH,+-5%,300MHZ	855007	91637	IM2-31-.56UH5%	2	
L 21, 24		INDUCTOR,0.33UH,+-5%,410MHZ	854992	91637	IM2-31-.33UH5%	2	
L 22, 23		INDUCTOR,0.39UH,+-5%,365MHZ	854997	91637	IM2-31-.39H5%	2	
L 25, 28		INDUCTOR,0.22UH,+-5%,510MHZ	854976	91637	IM2-31-.22UH5%	2	
L 26, 27		INDUCTOR,0.27UH,+-5%,430MHZ	854989	91637	IM2-31-.27UH5%	2	
L 29, 32		INDUCTOR,0.15UH,+-5%,600MHZ	854971	91637	IM2-31-.15UH5%	2	
L 30, 31		INDUCTOR,0.18UH,+-5%,550MHZ	854984	91637	IM2-31-.18UH5%	2	
L 36, 37, 58		INDUCTOR,0.10UH,+-10%,400MHZ,SHLD	257154	24759	MR-0.10	3	
L 42, 59		INDUCTOR,0.27UH,+-10%,400MHZ,SHLD	313031	24759	MR-0.27	2	
L 43		INDUCTOR,0.33UH,+-10%,300MHZ,SHLD	261743	24759	MR-0.33	1	
L 44, 62		INDUCTOR,0.39UH,+-5%,290MHZ,SHLD	329656	24759	MR-0.39	2	
L 45, 49, 52,		INDUCTOR,10 TURNS	463448	89536	463448	4	
L 73			463448				
L 46		INDUCTOR,1500UH,+-10%,2.5MHZ,SHLD	343863	24759	MR-1500	1	
L 48, 66, 67		INDUCTOR,6800UH,+-10%,1.5MHZ,SHLD	363184	24759	MR-6800	3	
L 53, 55		INDUCTOR,0.044UH,+-15%,500MHZ,SHLD	249110	72259	249110	2	
L 54		INDUCTOR,0.082UH,+-10%,500MHZ,SHLD	256289	91637	IMS-5.082UH10%	1	
L 57, 64		INDUCTOR,0.47UH,+-5%,264MHZ,SHLD	329664	24759	MR-0.47	2	
L 63		INDUCTOR,0.68UH,+-10%,221MHZ,SHLD	320937	24759	MR-O.68	1	
L 65		INDUCTOR,0.56UH,+-5%,249MHZ,SHLD	806570	24759	MR-.56	1	
L 75		INDUCTOR, 6.8MH	860796	89536	860796	1	
L 95		INDUCTOR,0.10UH,+-5%,1000MHZ	844923	52763	5087226-913	1	
MP 1		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
MP 2		OUTPUT AMP BASE PLATE, PLATED	860945	89536	860945	1	
MP 4- 27		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	24	
P 1		PIN FEED THRU	812735	20584	812735	1	
Q 1, 7, 9,	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	722256	04713	MRF581	4	
Q 10	*		722256				
Q 2, 4, 6,	*	TRANSISTOR,SI,PNP,T092	698233	04713	2N3906RLRA	7	
Q 8, 11, 12,	*		698233				
Q 17	*		698233				
Q 3	*	TRANSISTOR,SI,PNP,T092	698290	04713	MPS6562RLRA	1	
Q 5, 13	*	TRANSISTOR,NPN,SI,RF,LOW NOISE	845052	7E751	AT-41485	2	
Q 14	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	723379	89536	BFR96S	1	
Q 16	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	845024	04713	MRF587	1	
Q 18- 21	*	TRANSISTOR,SI,PNP,HI-SPEED SWTICH	875385	04713	2N5771RLRA	4	
R 1		RES,VAR,CERM,50,+-10%,0.5W	447862	80294	3386R-1-500	1	
R 2, 50		RES,MF,43.2,+-1%,0.125W,100PPM	855267	91637	CMF55 43R2 F T-1	2	

An * in 'S' column indicates a static-sensitive part.

Table 8-8. A8 Output PCA (cont.)

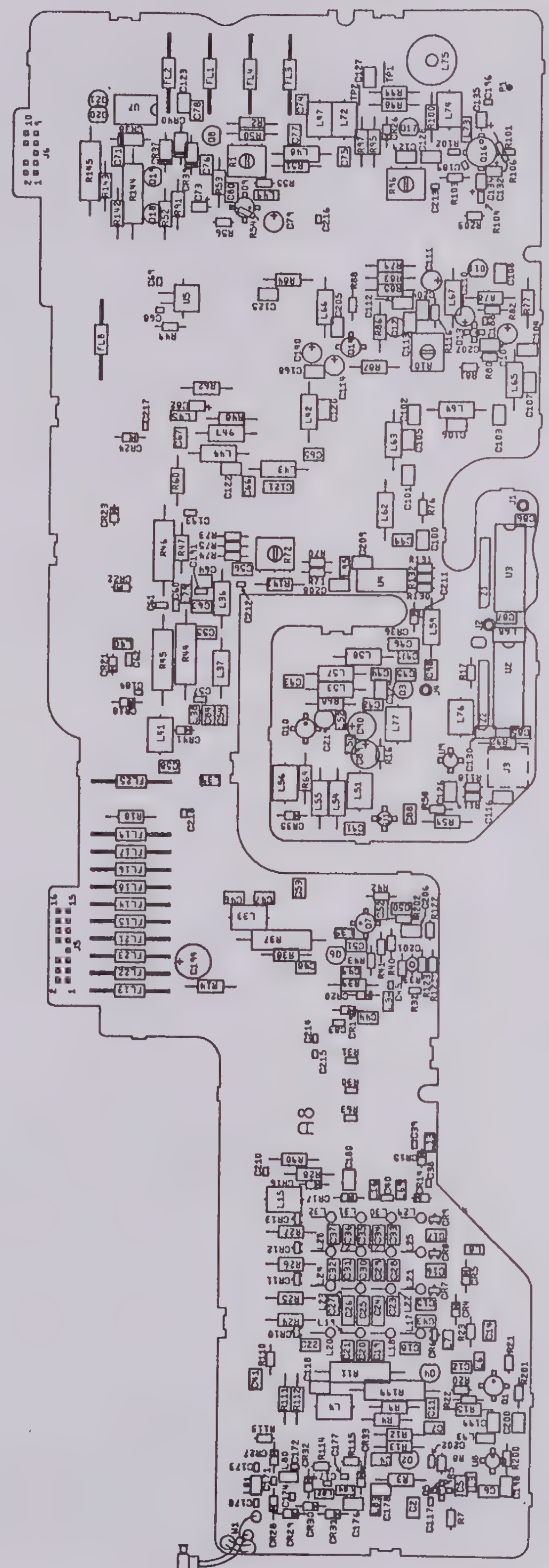
REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
R	3, 15, 28,		RES,CF,2K,+-5%,0.25W	573238	59124	CF1-4 202 J B	6	
R	53, 77, 86			573238				
R	4		RES,CC,300,+-5%,0.25W	348276	01121	CB3015	1	
R	5,106,119		RES,MF,182,+-1%,0.25W,100PPM	799726	91637	CCF-501820F	3	
R	7, 8,116,		RES,MF,30.1,+-1%,0.25W,100PPM	799692	91637	CCF-5030R1F	4	
R	201			799692				
R	9		RES,MF,5.76K,+-1%,0.125W,100PPM	720409	91637	CMF55 5761 F T-1	1	
R	10		RES,VAR,CERM,500,+-10%,0.5W	325613	80294	3386R-1-501	1	
R	11, 37		RES,MF,63.4,+-1%,0.5W,100PPM	155101	91637	CMF65 63R4 F T-1	2	
R	12		RES,MF,2.67K,+-1%,.125W,100PPM	851519	91637	CMF55 2671 F T-1	1	
R	13		RES,MF,6.65K,+-1%,0.125W,100PPM	720474	91637	CMF55 6651 F T-1	1	
R	14		RES,CF,15,+-5%,0.25W	641043	59124	CF1-4 150 J B	1	
R	16, 17,202		RES,CF,11,+-5%,0.125W	740019	59124	CF1-8RDS2 110 J B	3	
R	18, 47, 60,		RES,MF,301,+-1%,0.125W,100PPM	720029	91637	CMF55 3010 F T-1	5	
R	78, 79			720029				
R	20, 21, 42,		RES,CF,24,+-5%,0.125W	740043	59124	CF1-8RDS2 240 J B	6	
R	43, 55, 56			740043				
R	22, 41		RES,CF,120,+-5%,0.125W	740084	59124	CF1-8RDS2 121 J B	2	
R	23, 40,103		RES,CF,2K,+-5%,0.125W	854695	59124	RDS21-8202J	3	
R	24- 27,100,		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	6	
R	111			573170				
R	30, 32	*	RES,CERM,270,+-5%,.125W,200PPM,1206	746354	91637	CRCW1206-2700JB02	2	
R	31	*	RES,CERM,360,+-5%,.125W,200PPM,1206	783290	91637	CRCW1206-3600JB02	1	
R	33		RES,CF,75,+-5%,0.125W	740068	59124	CF1-8RDS2 750 J B	1	
R	38		RES,MF,1.4K,+-1%,.125W,100PPM	851563	91637	CMF55 1401 F T-1	1	
R	39, 52		RES,MF,2.55K,+-1%,0.125W,100PPM	719955	91637	CMF55 2551 F T-1	2	
R	44		RES,MF,1.21K,+-1%,0.5W,100PPM	241596	91637	CMF65 1211 F T-1	1	
R	45, 46		RES,MF,267,+-1%,0.5W,100PPM	233163	91637	CMF65 2670 F T-1	2	
R	48, 51		RES,MF,1K,+-1%,0.125W,100PPM	719468	91637	CMF55 1001 F T-1	2	
R	49, 73, 76		RES,CF,51,+-5%,0.125W	740050	59124	CF1-8RDST 510 J B	3	
R	54, 75,121,		RES,CF,160,+-5%,0.125W	740092	59124	CF1-8RDS2 161 J B	4	
R	122			740092				
R	58, 71, 74,		RES,CF,18,+-5%,0.125W	740035	59124	CF1-8RDS2 180 J B	4	
R	132			740035				
R	59		RES,MF,267,+-1%,0.125W,100PPM	866223	91637	CMF55 2670 F T-1	1	
R	62		RES,CF,0.51,+-5%,0.25W	631986	59124	CF1-4 0R51 J B	1	
R	63	*	RES,CERM,110,+-5%,.125W,200PPM,1206	747725	91637	CRCW1206-1100JB02	1	
R	68		RES,CF,51,+-5%,0.25W	572990	59124	CF1-4 510 J B	1	
R	69		RES,CF,270,+-5%,0.25W	573071	59124	CF1-4 271 J B	1	
R	70		RES,CF,270,+-5%,0.125W	557231	59124	RDS21-8 271 J B	1	
R	72		RES,VAR,CERM,200,+-10%,0.5W	275743	80294	3386R-1-201	1	
R	80- 82		RES,CF,15,+-5%,0.125W	740027	59124	CF1-8RDS2 150 J B	3	
R	83		RES,MF,8.87K,+-1%,.125W,100PPM	851472	91637	CMF55 8871 F T-1	1	
R	84		RES,MF,115,+-1%,0.125W,100PPM	866186	91637	CMF55 1150 F T-1	1	
R	85		RES,MF,11K,+-1%,0.125W,50PPM	714873	91637	CMF55 1102 B T-2	1	
R	87		RES,MF,100,+-1%,0.125W,100PPM	719450	91637	CMF55 1000 F T-1	1	
R	88		RES,MF,18.2,+-1%,0.25W,100PPM	799817	91637	CCF-5018R2F	1	
R	90		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	1	
R	91		RES,MF,475,+-1%,0.125W,100PPM	866231	91637	CMF55 4750 F T-1	1	
R	92		RES,CC,510,+-5%,0.25W	218032	01121	CB5145	1	
R	95		RES,MF,604,+-1%,0.125W,100PPM	832030	91637	CMF55 6040 F T-1	1	
R	96		RES,VAR,CERM,100,+-10%,0.5W	275735	80294	3386R-1-101	1	
R	97		RES,MF,6.49K,+-1%,0.125W,100PPM	720466	91637	CMF55 6491 F T-1	1	
R	98, 99		RES,MF,30.1,+-1%,0.125W,100PPM	855242	91637	CMF55 30R1 F T-1	2	
R	101,102	*	RES,CERM,27,+-5%,.125W,200PPM,1206	807735	91637	CRCW1206-27R0JB02	2	
R	104	*	RES,CERM,10,+-5%,.125W,200PPM,1206	746214	91637	CRCW1206-10R0JB02	1	
R	110		RES,MF,1K,+-1%,0.25W,100PPM	799791	91637	CCF-501001F	1	
R	112		RES,CF,470,+-5%,0.25W	573121	59124	CF1-4 471 J B	1	
R	113,115		RES,CF,39,+-5%,0.125W	844969	59124	RDS21-8390J	2	
R	114		RES,CF,22,+-5%,0.125W	557215	59124	RDS21-8 22R0 J B	1	
R	118		RES,MF,39.2,+-1%,0.25W,100PPM	799775	91637	CCF-5039R2	1	
R	123		RES,CF,33,+-5%,0.125W	830885	59124	CF1-4 330 J B	1	
R	130,131		RES,CF,300,+-5%,0.125W	844972	59124	RDS21-8301J	2	
R	141		RES,CF,1.8K,+-5%,0.25W	573220	59124	CF1-4 182 J B	1	
R	142,143		RES,CF,20,+-5%,0.25W	572958	59124	CF1-4 200 J B	2	
R	144,145		RES,MF,121,+-1%,0.5W,100PPM	801019	91637	CMF65 1210 F T-1	2	
R	199		RES,MF,187,+-1%,0.5W,100PPM	845032	91637	CMF65 1870 F T-1	1	
R	200		RES,CF,360,+-5%,0.125W	772277	59124	RDS21-8 361 J B	1	
R	203		RES JUMPER,0.01,0.125W	867069	91637	FRJ-50	1	
TP	1, 2		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	2	
U	1, 9	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	2	
U	2	*	IC,ECL,TRIPLE LINE RECEIVER	369702	04713	MC10116P	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-8. A8 Output PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
U	3	*	IC,ECL,DUAL D M/S F/F,W/SET&RESET	454959	04713	MC10131P	1	
U	4		MIXER,DOUBLE BALANCED,2-500MHZ	851282	1AV65	TFM-1H	1	
U	5	*	IC,GAAS,TRANSFER SWITCH	854831	33025	MA4GM502M-2000	1	
U	7	*	IC,STTL,DUAL DIFFERENTIAL LINE DRIVER	801308	07263	UA9638TC	1	
U	8	*	IC,BPLR,SELECT GAIN MSA 0404 @ 2GHZ	773226	7E751	SMA85-2025	1	
W	1		CABLE ASSY RF	808568	89536	808568	1	
Z	1, 2		RES,CERM,SIP,6 PIN,5 RES,510,+-2%	459974	91637	CSC06A-01-511G	2	

An * in 'S' column indicates a static-sensitive part.



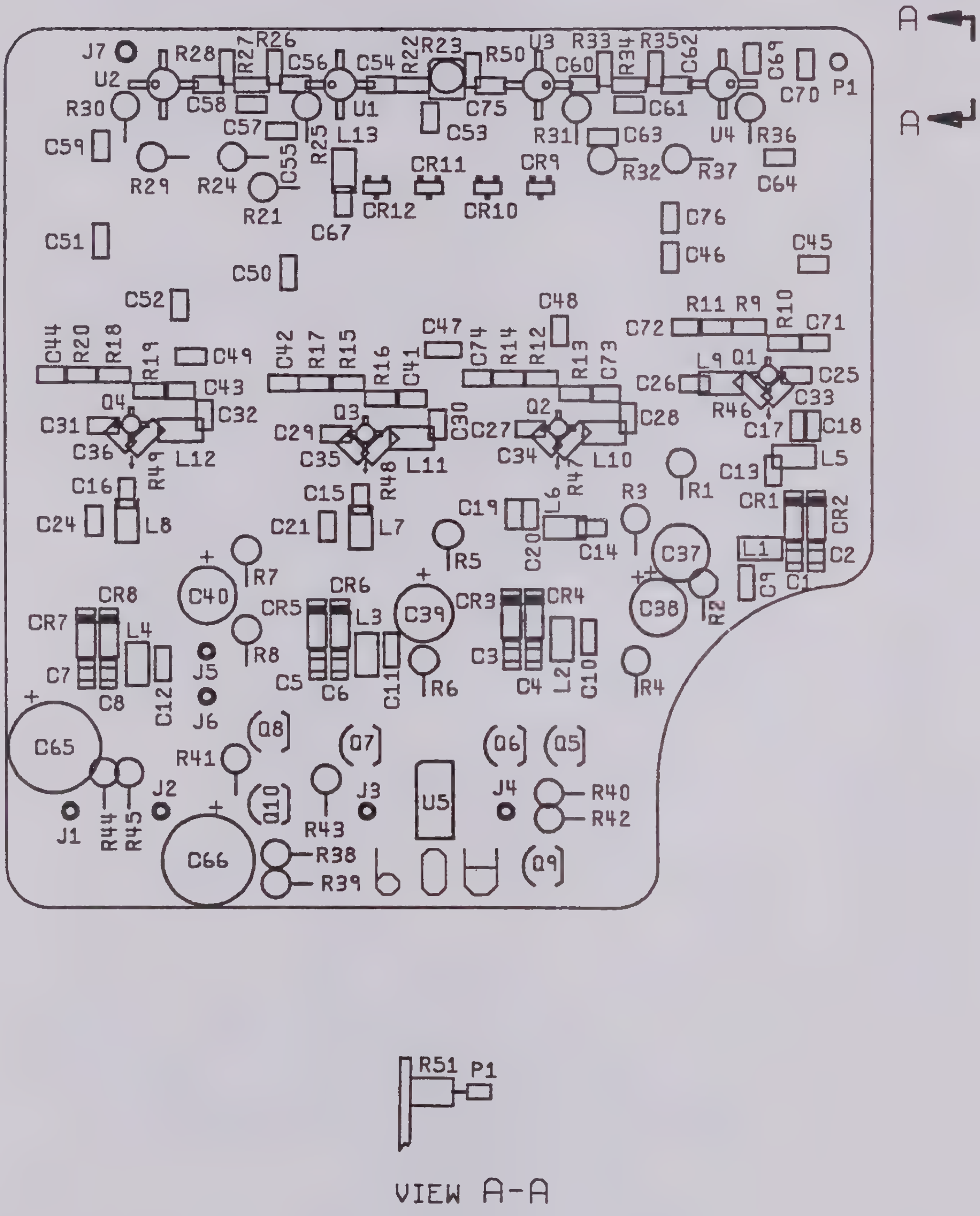
6082A-1640

Figure 8-8. A8 Output PCA

Table 8-9. A9 Sum Loop VCO PCA
(See Figure 8-9.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1- 4		CAP,PORC,1.8PF,+-0.1PF,50V,0505	800854	51406	MA181R8B	4	
C	5, 6		CAP,PORC,2.7PF,+-0.1PF,50V,0505	800862	51406	MA182R7B	2	
C	7		CAP,PORC,4.7PF,+-0.1PF,50V,0505	855098	51406	MA1844R7B	1	
C	8		CAP,PORC,3.6PF,+-0.1PF,50V,0505	806380	51406	MA183R6B	1	
C	9- 12		CAP,CER,22PF,+-10%,50V,C0G,1206	740563	04222	12065A220KAT060B	4	
C	13- 21, 24-		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	38	
C	32, 41- 44,			514133				
C	53- 56, 58-			514133				
C	60, 62- 64,			514133				
C	67, 71- 75			514133				
C	33, 48		CAP,CER,3.3PF,+-0.5PF,50V,C0G,0805	514208	51406	GRH708C0G3R3D200VPT	2	
C	34		CAP,CER,8.2PF,+-0.5PF,50V,C0G,0805	713982	95275	VJ0805Q8R2DXAT	1	
C	35, 52		CAP,CER,5.6PF,+-0.25PF,50V,C0G,0805	806778	04222	08055A5R6CAT1.3B	2	
C	36		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	1	
C	37- 40		CAP,TA,2.2UF,+-20%,25V	697425	56289	199D225X0025AG2	4	
C	45		CAP,CER,3.6PF,+-0.25PF,50V,C0G,0805	845169	04222	08055A3R6CAT051B	1	
C	46		CAP,CER,2.7PF,+-0.25PF,50V,C0G,0805	806752	04222	08055A2R7CAT1.3B	1	
C	47, 50		CAP,CER,4.3PF,+-10%,50V,C0G,1206	844738	04222	12065A4R3KAT060B	2	
C	49, 69, 70		CAP,CER,4.7PF,+-0.25PF,50V,C0G,0805	806760	04222	08055A4R7CAT1.3B	3	
C	51		CAP,CER,6.8PF,+-10%,50V,C0G,1206	747295	04222	12065A6R8KAT050B	1	
C	57, 61		CAP,CER,1.8PF,+-0.25PF,50V,C0G,0805	806745	04222	08055A1R8CAT1.3B	2	
C	65, 66		CAP,AL,470UF,+-20%,16V,SOLV PROOF	875497	62643	KME16VB471M10X12FT	2	
C	76		CAP,CER,1.0PF,+-0.5PF,50V,C0G,0805	512129	95275	VJ0805Q1R0DXAT	1	
CR	1- 8		DIODE,SI,VARACTOR,PIV=30V,18PF,MLF	866587	25403	BB215	8	
CR	9- 12	*	DIODE,SI,50V,PIN,RF SWITCHING,SOT23	854588	25088	BA885	4	
J	1- 6		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	6	
J	7		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	
L	1- 13		INDUCTOR,0.18UH,+-10%,770MHZ	800920	52763	S-5087227-213	13	
P	1		PIN,SINGLE,SOLDER,0.059 DIA	255901	55267	EJ20N22C000	1	
Q	1, 2	*	TRANSISTOR,SI,NPN,SM SIGNAL,HI FT	535153	33297	NE21935	2	
Q	3, 4	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	483156	33297	NE02135	2	
Q	5- 10	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	6	
R	1, 3, 5,		RES,CF,470,+-5%,0.25W	854567	59124	CF1-4 VT 471 J B	4	
R	7			854567				
R	2, 4, 6,		RES,CF,200,+-5%,0.25W	810390	59124	CF1-4 VT 201 J B	5	
R	8, 21			810390				
R	9, 12, 15,	*	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	91637	CRCW1206-47R0JB02	5	
R	18, 22	*		746263				
R	10, 11, 13,	*	RES,CERM,120,+-5%,.125W,200PPM,1206	746305	91637	CRCW1206-1200JB02	9	
R	14, 16, 17,	*		746305				
R	19, 20, 48	*		746305				
R	23		RES,VAR,CERM,500,+-30%,0.1W	876792	S4821	TRG043S1T-501	1	
R	24, 29, 32,		RES,CF,100,+-5%,0.25W	810465	59124	CF1-4 VT 101 J B	4	
R	37			810465				
R	25, 30, 31,		RES,CF,160,+-5%,0.25W	854724	59124	CF1-4 VT 161 J B	4	
R	36			854724				
R	26- 28, 33-	*	RES,CERM,82,+-5%,.125W,200PPM,1206	740480	91637	CRCW1206-82R0JB02	7	
R	35, 50	*		740480				
R	38, 40- 43		RES,MF,10K,+-1%,0.125W,100PPM	658914	59124	MF50DVT1002F REEL	5	
R	39		RES,CF,680,+-5%,0.25W	854570	59124	CF1-4 VT 681 J B	1	
R	44, 45		RES,CF,7.5,+-5%,0.25W	854559	59124	CF1-4 VT 7R5 J B	2	
R	46, 47	*	RES,CERM,150,+-5%,.125W,200PPM,1206	746313	91637	CRCW1206-1500JB02	2	
R	49	*	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	1	
R	51		RES,CC,150,+-5%,0.5W	186056	01121	EB1515	1	
U	1- 4	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	4	
U	5	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LM339DT	1	

An * in 'S' column indicates a static-sensitive part.


A
A
J7
U2
R28
R27
R26
C56
C54
R22
R23
R50
U3
R33
R34
R35
C62
C60
C69
C70
P1
R30
C58
U1
C75
R31
C61
U4
R36
C57
R25
L13
C53
C63
C59
R29
R24
C55
CR11
CR9
R32
R37
C64
R21
CR12
CR10
C67
C76
C51
C46
C45
C50
C52
C48
R11
R9
R10
C72
C71
C47
C44
R20
R18
R19
C49
C42
R17
R15
R16
C41
C74
R14
R12
R13
C73
L9
Q1
C26
C25
C43
C33
Q4
C32
Q3
C30
Q2
R46
C31
C29
C27
C28
C17
C18
C36
L12
C35
L11
C34
L10
R49
R48
R47
L5
C16
C15
R3
R1
C13
CR1
C24
L8
C21
L7
C19
L6
C20
C14
CR2
R5
C37
L1
C2
R7
C9
C1
CR8
C40
CR6
C39
CR3
CR4
C38
R2
CR7
L4
CR5
L3
J5
R8
C3
C7
C5
C6
C11
R6
C4
L2
C10
R4
C8
C12
J6
C65
Q8
Q7
Q6
Q5
R41
J2
J3
J4
R40
R42
Q10
U5
J1
R44
R45
C66
R43
R38
R39
Q9
R51
P1
VIEW A-A

6082A-1641

Figure 8-9. A9 Sum Loop VCO PCA

Table 8-10. A10 Premodulator PCA
(See Figure 8-10.)

REFERENCE DESIGNATOR -A>	NUMERICS	S	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTE
C	1, 45		CAP,CER,1.8PF,+-0.25PF,100V,C0K	512897	51406	RPE110C0K1R8C1	2	
C	2, 18, 20,		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	23	
C	23, 25, 31,			514133				
C	46,175,177,			514133				
C	179,181,183,			514133				
C	186,188,190,			514133				
C	192,194,196,			514133				
C	198,200,202,			514133				
C	380,381			514133				
C	3,342,345		CAP,CER,1.5PF,+-0.5PF,50V,C0G,0805	514166	51406	GRH708C0G1R5D200VPB	3	
C	4, 6, 9,		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	10	
C	12, 40- 42,			837609				
C	48, 52,376			837609				
C	5, 32, 86,		CAP,CER,6.8PF,+-0.25PF,100V,C0H	866553	04222	SR151A6R8CAA	5	
C	89, 90			866553				
C	7		CAP,VAR,0.5-1.3PF,250V,CER	783548	91293	9401-1	1	
C	8, 10, 13,		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	28	
C	22, 26, 28,			837542				
C	29, 49, 65,			837542				
C	66, 72, 73,			837542				
C	76- 78, 80,			837542				
C	82, 96, 97,			837542				
C	108,124,130-			837542				
C	132,134,210,			837542				
C	369,377			837542				
C	11		CAP,CER,4.7PF,+-0.5PF,50V,C0G,0805	855171	95275	VJ0805Q4R7DXAT	1	
C	14		CAP,CER,5.6PF,+-0.25PF,50V,C0G,0805	806778	04222	08055A5R6CAT1.3B	1	
C	15		CAP,CER,2.7PF,+-0.25PF,100V,C0J	363705	51406	RPE110C0J279C1	1	
C	16, 95		CAP,CER,10PF,+-2%,50V,C0G	713875	04222	SR595A100GAATR1A	2	
C	19,122,361		CAP,CER,0.68PF,+-0.25PF,100V,M7J	485011	51406	RPE110M7J684C1	3	
C	24, 30		CAP,CER,1.5PF,+-0.25PF,100V,C0K	529909	51406	RPE110C0K1R5C1	2	
C	33		CAP,CER,3.3PF,+-0.25PF,100V,C0J	519330	51406	RPE110C0J3R3C1	1	
C	34, 43, 44		CAP,CER,2.2PF,+-0.25PF,100V,C0G	362731	04222	SR15A2R2CAT	3	
C	35,362-364		CAP,CER,1.2PF,+-0.25PF,100V,C0K	543256	51406	RPE110C0K1R2C1	4	
C	36		CAP,CER,3.9PF,+-0.25PF,100V,C0J	512947	51406	RPE110C0J3R9C1	1	
C	37, 38,115,		CAP,CER,5.6PF,+-0.25PF,100V,C0H	512954	51406	RPE110C0H5R6C1	4	
C	116			512954				
C	39		CAP,CER,3.3PF,+-0.5PF,50V,C0G,0805	514208	51406	GRH708C0G3R3D200VPT	1	
C	50, 56, 69		CAP,TA,39UF,+-20%,6.3V	836890	56289	199D396X06R3DG2	3	
C	58, 61, 62,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	13	
C	64,118,120,			837526				
C	121,185,319,			837526				
C	320,323,324,			837526				
C	337			837526				
C	87, 88,391		CAP,CER,15PF,+-2%,100V,C0G	369074	59660	8101-100-C0G-150-G	3	
C	91		CAP,CER,15PF,+-2%,100V,C0G	832287	04222	SR591A150GAATR1A	1	
C	92, 93		CAP,CER,27PF,+-2%,100V,C0G	812107	04222	SR291A270GAATR1A	2	
C	94,113,114		CAP,CER,12PF,+-2%,100V,C0G	376871	59660	8101-100-C0G-126G	3	
C	109-111		CAP,CER,4700PF,+-20%,100V,X7R	866426	04222	SR151C472MAATR2A	3	
C	112		CAP,CER,8.2PF,+-0.25PF,100V,C0H	715359	51406	RPE110-C0H8R2C1	1	
C	117,123		CAP,CER,3300PF,+-10%,25V,X7R,0805	602870	04222	08051C332KAT050R	2	
C	119,214,215		CAP,AL,100UF,+50-20%,35V	416982	62643	SM35VB1008X11LL	3	
C	216		CAP,TA,68UF,+-20%,6.3V	821785	56289	199D686X06R3DG2	1	
C	341,343		CAP,CER,3.0PF,+-0.5PF,50V,C0G,0805	512137	95275	VJ0805Q3R0DXAT	2	
C	344,375		CAP,CER,1.0PF,+-0.5PF,50V,C0G,0805	512129	95275	VJ0805Q1R0DXAT	2	
C	346-348		CAP,CER,4700PF,+-20%,100V,C0G	743427	04222	SR591A472MAATR1A	3	
C	390		CAP,CER,10PF,+-2%,100V,C0G	512343	51406	RPE110A100G1	1	
CR	1- 4, 9-	*	DIODE,SI,PIN,100V,100MA	855077	33025	MA4P274	18	
CR	19, 22, 23,	*		855077				
CR	31	*		855077				
CR	20, 21	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	2	
CR	24- 30, 32,	*	DIODE,SI,PIN,SMALL SIGNAL,UHF & VHF	402776	28480	5082-3379 T-25	10	
CR	71, 72	*		402776				
J	1		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	1	1
J	2		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	1	1
J	5		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	
J	8- 10, 12		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	4	
J	11		SOCKET,SINGLE,PWB,FOR 0.034-0.037 PIN	732826	00779	2-332070-7	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-10. A10 Premodulator PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
J	16		CONN,COAX,SMB(M),PWB	352450	98291	51-051-0000-220	1	
L	2		INDUCTOR,10 TURNS	463448	89536	463448	1	
L	3, 18,107		INDUCTOR,0.12UH,+-10%,1000MHZ	800912	52763	S-5087227-013	3	
L	10, 39, 48,		CHOKE,6TURN	320911	89536	320911	6	
L	49,103,104			320911				
L	15- 17		INDUCTOR,0.68UH,+-10%,221MHZ,SHLD	320937	24759	MR-0.68	3	
L	22, 28		INDUCTOR,0.056UH,+-5%,1000MHZ	844907	52763	5087226-613	2	
L	23		INDUCTOR,0.047UH,+-5%,1000MHZ	844936	52763	5087226-513	1	
L	24, 40		INDUCTOR,0.039UH,+-10%,1000MHZ	844931	52763	5087226-423	2	
L	26		INDUCTOR,0.082UH,+-5%,1000MHZ	844915	52763	5087226-813	1	
L	27		INDUCTOR,0.068UH,+-5%,1000MHZ	844910	52763	5087226-713	1	
L	41, 42		INDUCTOR,0.022UH,+-20%,1000MHZ	844949	52763	S-5087226-233	2	
L	45		INDUCTOR,5.6UH,+-20%,130MHZ	844881	52763	5087230-723	1	
MP	1- 25		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	25	
MP	26		EXTENSION BOARD ASSEMBLY	879200	89536	879200	1	
Q	1, 4, 9,	*	TRANS,SI,NPN,SELECTED IEBO,SMALL SIG	685404	04713	SPS8763RLRA	4	
Q	10	*		685404				
Q	3, 7, 8	*	TRANSISTOR,SI,PNP,T092	698290	04713	MPS6562RLRA	3	
Q	5	*	TRANSISTOR,SI,PNP,T092	698233	04713	2N3906RLRA	1	
Q	6	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	722256	04713	MRF581	1	
R	1, 3	*	RES,CERM,220,+-5%,.125W,200PPM,1206	746347	91637	CRCW1206-2200JB02	2	
R	2	*	RES,CERM,22,+-5%,.125W,200PPM,1206	746230	91637	CRCW1206-22R0JB02	1	
R	4, 20, 40,		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	10	
R	45, 48, 53,			573212				
R	59, 64, 73,			573212				
R	78			573212				
R	5, 97		RES,CF,2K,+-5%,0.25W	573238	59124	CF1-4 202 J B	2	
R	6, 12, 14,	*	RES,CERM,130,+-5%,.125W,200PPM,1206	816041	91637	CRCW1206-1300JB02	5	
R	21, 23	*		816041				
R	7, 8, 15,	*	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	91637	CRCW1206-47R0JB02	4	
R	16	*		746263				
R	13, 22	*	RES,CERM,39,+-5%,.125W,200PPM,1206	746255	91637	CRCW1206-39R0JB02	2	
R	24, 26		RES,MF,422,+-1%,0.5W,100PPM	150821	91637	CMF65 4220 F T-1	2	
R	25, 27		RES,MF,301,+-1%,0.5W,100PPM	167494	91637	CMF65 3010 F T-1	2	
R	30- 35, 60,		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	15	
R	61, 81- 84,			573170				
R	94,276,277			573170				
R	36		RES,CF,2.7K,+-5%,0.25W	573261	59124	CF1-4 272 J B	1	
R	37		RES,CC,100,+-5%,0.5W	188508	01121	EB1015	1	
R	46		RES,MF,210,+-1%,0.5W,100PPM	513952	91637	CMF65 2100 F T-1	1	
R	49	*	RES,CERM,11,+-1%,.125W,100PPM,1206	780973	91637	CRCW1206-11R0FB02	1	
R	51		RES,VAR,CERM,500,+-10%,0.5W	325613	80294	3386R-1-501	1	
R	56		RES,CF,22,+-5%,0.125W	557215	59124	RDS21-8 22R0 J B	1	
R	62, 75, 76		RES,CF,51,+-5%,0.125W	740050	59124	CF1-8RDST 510 J B	3	
R	65, 66		RES,MF,301,+-1%,0.125W,100PPM	720029	91637	CMF55 3010 F T-1	2	
R	67, 85		RES,CF,100,+-5%,0.125W	557223	59124	RDS21-8 101 J B	2	
R	68,100,101		RES,CF,24,+-5%,0.125W	740043	59124	CF1-8RDS2 240 J B	3	
R	86, 87, 93,		RES,CF,110,+-5%,0.125W	740076	59124	CF1-8RDS2 111 J B	5	
R	307,309			740076				
R	88		RES,MF,82.5,+-1%,0.25,100PPM	799783	91637	CCF-5082R5F	1	
R	89, 90, 92		RES,CF,91,+-5%,0.125W	854380	59124	RDS21-8910J	3	
R	91		RES,MF,26.7,+-1%,0.125W,100PPM	855234	91637	CMF55 26R7 F T-1	1	
R	95		RES,MF,1.4K,+-1%,.125W,100PPM	851563	91637	CMF55 1401 F T-1	1	
R	96		RES,MF,2.55K,+-1%,0.125W,100PPM	719955	91637	CMF55 2551 F T-1	1	
R	98		RES,MF,59.0,+-1%,0.5W,100PPM	150920	91637	CMF65 59R0 F T-1	1	
R	99		RES,CF,160,+-5%,0.125W	740092	59124	CF1-8RDS2 161 J B	1	
R	102		RES,MF,511,+-1%,0.25W,100PPM	799684	91637	CCF-505110F	1	
R	103		RES,CF,360,+-5%,0.125W	772277	59124	RDS21-8 361 J B	1	
R	136,137		RES,CF,22,+-5%,0.25W	572966	59124	CF1-4 220 J B	2	
R	138		RES,CF,33K,+-5%,0.25W	573485	59124	CF1-4 333 J B	1	
R	139		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	1	
R	140	*	RES,CERM,18,+-5%,.125W,200PPM,1206	876128	91637	CRCW1206-180JB02	1	
R	300-302,305,		RES JUMPER,0.02,0.25W	682575	91637	FRJ-55	5	
R	310			682575				
R	303		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	
R	308		RES,CF,68,+-5%,0.125W	830893	59124	RDS21-8 680 J B	1	
R	332		RES,MF,150,+-1%,0.125W,100PPM	719674	91637	CMF55 1500 F T-1	1	
T	2		TRANSFORMER,RF,50KHZ-200MHZ,1:1	844832	1AV65	T1-1T-X65	1	
U	2, 11	*	IC,2.5 GHZ DIVIDE BY 2 PRESCALER,SOIC	854302	33297	UPB584G-E2	2	
U	4, 5, 12,	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	4	
U	13	*		867049				
U	8, 9, 58	*	IC,ECL,DUAL D M/S F/F,+EDGE TRIGGER	845099	04713	MC10H131P	3	

An * in 'S' column indicates a static-sensitive part.

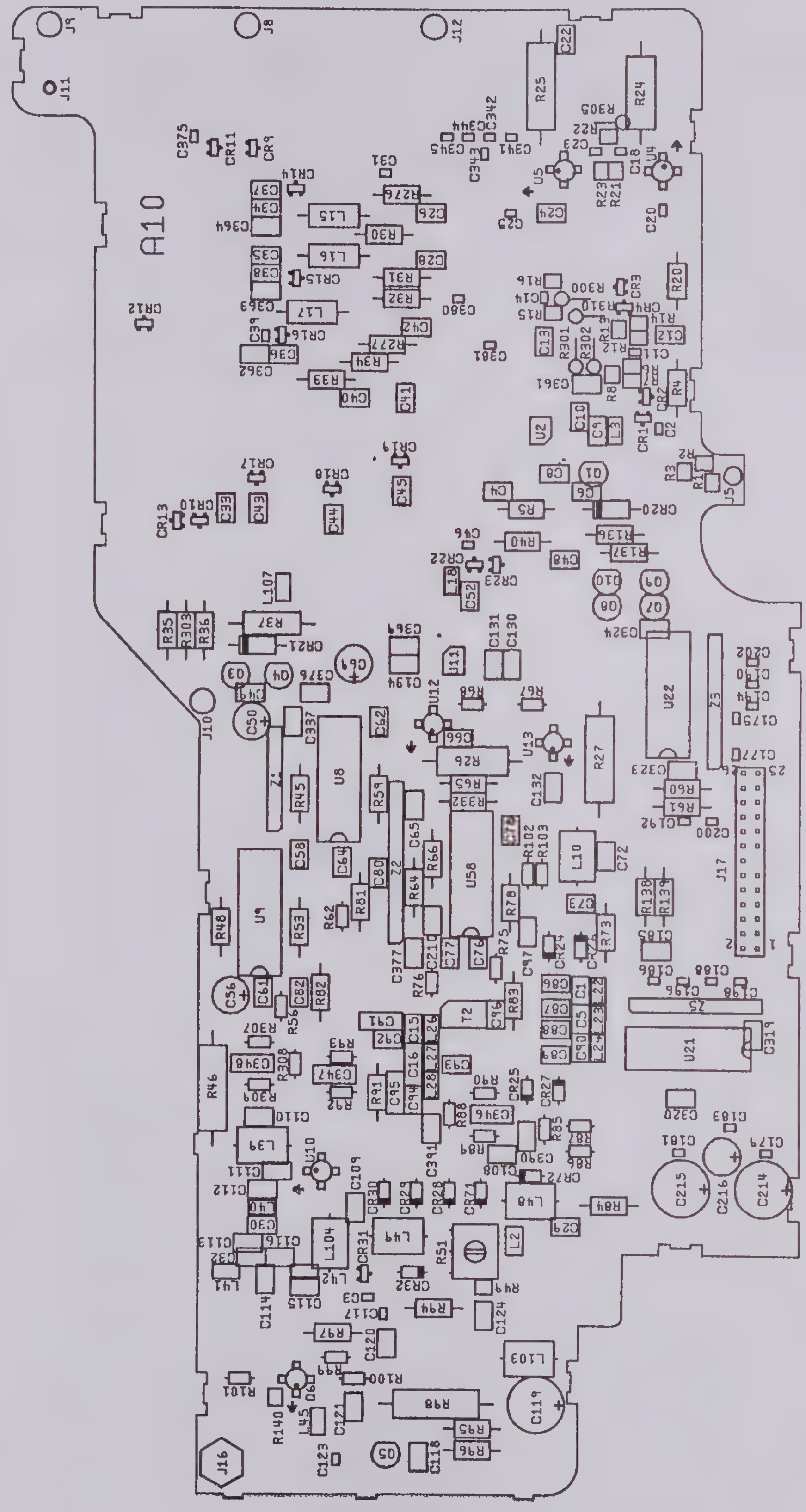
Table 8-10. A10 Premodulator PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	NOTE
U	10	*	IC,BPLR,SELECT GAIN MSA 0404 @ 2GHZ	773226	7E751	SMA85-2025	1	
U	21, 22	*	IC,OP AMP,QUAD,14 PIN DIP	402669	27014	LM324N	2	
Z	1		RES,CERM,SIP,6 PIN,5 RES,510,+-2%	459974	91637	CSC06A-01-511G	1	
Z	2		RES,CERM,SIP,10 PIN,9 RES,510,+-2%	478800	91637	CSC10A-01-511G	1	
Z	3, 5		RES,CERM,SIP,8 PIN,4 RES,1K,+-2%	714345	91637	CSC08A-03-102G	2	

An * in 'S' column indicates a static-sensitive part.

NOTES:

NOTE 1 = Components are installed on MP 26.


A10
J9
J8
J12
J11
C22
R25
R24
R305
R22
C23
C342
C344
C345
C343
C341
C18
U4
U5
R23
R21
C20
C24
C29
C375
CR11
CR9
CR14
C31
R276
C37
C34
C364
L15
C26
R30
C35
C38
L16
C28
CR15
R31
R32
R16
R300
CR3
R20
C14
R310
CR4
R15
R14
C363
L17
C380
CR12
C39
CR16
C42
R13
C13
R301
R302
C12
C36
R277
R12
C11
C362
R34
C381
R9
R8
R4
R33
C361
CR2
C40
C41
C10
C9
L3
U2
CR1
C2
CR19
CR17
CR18
R2
C8
Q1
R3
R1
C4
C6
J5
C45
C33
C43
R5
CR20
CR13
CR10
C44
C46
R40
R136
R137
CR22
C48
L18
CR23
L107
C52
Q10
Q9
Q8
Q7
R35
R303
R36
R37
C369
CR21
C131
C130
C324
C202
C61
C376
C194
J11
C70
Q3
Q4
C49
U12
R68
R67
U22
Z3
C74
C50
J10
C337
C62
C66
U13
R27
C175
C177
Z1
R45
U8
R59
R26
C323
25
R65
C132
R60
R332
R61
C192
C200
C58
C64
C80
C65
C71
R102
R103
L10
C72
J17
Z2
R66
U58
R64
R48
U9
R53
R62
R81
R78
C73
R138
R139
C185
R73
CR24
CR26
C377
C210
C77
C76
R75
C97
C186
C188
C196
C198
C56
C61
C82
R82
R76
R83
C86
C1
L22
2
1
R56
C91
C15
L26
T2
C96
C87
C5
L23
Z5
R307
C92
C88
C90
L24
U21
C319
R93
R308
C348
C347
C16
L27
C93
C89
R46
R91
C95
C94
L28
R90
CR25
CR27
R309
R92
C110
R88
C346
R85
C320
C183
L39
U10
C109
C391
R89
R87
C181
C179
C111
C390
R86
C108
CR72
C112
CR30
CR29
CR28
CR71
L48
R84
C215
C216
C214
L40
C30
C29
C113
C116
L104
L49
R51
L2
C32
CR31
L41
C114
L42
CR32
R49
C115
C3
C124
C117
R94
R97
C120
L103
R99
R100
R101
Q6
C119
R140
L45
C121
R98
R95
J16
C123
Q5
C118
R96

6082A-1646

Figure 8-10. A10 Premodulator PCA

Table 8-11. A11 Modulation Control PCA
(See Figure 8-11.)

REFERENCE DESIGNATOR -A>-	-NUMERICS---->	S	------------DESCRIPTION------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1		CAP,CER,1000PF,+-5%,100V,C0G	876003	04222	SR291A102JAATR1A	1	
C	2		CAP,CER,430PF,+-5%,50V,C0G	732644	04222	SR595A431JAATR1A	1	
C	8- 12, 16,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	52	
C	18, 20, 21,			837526				
C	23, 24, 27,			837526				
C	28, 30- 32,			837526				
C	36- 41, 43,			837526				
C	45, 46, 50,			837526				
C	52- 54, 56-			837526				
C	59, 72, 74,			837526				
C	79, 83- 86,			837526				
C	88, 89, 92,			837526				
C	101,103,105,			837526				
C	107,111-113,			837526				
C	126,140			837526				
C	13, 14		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	62643	KME50VB47RM6X11RP	2	
C	15		CAP,CER,4.7PF,+-0.25PF,100V,C0H	875455	04222	SR151A4R7CAATR2A	1	
C	19, 73, 77,		CAP,TA,10UF,+-20%,10V	714766	56289	199D106X0010BG2	5	
C	81, 82			714766				
C	22, 26		CAP,CER,33PF,+-2%,50V,C0G	715292	04222	SR595A330GAATR1A	2	
C	29, 62, 66,		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	5	
C	69,130			837609				
C	34		CAP,CER,560PF,+-5%,50V,C0G	875562	04222	SR595A561JAATR1A	1	
C	47, 51, 78,		CAP,TA,39UF,+-20%,6.3V	836890	56289	199D396X06R3DG2	4	
C	80			836890				
C	48, 49, 75,		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	4	
C	76			714774				
C	60, 61, 64,		CAP,AL,100UF,+-20%,16V,SOLV PROOF	816850	62643	KME16VB101M6.3X11RP	4	
C	65			816850				
C	67, 68		CAP,AL,22UF,+-20%,35V,SOLV PROOF	851766	62643	KRE35VB22RM6X5RP	2	
C	87		CAP,CER,3.3PF,+0.25PF,100V,C0J	816678	04222	SR591A3R3CAATR1A	1	
C	90		CAP,AL,220UF,+-20%,25V,SOLV PROOF	816793	62643	KME25VB221M8X11.5RP	1	
C	91		CAP,AL,22UF,+-20%,35V,SOLV PROOF	817056	62643	KMA35VB220M6X7PT	1	
C	102		CAP,AL,120UF,+-20%,35V,SOLV PROOF	866954	62643	SXF35VB121M8X12FT	1	
C	104,106,110,		CAP,POLYES,0.001UF,+-10%,50V	720938	60935	185-2/.001/K/0050/R/A/B	4	
C	137			720938				
C	108		CAP,CER,330PF,+-5%,100V,C0G	838474	04222	SR071A331JAATR1A	1	
C	109		CAP,CER,47PF,+-2%,100V,C0G	812123	04222	SR291A470GAATR1A	1	
C	123		CAP,CER,5.6PF,+-0.25PF,100V,C0H	512954	51406	RPE110C0H5R6C1	1	
C	124		CAP,CER,2.7PF,+-0.25PF,100V,C0J	816231	04222	SR071A2R7CAATR1A	1	
C	134		CAP,CER,680PF,+-5%,50V,C0G	743351	04222	SR595A681JAATR1A	1	
C	135		CAP,POLYES,0.22UF,+-10%,50V	706028	60935	185-2/0.22/K/0050/R/C/B	1	
C	136		CAP,CER,56PF,+-2%,50V,C0G	714378	04222	SR595A560GAATR1A	1	
C	139		CAP,TA,0.47UF,+-20%,35V	655035	56289	199D474X0035AG2	1	
CR	1, 13	*	ZENER,UNCOMP,6.2V,5%,20.0MA,0.4W	698662	04713	1N753A-SR4348RL	2	
CR	2	*	ZENER,UNCOMP,4.3V,5%,20.0MA,0.4W	851589	04713	1N749A	1	
CR	3, 4	*	DIODE,SI,BV= 50.0V,IO=150MA,SELCTD VF	234468	12040	1M916B	2	
CR	5, 6	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	535195	28480	5082-2800	2	
CR	7	*	ZENER,COMP, 6.4V, 5%, 1 PPM TC, 2.0MA	381988	04713	SZG20120	1	
CR	8- 11	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	4	
CR	12	*	BANDGAP REF DIODE, 1.22V, 35PPM TC	634154	27014	LM385BX-1.2	1	
CR	14- 16	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	3	
CR	17, 18	*	ZENER,UNCOMP,5.1V,5%,20.0MA,0.4W	159798	04713	1N751A	2	
J	13- 16, 20		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	5	
L	2		INDUCTOR,0.22UH,+-10%,400MHZ,SHLD	261735	24759	MR-0.2	1	
L	10, 11		INDUCTOR, 125UH	738484	89536	738484	2	
L	12		CHOKE,6TURN	320911	89536	320911	1	
MP	1- 7, 9-17,		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	61	
MP	19- 30,57- 8,			866764				
MP	70-74,77- 81,			866764				
MP	83-.91,118,			866764				
MP	119			866764				
MP	31- 37, 39-		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	49	
MP	51, 53- 56,			267500				
MP	92-103,105-			267500				
MP	117			267500				
MP	120,121		COMPONENT HOLDER	422865	98159	2829-75-2	2	
MP	122		SPACER,TRANSISTOR MOUNT,DAP,TO-18	175125	07047	10172-DAP	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-11. A11 Modulation Control PCA (cont.)

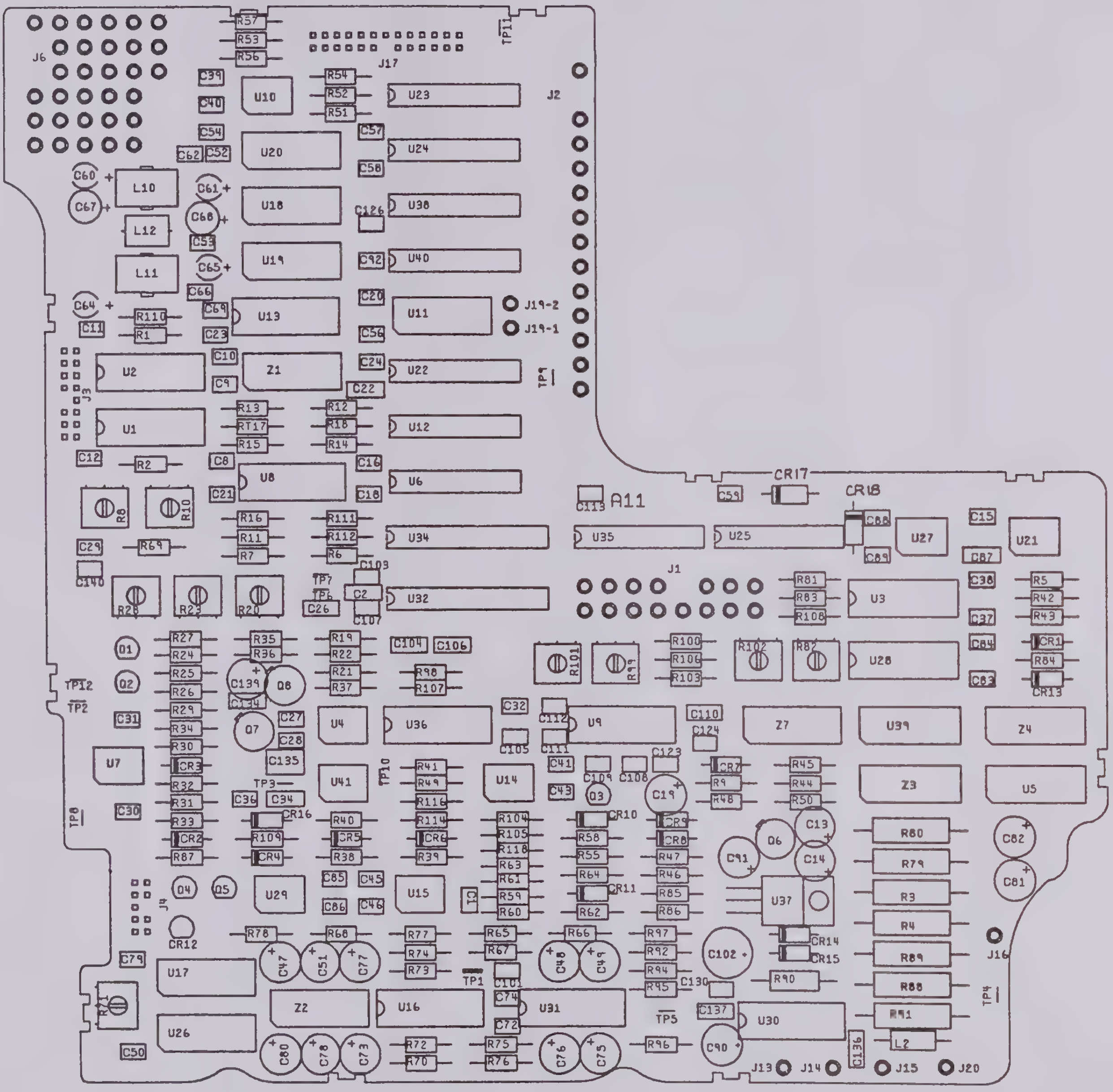
REFERENCE DESIGNATOR -A>-	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
Q	1	*	TRANSISTOR,SI,PNP,TO92	698233	04713	2N3906RLRA	1	
Q	2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	698225	04713	2N3904RLRA2	1	
Q	3	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	225599	07263	2N4250	1	
Q	4	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	330803	04713	MPS6560	1	
Q	5	*	TRANSISTOR,SI,PNP,TO92	698290	04713	MPS6562RLRA	1	
Q	6- 8	*	TRANSISTOR,SI,N-DMOS FET,TO-72	783308	17856	SD215DE	3	
R	1		RES,CF,33K,+-5%,0.25W	573485	59124	CF1-4 333 J B	1	
R	2, 45, 56,		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	5	
R	110,116			573311				
R	3, 4, 79,		RES,MF,1.37K,+-1%,0.5W,100PPM	148874	91637	CMF65 1371 F T-1	4	
R	80			148874				
R	5		RES,MF,40.2K,+-1%,0.125W,100PPM	720227	91637	CMF55 4022 F T-1	1	
R	6, 21		RES,CF,47,+-5%,0.25W	572982	59124	CF1-4 470 J B	2	
R	7, 22		RES,CF,56K,+-5%,0.25W	641126	59124	CF1-4 563 J B	2	
R	8, 23		RES,VAR,CERM,10K,+-10%,0.5W	309674	32997	3386R-1-103	2	
R	9, 34, 35		RES,MF,2.15K,+-1%,0.125W,100PPM	719880	91637	CMF55 2151 F T-1	3	
R	10, 28		RES,VAR,CERM,2K,+-10%,0.5W	309666	80294	3386R-1-202	2	
R	11		RES,MF,6.81K,+-1%,0.125W,100PPM	866314	91637	CMF55 6811 F T-1	1	
R	12,112		RES,MF,4.99K,+-1%,0.125W,100PPM	714923	91637	CMF55 4991 F T-1	2	
R	13		RES,MF,8.66K,+-1%,0.125W,100PPM	720557	91637	CMF55 8661 F T-1	1	
R	14		RES,MF,10K,+-1%,0.125W,100PPM	719476	91637	CMF55 1002 F T-1	1	
R	15		RES,MF,46.4K,+-1%,0.125W,50PPM	715185	91637	CMF55 4642 B T-2	1	
R	16		RES,MF,1.62K,+-1%,.125W,100PPM	851506	91637	CMF55 1621 F T-1	1	
R	18		RES,MF,649,+-1%,0.125W,100PPM	720458	91637	CMF55 6490 F T-1	1	
R	19,104		RES,MF,365,+-1%,0.125W,100PPM	459859	91637	CMF55 3650 F T-1	2	
R	20		RES,VAR,CERM,1K,+-10%,0.5W	275750	80294	3386R-1-102	1	
R	24, 26		RES,MF,20K,+-1%,0.125W,100PPM	719823	91637	CMF55 2002 F T-1	2	
R	25		RES,MF,66.5K,+-1%,0.125W,100PPM	866322	91637	CMF55 6652 F T-1	1	
R	27		RES,MF,100K,+-1%,0.125W,100PPM	719484	91637	CMF55 1003 F T-1	1	
R	29		RES,MF,49.9K,+-1%,0.125W,100PPM	720334	91637	CMF55 4992 F T-1	1	
R	30, 46		RES,MF,34.8K,+-1%,0.125W,100PPM	866306	91637	CMF55 3482 F T-1	2	
R	31		RES,MF,16.9K,+-1%,0.125W,100PPM	866293	91637	CMF55 1692 F T-1	1	
R	32		RES,MF,2.55K,+-1%,0.125W,100PPM	719955	91637	CMF55 2551 F T-1	1	
R	33, 94		RES,MF,499,+-1%,0.125W,100PPM	816462	91637	CMF55 4990 F T-1	2	
R	36		RES,MF,1.91K,+-1%,0.125W,100PPM	866277	91637	CMF55 1911 F T-1	1	
R	37		RES,MF,37.4K,+-1%,0.125W,100PPM	720177	91637	CMF55 3742 F T-1	1	
R	38		RES,MF,900,+-0.1%,0.125W,100PPM	443150	91637	CMF55 9000 B T-1	1	
R	39		RES,MF,1K,+-1%,0.125W,100PPM	719468	91637	CMF55 1001 F T-1	1	
R	40		RES,CF,100K,+-5%,0.25W	573584	59124	CF1-4 104 J B	1	
R	41		RES,CF,1,+-5%,0.25W	572883	59124	CF1-4 1R0 J B	1	
R	42, 52		RES,MF,24.3K,+-1%,0.125W,100PPM	719922	91637	CMF55 2432 F T-1	2	
R	43, 51		RES,MF,6.04K,+-1%,0.125W,100PPM	844667	91637	CMF55 6041 F T-1	2	
R	44		RES,MF,15.4K,+-1%,0.125W,100PPM	719708	91637	CMF55 1542 F T-1	1	
R	47, 57, 84,		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4 103 J B	4	
R	114			573394				
R	48,100,108		RES,MF,1.21K,+-1%,0.125W,100PPM	719559	91637	CMF55 1211 F T-1	3	
R	49, 73		RES,MF,2K,+-1%,0.125W,100PPM	719815	91637	CMF55 2001 F T-1	2	
R	50		RES,MF,5.49K,+-1%,0.125W,100PPM	720383	91637	CMF55 5491 F T-1	1	
R	53		RES,MF,9.31K,+-1%,0.125W,100PPM	866285	91637	CMF55 9311 F T-1	1	
R	54		RES,MF,3.48K,+-1%,0.125W,100PPM	832071	91637	CMF55 3481 F T-1	1	
R	55		RES,MF,1.5K,+-1%,0.125W,100PPM	719682	91637	CMF55 1501 F T-1	1	
R	58		RES,MF,3.4K,+-1%,0.125W,100PPM	866280	91637	CMF55 3401 F T-1	1	
R	59		RES,CF,5.1K,+-5%,0.25W	573329	59124	CF1-4 512 J B	1	
R	60, 61		RES,MF,4.02K,+-1%,.125W,25PPM	851480	91637	CMF55 4021 F T-9	2	
R	62		RES,MF,5.9K,+-1%,0.125W,100PPM	267351	91637	CMF55 5901 F T-1	1	
R	63		RES,MF,17.4K,+-1%,0.125W,100PPM	719740	91637	CMF55 1742 F T-1	1	
R	64		RES,MF,14.7K,+-1%,0.125W,100PPM	719666	91637	CMF55 1472 F T-1	1	
R	65, 68, 77,		RES,CF,30K,+-5%,0.25W	574251	59124	CF1-4 303 J B	4	
R	78			574251				
R	66, 76		RES,MF,9.09K,+-1%,0.125W,100PPM	720573	91637	CMF55 9091 F T-1	2	
R	67, 75, 95,		RES,CF,560,+-5%,0.25W	573147	59124	CF1-4 561 J B	5	
R	96,103			573147				
R	69		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	1	
R	70		RES,MF,31.6K,+-1%,0.125W,100PPM	720060	91637	CMF55 3162 F T-1	1	
R	71		RES,VAR,CERM,5K,+-10%,0.5W	288282	80294	3386S-1-502	1	
R	72		RES,MF,8.06K,+-1%,0.125W,100PPM	720524	91637	CMF55 8061 F T-1	1	
R	74		RES,MF,48.7K,+-1%,0.125W,100PPM	720300	91637	CMF55 4872 F T-1	1	
R	81		RES,MF,845,+-1%,.125W,100PPM	875513	91637	CMF55 8450 F T-1	1	
R	82		RES,VAR,CERM,50,+-10%,0.5W	285122	80294	3386S-1-502	1	
R	83		RES,MF,226,+-1%,0.125W,100PPM	866215	91637	CMF55 2260 F T-1	1	
R	85		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	1	
R	86		RES,CF,3.3K,+-5%,0.25W	573287	59124	CF1-4 332 J B	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-11. A11 Modulation Control PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R 87		RES,CF,22,+-5%,0.25W	572966	59124	CF1-4 220 J B	1	
R 88, 91		RES,MF,130,+-1%,0.5W,100PPM	151134	91637	CMF65 1300 F T-1	2	
R 89		RES,MF,205,+-1%,0.5W,100PPM	513960	91637	CMF65 2050 F T-1	1	
R 90		RES,CC,1K,+-5%,0.5W	108597	01121	EB1025	1	
R 92		RES,MF,124,+-1%,0.125W,100PPM	866194	91637	CMF55 1240 F T-1	1	
R 97		RES,MF,31.6,+-1%,0.125W,100PPM	855247	91637	CMF55 31R6 F T-1	1	
R 98,107		RES,MF,590,+-1%,0.125W,100PPM	866236	91637	CMF55 5900 F T-1	2	
R 99,101,102		RES,VAR,CERM,200,+-10%,0.5W	285148	80294	3386S-1-201	3	
R 105		RES,MF,634,+-1%,0.125W,100PPM	720441	91637	CMF55 6340 F T-1	1	
R 106		RES,MF,604,+-1%,0.125W,100PPM	832030	91637	CMF55 6040 F T-1	1	
R 109		RES,MF,200,+-1%,0.125W,100PPM	832063	91637	CMF55 2000 F T-1	1	
R 111		RES,MF,1.82K,+-1%,.125W,100PPM	851527	91637	CMF55 1821 F T-1	1	
R 118		RES,MF,3.92K,+-1%,0.125W,100PPM	844709	91637	CMF55 3921 F T-1	1	
RT 17		THERMISTOR,DISC,NEG.,10K,+-10%,25C	104596	15801	140-103LAG-A01	1	
TP 1		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	1	
TP 2- 12		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	11	
U 1, 2	*	IC,OP AMP,QUAD,14 PIN DIP	402669	27014	LM324N	2	
U 3, 16, 28	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	3	
U 4, 7, 14,	*	IC,OP AMP,LO-NOISE,8 PIN DIP	495051	18324	N35534N	4	
U 15	*		495051				
U 5, 39	*	IC,DMOS,FET QUAD SWITCH	507228	17856	SSD500203	2	
U 6	*	IC,CMOS,12 BIT,1/2 BIT,UP COMPATIBLE	851647	24355	AD7548KN	1	
U 8	*	IC,OP AMP,QUAD JFET INPUT,14 PIN DIP	659748	01295	TL074CN	1	
U 9	*	IC,OP AMP,QUAD,HIGH SPEED,LOW NOISE	845016	06665	OP471FY	1	
U 10	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	
U 11	*	IC,CMOS,8-BIT DAC WITH AMPLIFIER	845008	24355	AD7524JN	1	
U 12	*	IC,CMOS,14BIT DAC,12BIT ACC,CUR OUT	773101	24355	AD7534KN	1	
U 13	*	IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	01295	SN74LS11N	1	
U 17, 26	*	IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	404186	01295	SN74LS123N	2	
U 18- 20	*	IC,CMOS,3-8 LINE DCDR W/ENABLE	773036	01295	SN74HC138N	3	
U 21	*	IC,OP AMP,JFET INPUT,22V SUPPLY,DIP	832584	04713	LF356BN	1	
U 22- 25, 35,	*	IC,CMOS,OCTAL D F/F W/RESET	743286	18324	N74HCT273N	7	
U 38, 40	*		743286				
U 27	*	IC,OP AMP,PRECISION,LOW NOISE	816744	06665	OP-37GP	1	
U 29	*	IC,OP AMP,JFET IN,COMPENSTD,8 PIN DIP	418780	04713	MC34001P	1	
U 30	*	IC,COMPARATOR,HI-SPEED,14 PIN DIP	647115	18324	NE522N	1	
U 31	*	IC,FTTL,QUAD 2 INPUT NAND GATE	654640	04713	MC74F00N	1	
U 32, 34	*	IC,CMOS,DUAL 12-BIT DAC	845011	24355	AD7537KN	2	
U 36	*	IC,OP AMP,DUAL,PRECISION MATCHED	782375	64155	OP227GN	1	
U 37	*	IC,VOLT REG,FIXED,-8 VOLTS,1.5 AMPS	407635	04713	MC7908CT	1	
U 41	*	IC,OP AMP,LO-NOISE,8 PIN DIP	477745	18324	NE5534AN	1	
Z 1		RES,CERM,DIP,16 PIN,8 RES,1K,+-5%	358119	91637	MDP16-03-102J	1	
Z 2, 4		RES,CERM,DIP,16 PIN,8 RES,10K,+-5%	500710	91637	MDP16-03-103J	2	
Z 3, 7		RES,CERM,DIP,16 PIN,8 RES,10K,1%	501841	01121	316B103F	2	

An * in 'S' column indicates a static-sensitive part.


J6
R57
R53
R56
J17
TP11
J2
C39
C40
C54
C62
C52
U10
R54
R52
R51
U23
C57
U20
U24
C58
C60
C67
L10
C61
C68
L12
U18
C126
U38
C53
L11
C65
U19
C92
U40
C66
C64
C69
U13
C20
U11
J19-2
J19-1
C11
R110
R1
C23
C56
C10
C24
U2
Z1
U22
TP9
J3
C9
C22
U1
R13
RT17
R15
R12
R18
R14
U12
C12
R2
C8
U8
C16
U6
C21
C18
R8
R10
R16
R11
R7
R111
R112
R6
U34
CR17
C59
CR18
C113
A11
C88
U35
U25
U27
C15
U21
C29
R69
C140
C103
TP7
TP6
C2
C107
C26
U32
J1
C89
C87
R81
R83
R108
U3
C38
R5
R42
R43
R28
R23
R20
R27
R24
R25
R26
R29
R34
R30
CR3
R32
R31
R33
CR2
R87
R35
R36
C139
Q8
C134
C27
C28
Q7
C135
R19
R22
R21
R37
C104
C106
R98
R107
R101
R99
R100
R106
R103
R102
R82
U28
C37
C84
C83
CR1
R84
CR13
Q1
Q2
TP12
TP2
C31
U7
TP8
C30
U4
U36
C32
C112
C105
C111
U9
C110
C124
Z7
U39
Z4
C123
TP3
U41
TP10
R41
R49
R116
R114
CR6
R39
U14
C41
C43
C109
C108
Q3
C19
CR7
R9
R48
R45
R44
R50
Z3
U5
C36
C34
CR16
R40
R109
CR5
CR4
R38
R104
R105
R118
R63
R61
R59
R60
CR10
R58
R55
R64
CR11
R62
CR9
CR8
R47
R46
R85
R86
Q6
C13
C91
C14
U37
R80
R79
R3
R4
R89
R88
R91
L2
C82
C81
J16
TP4
Q4
Q5
J4
CR12
U29
C85
C86
C45
C46
U15
C1
R78
R68
R77
R74
R73
R65
R67
R66
R97
R92
R94
R95
C102
C130
CR14
CR15
R90
C79
U17
C47
C51
C77
C48
C49
TP1
C101
C74
R71
Z2
U16
U31
C72
TP5
C137
U30
C136
U26
C50
C80
C78
C73
R72
R70
R75
R76
C76
C75
R96
C90
J13
J14
J15
J20

6082A-1648

Figure 8-11. A11 Modulation Control PCA

Table 8-12. A12 Sum Loop PCA
(See Figure 8-12.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1, 81, 82		CAP,CER,2.7PF,+-0.25PF,50V,C0G,0805	806752	04222	08055A2R7CAT1.3B	3	
C	3, 4, 6,		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	10	
C	9, 10, 38,			837609				
C	65, 72, 91,			837609				
C	148			837609				
C	5		CAP,CER,3.9PF,+-0.5PF,100V,C0J	875448	04222	SR151A3R9DAATR2A	1	
C	7, 8, 11,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	28	
C	12, 50, 53,			837526				
C	54, 62, 67-			837526				
C	70, 75, 84,			837526				
C	105,111,112,			837526				
C	116,119,120,			837526				
C	126,129,130,			837526				
C	132-134,150,			837526				
C	151			837526				
C	13, 19		CAP,CER,4.7PF,+-0.25PF,50V,C0G,0805	806760	04222	08055A4R7CAT1.3B	2	
C	14,113		CAP,CER,10PF,+-2%,100V,C0G	875450	04222	SR151A100GAATR2A	2	
C	15- 18		CAP,CER,0.01UF,+-20%,100V,X7R	875489	04222	SR151C103MAATR2A	4	
C	21, 22		CAP,CER,4.7PF,+-0.25PF,100V,C0H	875455	04222	SR151A4R7CAATR2A	2	
C	23, 24		CAP,CER,10PF,+-5%,50V,C0G,0805	494781	51406	GRH708C0G100J200VPT	2	
C	26		CAP,CER,47PF,+-5%,50V,C0G,0805	494633	04222	08055A470JAT050B	1	
C	27, 28, 34-		CAP,CER,0.01UF,+-20%,50V,X7R	816249	04222	SR075C103MAATR1A	20	
C	36, 40, 55,			816249				
C	60, 61, 63,			816249				
C	64, 83,108,			816249				
C	141-146,149			816249				
C	33		CAP,CER,1000PF,+-20%,100V,X7R	837542	04222	SR151C102MAATR2A	1	
C	37		CAP,TA,2.2UF,+-20%,25V	697425	56289	199D225X0025AG2	1	
C	41		CAP,CER,68PF,+-5%,50V,C0G,0805	573857	04222	08055A680JAT050B	1	
C	42, 44, 76		CAP,CER,180PF,+-5%,50V,C0G,0805	853361	04222	08055A181JAT065B	3	
C	43		CAP,CER,100PF,+-5%,50V,C0G,0805	514133	51406	GRH708C0G101J200VPT	1	
C	45		CAP,CER,82PF,+-2%,100V,C0G	512350	04222	SR291A820GAATR1A	1	
C	46		CAP,CER,47PF,+-2%,100V,C0G	812123	04222	SR291A470GAATR1A	1	
C	47		CAP,CER,56PF,+-2%,100V,C0G	876136	04222	SR151A560GAATR2A	1	
C	49, 89		CAP,CER,4700PF,+-20%,100V,X7R	866426	04222	SR151C472MAATR2A	2	
C	56		CAP,CER,270PF,+-5%,50V,C0G	658898	04222	SR595A271JAATR1A	1	
C	57		CAP,CER,750PF,+-5%,50V,C0G	875484	04222	SR595A751JAATR1A	1	
C	58, 59		CAP,CER,430PF,+-5%,50V,C0G	732644	04222	SR595A431JAATR1A	2	
C	66		CAP,CER,0.01UF,+-10%,100V,X7R	557587	04222	SR591C103KAATR1A	1	
C	71		CAP,AL,22UF,+-20%,35V,SOLV PROOF	851766	62643	KRE35VB22RM6X5RP	1	
C	73		CAP,CER,39PF,+-5%,50V,C0G,0805	845102	95275	VJ0805Q390JXAT	1	
C	74		CAP,CER,18PF,+-5%,50V,C0G,0805	514224	51406	GRM708C0G180J200VPB	1	
C	77		CAP,TA,68UF,+-20%,6.3V	821785	56289	199D686X06R3DG2	1	
C	78		CAP,CER,39PF,+-2%,100V,C0G	816207	04222	SR291A390GAATR1A	1	
C	79, 80		CAP,CER,220PF,+-2%,100V,C0G	812131	04222	SR291A221GAATR1A	2	
C	92		CAP,CER,330PF,+-5%,100V,C0G	838474	04222	SR071A331JAATR1A	1	
C	101		CAP,POLYES,0.27UF,+-10%,50V	807867	60935	185-2/.27/K/0050/R/C/B	1	
C	102,131		CAP,POLYES,0.068UF,+-10%,50V	851175	60935	185-2/.068/K/0050/R/A/B	2	
C	103		CAP,POLYES,0.015UF,+-10%,50V	875492	68919	MKS21502K50	1	
C	104		CAP,POLYES,1UF,+-10%,50V	733089	60935	185-2/1/K/0050/R/A/B	1	
C	106,107		CAP,POLYES,0.22UF,+-10%,50V	706028	60935	185-2/0.22/K/0050/R/C/B	2	
C	115		CAP,POLYES,2200PF,+-10%,50V	832683	60935	185-2/222/K/0050/R/A/B	1	
C	121,124,125,		CAP,CER,3300PF,+-5%,50V,C0G	830612	04222	SR595A332JAATR1A	4	
C	135			830612				
C	127,138		CAP,POLYES,0.047UF,+-10%,50V	820548	60935	185-2/.047/K/0050/R/A/B	2	
C	128,140		CAP,TA,0.47UF,+-20%,35V	655035	56289	199D474X0035AG2	2	
C	136		CAP,POLYES,0.1UF,+-10%,50V	649913	60935	185-2/0.1/K/0050/R/A/B	1	
C	137		CAP,POLYES,0.47UF,+-10%,50V	697409	60935	185-2/0.47/K/0050/R/A/B	1	
C	139		CAP,POLYES,0.022UF,+-10%,50V	715268	60935	185-2/.022/K/0050/R/A/B	1	
C	152		CAP,AL,10UF,+-20%,63V,SOLV PROOF	816843	62643	KME63VB10RM5X11RP	1	
C	153		CAP,CER,68PF,+-2%,100V,C0G	362756	04222	SR291A680GAATR1A	1	
CR	1, 2	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	535195	28480	5082-2800	2	
CR	3	*	ZENER,UNCOMP,4.3V,5%,20.0MA,0.4W	851589	04713	1N749A	1	
CR	4	*	DIODE,SI,PIN,RF CUR CONT RESIST DIODE	742296	28480	QPND-4348	1	
CR	102	*	ZENER,UNCOMP,3.3V,10%,20.0MA,0.4W	698647	04713	1N746-SR4348RL	1	
CR	103,104	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	2	
CR	105	*	ZENER,UNCOMP,3.9V,10%,20.0MA,0.4W	698654	04713	IN748-SR4348RL	1	
CR	106	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	1	
CR	108	*	ZENER,UNCOMP,10.0V,5%,12.5MA,0.4W	698696	04713	1N961B-SR4348RL	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-12. A12 Sum Loop PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	----DESCRIPTION----	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
J	1- 6, 9,		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	25	
J	12- 16			866764				
J	10		CONN,COAX,SMB(M),PWB OR PANEL	512095	98291	051-051-0429-220	1	
J	11		CONN,COAX,SMA(M),PWB OR PANEL	512087	21845	2985-6011	1	
J	17		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	
K	102		RELAY,REED,1 FORM A,5VDC	461434	71707	1203-0085	1	
L	1, 2, 8,		INDUCTOR,10 TURNS	463448	89536	463448	5	
L	16, 19			463448				
L	3		INDUCTOR,0.022UH,+-20%,1000MHZ	844949	52763	S-5087226-233	1	
L	4, 20		INDUCTOR,0.10UH,+-5%,1000MHZ	844923	52763	5087226-913	2	
L	9, 23		INDUCTOR,0.33UH,+-5%,570MHZ	844886	52763	5087227-513	2	
L	10, 21		INDUCTOR,0.56UH,+-5%,440MHZ	844944	52763	5087227-813	2	
L	11, 25		INDUCTOR,0.12UH,+-10%,400MHZ,SHLD	272617	24759	MR-0.12	2	
L	13- 15, 26		INDUCTOR,1.8UH,+-5%,121MHZ,SHLD	806554	24759	MR-1.8	4	
L	18, 24		INDUCTOR,10UH,+-10%,53MHZ,SHLD	249078	24759	MR-10	2	
L	22		INDUCTOR,0.15UH,+-5%,825MHZ	844902	52763	5087227-113	1	
MP	15- 17, 19-		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	17	
MP	32			267500				
Q	1, 2, 6	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	722256	04713	MRF581	3	
Q	3, 4, 7	*	TRANSISTOR,SI,PNP,T092	698233	04713	2N3906RLRA	3	
Q	5, 8, 9,	*	TRANSISTOR,SI,NPN,HI-FREQ,SMALL SIGNL	535013	04713	BFR91	4	
Q	108	*		535013				
Q	10	*	TRANSISTOR,SI,NPN,HI-SPEED SW,TO-92	875521	12040	2N4274D26Z	1	
Q	11	*	TRANSISTOR,SI,PNP,HI-SPEED SWTICH	875385	04713	2N5771RLRA	1	
Q	101,103,105	*	TRANSISTOR,SI,JFET,LO-RDS(ON),TO-92	875526	12040	J108D26Z	3	
Q	106,107,109	*	TRANSISTOR,SI,N-JFET,TO-92,SWITCH	261578	17856	J2317	3	
R	4, 52, 54		RES,MF,162,+-1%,0.25W,100PPM	799890	91637	CCF-501620F	3	
R	5		RES,MF,121,+-1%,0.25W,100PPM	799734	91637	CCF-501210F	1	
R	6, 8, 11,		RES,MF,200,+-1%,0.25W,100PPM	799759	91637	CCF-502000F	6	
R	24, 50,154			799759				
R	7, 9		RES,MF,82.5,+-1%,0.25,100PPM	799783	91637	CCF-5082R5F	2	
R	10, 57, 58,		RES,MF,100,+-1%,0.25W,100PPM	799668	91637	CCF-501000F	4	
R	61			799668				
R	12		RES,MF,3.01K,+-1%,0.25W,100PPM	854356	91637	CCF-503011F	1	
R	13, 21,161		RES,MF,1K,+-1%,0.25W,100PPM	799791	91637	CCF-501001F	3	
R	14		RES,MF,5.62K,+-1%,0.125W,100PPM	720417	91637	CMF55 5621 F T-1	1	
R	15, 28, 36,		RES,MF,4.99K,+-1%,0.125W,100PPM	714923	91637	CMF55 4991 F T-1	6	
R	110,134,135			714923				
R	16		RES,MF,4.32K,+-1%,.125W,100PPM	851535	91637	CMF55 4321 F T-1	1	
R	17		RES,MF,80.6,+-1%,0.5W,100PPM	158790	91637	CMF65 80R6 F T-1	1	
R	18, 19, 29,		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	4	
R	31			573170				
R	20, 41	*	RES,CERM,51,+-5%,.125W,200PPM,1206	746271	91637	CRCW1206-51R0JB02	2	
R	22,117		RES,MF,750,+-1%,0.125W,100PPM	720516	91637	CMF55 7500 F T-1	2	
R	23, 53		RES,MF,182,+-1%,0.25W,100PPM	799726	91637	CCF-501820F	2	
R	25, 27		RES,MF,150,+-1%,0.125W,100PPM	719674	91637	CMF55 1500 F T-1	2	
R	26		RES,MF,37.4,+-1%,0.125W,100PPM	714501	91637	CMF55 37R4 F T-1	1	
R	30		RES,MF,464,+-1%,0.25W,100PPM	801282	91637	CCF-504640F	1	
R	32		RES,MF,2.94K,+-1%,0.125W,100PPM	261628	91637	CMF55 2941 F T-1	1	
R	33		RES,MF,12.1K,+-1%,0.125W,100PPM	719542	91637	CMF55 1212 F T-1	1	
R	34		RES,MF,348,+-1%,0.5W,100PPM	245761	91637	CMF65 3480 F T-1	1	
R	35		RES,MF,301,+-1%,0.5W,100PPM	167494	91637	CMF65 3010 F T-1	1	
R	37		RES,MF,6.65K,+-1%,0.125W,100PPM	720474	91637	CMF55 6651 F T-1	1	
R	38		RES,MF,14.3K,+-1%,0.125W,100PPM	291617	91637	CMF55 1432 F T-1	1	
R	39		RES,MF,453,+-1%,0.125W,100PPM	267393	91637	CMF 4530 F T-1	1	
R	40		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	
R	42, 71		RES,MF,68.1,+-1%,0.125W,100PPM	855270	91637	CMF55 68R1 F T-1	2	
R	43		RES,CF,300,+-5%,0.25W	643502	59124	CF1-4 301 J B	1	
R	44,169		RES,MF,392,+-1%,0.125W,100PPM	260299	91637	CMF55 3920 F T-1	2	
R	45		RES,MF,806,+-1%,0.125W,100PPM	223552	91637	CMF55 8060 F T-1	1	
R	47		RES,MF,523,+-1%,0.125W,100PPM	820274	59124	MF50DVT5230F REEL	1	
R	48		RES,MF,402,+-1%,0.125W,100PPM	720201	91637	CMF55 4020 F T-1	1	
R	49		RES,CF,4.3,+-5%,0.25W	640987	59124	CF1-4 4R3 J B	1	
R	51		RES,MF,11,+-1%,0.125W,100PPM	854729	59124	MF50DVT11R0F REEL	1	
R	55,144		RES,MF,357,+-1%,0.25W,100PPM	782045	91637	CCF-503570F	2	
R	56		RES,MF,51.1,+-1%,0.25W,100PPM	799650	91637	CCF-5051R1F	1	
R	59, 60		RES,CF,120,+-5%,0.25W	643494	59124	CF1-4 121 J B	2	
R	68		RES,CF,100,+-5%,0.25W	810465	59124	CF1-4 VT 101 J B	1	
R	69		RES,CF,4.7,+-5%,0.25W	816637	59124	CF1-4 VT 4R7 J B	1	
R	70		RES,MF,154,+-1%,0.125W,100PPM	866202	91637	CMF55 1540 F T-1	1	
R	72		RES,CF,5.1,+-5%,0.25W	640995	59124	CF1-4 5R1 J B	1	
R	73		RES,CF,110,+-5%,0.25W	643486	59124	CF1-4 111 J B	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-12. A12 Sum Loop PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R	74		RES,MF,33.2,+-1%,0.125W,100PPM	296681	91637	CMF55 33R2 F T-1	1	
R	75		RES,CF,24,+-5%,0.25W	572974	59124	CF1-4 240 J B	1	
R	76		RES,CF,130,+-5%,0.25W	573022	59124	CF1-4 131 J B	1	
R	77		RES,CF,75,+-5%,0.25W	631374	59124	CF1-4 750 J B	1	
R	101,123		RES,CF,13K,+-5%,0.25W	573410	59124	CF1-4 133 J B	2	
R	102,124,155		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	3	
R	103		RES,CF,20K,+-5%,0.25W	573444	59124	CF1-4 203 J B	1	
R	105		RES,MF,249,+-1%,0.125W,100PPM	816454	91637	CMF55 2490 F T-1	1	
R	106		RES,MF,1.15K,+-1%,0.125W,100PPM	293597	91637	CMF55 1151 F T-1	1	
R	107		RES,MF,4.87K,+-1%,0.125W,100PPM	720292	91637	CMF55 4871 F T-1	1	
R	108		RES,MF,64.9,+-1%,0.125W,100PPM	313338	91637	CMF55 64R9 F T-1	1	
R	109		RES,MF,1.54K,+-1%,0.125W,100PPM	289066	91637	CMF55 1541 F T-1	1	
R	111		RES,MF,3.01K,+-1%,0.125W,100PPM	720037	91637	CMF55 3011 F T-1	1	
R	112,116		RES,VAR,CERM,500,+-20%,0.5W	226068	80294	3329H-1-501	2	
R	113		RES,MF,845,+-1%,0.125W,100PPM	344317	91637	CMF55 8450 F T-1	1	
R	114		RES,MF,2.49K,+-1%,0.125W,100PPM	719930	91637	CMF55 2491 F T-1	1	
R	118		RES,CF,47K,+-5%,0.25W	573527	59124	CF1-4 473 J B	1	
R	119,120,122,		RES,MF,2K,+-1%,0.125W,100PPM	719815	91637	CMF55 2001 F T-1	6	
R	131,133,163			719815				
R	121		RES,VAR,CERM,200,+-20%,0.5W	226050	80294	3329H-1-201	1	
R	127		RES,MF,1.43K,+-1%,0.125W,100PPM	719633	91637	CMF55 1431 F T-1	1	
R	129		RES,MF,28.7K,+-1%,0.125W,100PPM	720011	91637	CMF55 2872 F T-1	1	
R	130		RES,MF,634,+-1%,0.125W,100PPM	720441	91637	CMF55 6340 F T-1	1	
R	132		RES,VAR,CERM,2K,+-20%,0.5W	226076	80294	3329H-1-202	1	
R	136		RES,MF,105,+-1%,0.125W,100PPM	236760	91637	CMF55 1050 F T-1	1	
R	137		RES,MF,619,+-1%,0.125W,100PPM	866244	91637	CMF55 6190 F T-1	1	
R	138		RES,MF,60.4,+-1%,0.125W,100PPM	235366	91637	CMF55 60R4 F T-1	1	
R	139		RES,MF,127,+-1%,0.125W,100PPM	866199	91637	CMF55 1270 F T-1	1	
R	140		RES,MF,232,+-1%,0.125W,100PPM	719906	91637	CMF55 2320 F T-1	1	
R	141		RES,MF,499,+-1%,0.125W,100PPM	816462	91637	CMF55 4990 F T-1	1	
R	142		RES,MF,1.02K,+-1%,0.125W,100PPM	223545	91637	CMF55 1021 F T-1	1	
R	143		RES,MF,2.1K,+-1%,0.125W,100PPM	168237	91637	CMF55 2101 F T-1	1	
R	145		RES,MF,7.32K,+-1%,0.125W,100PPM	853630	59124	MF50DVT7321B REEL	1	
R	146,160,170,		RES,CF,100K,+-5%,0.25W	573584	59124	CF1-4 104 J B	4	
R	171			573584				
R	148		RES,CF,4.7K,+-5%,0.25W	721571	59124	CF1-4 VT 472 J B	1	
R	149		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	1	
R	156		RES,MF,200,+-1%,0.125W,100PPM	820282	59124	MF50DVT2000F REEL	1	
R	157		RES,MF,93.1K,+-1%,0.125W,100PPM	817551	59124	MF50DVT9312F REEL	1	
R	158		RES,MF,15.4K,+-1%,0.125W,100PPM	772038	59124	MF50DVT1542J REEL	1	
R	159		RES,CF,30K,+-5%,0.25W	574251	59124	CF1-4 303 J B	1	
R	162		RES,MF,1.21K,+-1%,0.125W,100PPM	719559	91637	CMF55 1211 F T-1	1	
R	165,166		RES,MF,1.4K,+-1%,.125W,100PPM	851563	91637	CMF55 1401 F T-1	2	
R	167		RES,VAR,CERM,50,+-20%,0.5W	320861	80294	3329H-1-500	1	
R	168		RES,MF,137,+-1%,0.125W,100PPM	235218	91637	CMF55 1370 F T-1	1	
R	172		RES,CF,10K,+-5%,0.25W	697102	59124	CF1-4 VT 103 J B	1	
R	173		RES,MF,10K,+-1%,0.25W,100PPM	799635	91637	CCF-501002F	1	
R	174		RES,CF,22M,+-5%,0.25W	757104	59124	CF1-4 VT 226 J B	1	
R	175		RES,MF,392,+-1%,0.125W,100PPM	854732	59124	MF50DVT3920F REEL	1	
R	176	*	RES,CERM,150,+-5%,.125W,200PPM,1206	746313	91637	CRCW1206-1500JB02	1	
R	177		RES,MF,10K,+-1%,0.125W,100PPM	719476	91637	CMF55 1002 F T-1	1	
TP	1, 5, 7,		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	4	
TP	9			512889				
TP	2- 4, 6,		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	6	
TP	8, 15			816090				
U	1		MIXER,DOUBLE BALANCED,5 - 1000 MHZ	512103	1AV65	TFM-2H-8	1	
U	2		MIXER,DOUBLE BALANCED,2-500MHZ	851282	1AV65	TFM-1H	1	
U	3		MIXER,DOUBLE BALANCED,1-500MHZ	854039	1AV65	SBL-1-59	1	
U	4	*	IC,OP AMP,SELECTED GBW 600KHZ	418566	18324	LM358	1	
U	5	*	IC,STTL,DUAL D F/F,+EDG TRG,W/SET&CLR	418269	01295	SN74S74N	1	
U	7, 8	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	2	
U	9	*	IC,VOLT REG,FIXED,+5 VOLTS,0.1 AMPS	875588	04713	MC78L05ACPRLRA	1	
U	101,102,111	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	3	
U	103-106,108	*	IC,OP AMP,LO-NOISE,8 PIN DIP	495051	18324	N35534N	5	
U	107,113	*	IC,DMOS,FET QUAD SWITCH	507228	17856	SSD500203	2	
U	109	*	IC,CMOS,10BIT DAC,8BIT ACCUR,CUR OUT	524868	24355	AD7533JN	1	
U	110		PROM, SUM LOOP	860994	89536	860994	1	
U	112	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	
U	114	*	IC,LSTTL,DUAL MONOSTAB MULTIV W/SCHMT	404202	01295	SN74LS221N	1	
U	115	*	IC,COMPARATOR,HI-SPEED,14 PIN DIP	386920	18324	NE529N	1	
U	116	*	IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	412734	01295	SN74LS122N	1	
Z	101		RES,CERM,DIP,14 PIN,7 RES,100K,+-5%	516930	91637	MDP14-03-104J	1	

An * in 'S' column indicates a static-sensitive part.

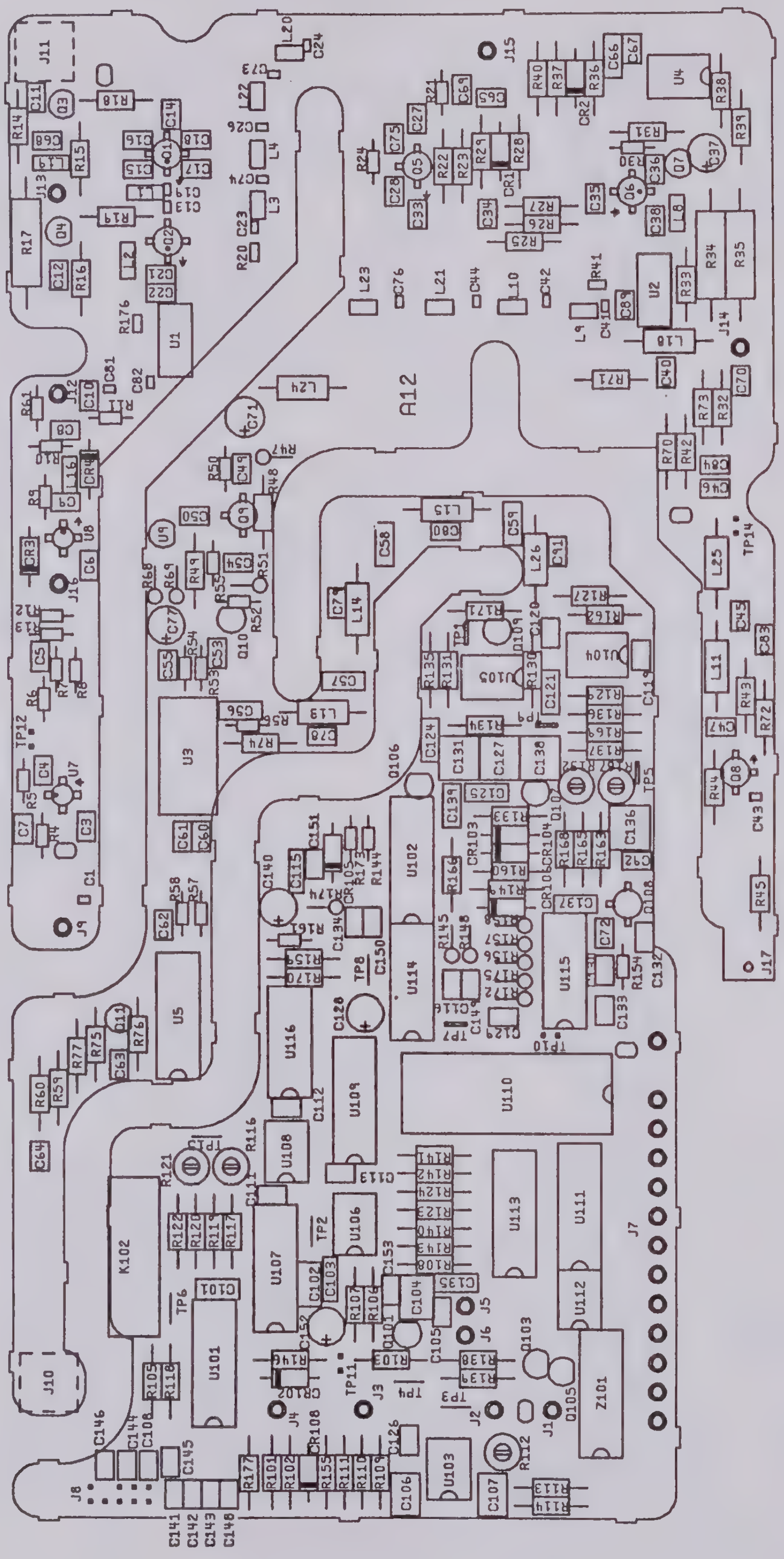


Figure 8-12. A12 Sum Loop PCA

Table 8-13. A13 Controller PCA
(See Figure 8-13.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE
C 1		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	62643	KME50VB47RM6X11RP	1	
C 2, 10, 11,		CAP,POLYES,0.1UF,+-10%,50V	649913	60935	185-2/0.1/K/0050/R/A/B	35	
C 15- 33, 35,			649913				
C 36, 52- 62			649913				
C 9, 34		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	2	
C 12, 13		CAP,CER,33PF,+-2%,100V,C0G	838466	04222	SR071A330GAATR1A	2	
C 14		CAP,TA,15UF,+-20%,20V	807610	56289	199D156X0020DG2	1	
C 37		CAP,CER,0.047UF,+-20%,50V,X7R	831487	04222	SR595C473MAATR1A	1	
C 38- 50, 63-		CAP,CER,220PF,+-20%,50V,C0G	740654	04222	SR595A221MAATR1A	20	
C 69			740654				
L 4		CHOKE,6TURN	320911	89536	320911	1	
MP 1- 6, 8-		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	118	
MP 12, 14- 67,			267500				
MP 69- 72			267500				
MP 99-109,111-		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	31	
MP 115,118-122,			866764				
MP 124-128,130-			866764				
MP 134			866764				
Q 1	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	150359	07263	2N3053	1	
R 1		RES,CF,1M,+-5%,0.25W	573691	59124	CF1-4 105 J B	1	
R 2		RES,CF,2K,+-5%,0.25W	573238	59124	CF1-4 202 J B	1	
R 3, 5		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	2	
R 4		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	
R 6		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	1	
R 7, 8		RES,CF,120,+-5%,0.25W	643494	59124	CF1-4 121 J B	2	
R 9, 10		RES,CF,51,+-5%,0.25W	572990	59124	CF1-4 510 J B	2	
R 11- 13		RES,CF,470,+-5%,0.25W	573121	59124	CF1-4 471 J B	3	
S 1		SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
TP 1- 4		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	4	
U 1	*	IC,CMOS,16 BIT MPU,8 MHZ,DIP	816926	04713	MC68HC000P-8	1	
U 2		IC,MOS,128K X 8 PROM,OTP,PROGRAMMED	882126	89536	882126	1	1
U 3		IC,MOS,128K X 8 PROM,OTP,PROGRAMMED	882134	89536	882134	1	1
U 4		IC,MOS,128K X 8 PROM,OTP,PROGRAMMED	879155	89536	879155	1	1
U 5		IC,MOS,128K X 8 PROM,OTP,PROGRAMMED	879098	89536	879098	1	1
U 6, 7	*	IC,CMOS,32K X 8 STATIC RAM,120 NSEC	800995	12581	HM62256LP-12	2	
U 8	*	IC,CMOS,8K X 8 STAT RAM,200 NSEC,NVM	810804	080A9	DS1225-200	1	
U 9		IC,NMOS,8K X 8 EEPROM,250 NSEC	800243	66419	XL2865AP-250	1	
U 11	*	IC,16V8,LOG ARRAY,6080A-90201	855049	27014	855049	1	
U 12	*	IC,CMOS,8 TO 3 LINE PRIORITY ENCODER	875476	01295	SN74HC148N	1	
U 13	*	IC,VOLT SUPERVISOR,4.55V SENSE INPUT	780577	01295	TI7705ACP	1	
U 14	*	IC,CMOS,DUAL DIV BY 16 BINARY CNTR	741488	04713	MC74HC393N	1	
U 15	*	IC,16V8,LOG ARRAY,6080A-90202	855051	27014	855051	1	
U 16	*	IC,CMOS,DUAL 4 INPUT NAND GATE	854026	01295	SN74HC20N	1	
U 17	*	IC,CMOS,HEX INVERTERS	799924	18324	74HCT04N	1	
U 18	*	IC,CMOS,HEX INVERTER,UNBUFFERED	741199	01295	SN74HCU04N	1	
U 19	*	IC,74HC05,HEX INVERTER W/OPEN DRAIN	854018	01295	SN74HC05N	1	
U 20	*	IC,CMOS,14 STAGE BINARY COUNTER	807701	04713	MC74HC4020N	1	
U 21	*	IC,CMOS,DUAL D F/F,+EDG TRG,W/CLR	741702	04713	SN74HC74N	1	
U 22	*	IC,FTTL,QUAD 2 INPUT OR GATE	659904	04713	MC74F32N	1	
U 23, 41, 42,	*	IC,CMOS,3-8 LINE DCDR W/ENABLE	773036	01295	SN74HC138N	4	
U 44	*		773036				
U 24, 25, 27,	*	IC,CMOS,OCTL LINE DRVR W/3-ST OUT	741892	01295	SN74HCT244N	5	
U 32, 33	*		741892				
U 26	*	IC,CMOS,QUAD BUS BUFFER W/3-STATE	854021	01295	74HC125N	1	
U 28	*	IC,NMOS,GPIB TALKER/LISTENER/CNTRLR	773143	33297	UPD7210 (C OR D)	1	
U 29	*	IC,LSTTL,OCTAL GPIB XCVR W/OPEN COL	585224	01295	SN75160BN	1	
U 30	*	IC,LSTTL,OCTAL GPIB ACTV PULL-UP XCVR	585232	01295	SN75161BN	1	
U 31	*	IC,CMOS,OCTAL BUS TRANSCEIVER	722017	27014	MM74HCT245N	1	
U 34, 38, 39	*	IC,CMOS,OCTAL D F/F W/RESET	743286	18324	N74HCT273N	3	
U 35- 37, 45	*	IC,CMOS,OCTAL D TRANSPARENT LATCH	743294	01295	SN74HCT373N	4	
U 40	*	IC,ARRAY,7 TRANS,NPN,DARLINGTON PAIRS	454116	01295	ULN2003AN	1	
U 43	*	IC,CMOS,QUAD 2 INPUT OR GATE	817312	04713	MC74HC32N	1	
XU 1		SOCKET,IC,64 PIN	483842	00779	643575-3	1	
XU 2- 5		SOCKET,IC,32 PIN	807156	00779	2-644018-3	4	
XU 6- 10		SOCKET,IC,28 PIN	448217	91506	228-AG39D	5	
XU 11, 15		SOCKET,IC,20 PIN	454421	00779	2-640464-1	2	
XU 28		SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
Y 1		CRYSTAL,8.00MHZ QUARTZ HC-18U	707133	89536	707133	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-13. A13 Controller PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
Z	1- 11, 14,		RES,CERM,SIP,10 PIN,9 RES,4.7K,+-2%	484063	91637	CSC10A-01-472G	17	
Z	17, 21- 23,			484063				
Z	25			484063				
Z	12, 16, 19		RES,CERM,SIP,6 PIN,5 RES,4.7K,+-2%	494690	91637	CSC06A-01-472G	3	
Z	20, 24		RES,CERM,DIP,16 PIN,8 RES,120,+-5%	448423	91637	MDP16-03-121J	2	

An * in 'S' column indicates a static-sensitive part.

NOTES:

NOTE 1 = U2-U5 are a match set. If one fails replace all four.

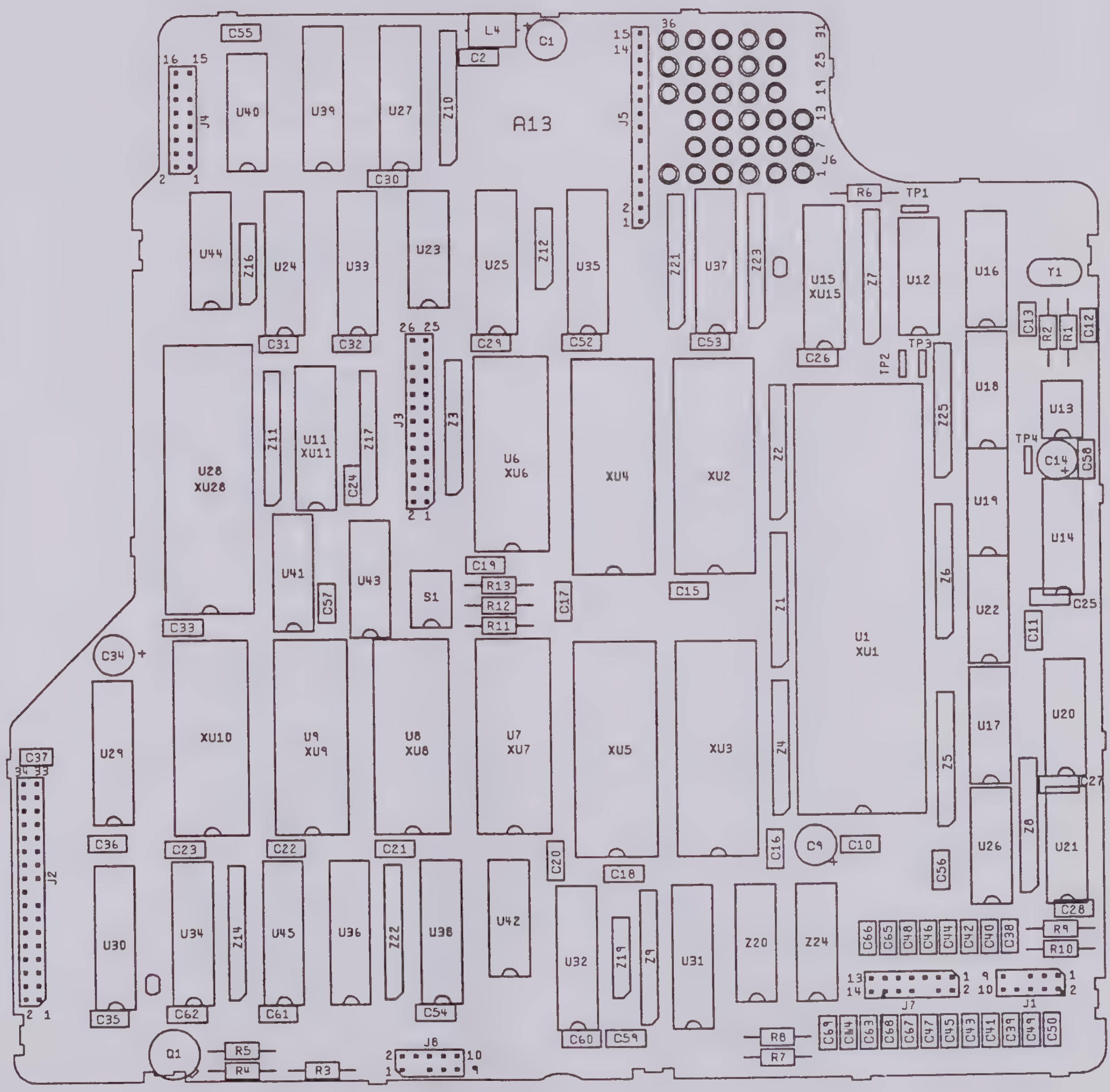

A13
C55
U40
U39
U27
Z10
L4
C1
C2
J4
16
15
2
1
C30
J5
15
14
2
1
36
31
25
19
13
7
1
J6
R6
TP1
U44
Z16
U24
U33
U23
U25
Z12
U35
Z21
U37
Z23
U15
XU15
Z7
U12
U16
Y1
C13
R2
R1
C12
C31
C32
C29
C52
C53
C26
TP2
TP3
26
25
J3
Z3
U28
XU28
Z11
U11
XU11
Z17
C24
U6
XU6
XU4
XU2
Z2
U1
XU1
Z25
U18
U13
TP4
C14
C58
U19
U14
U41
C57
U43
S1
C19
R13
R12
R11
C17
C15
Z1
Z6
U22
C25
C11
C33
C34
C37
34
33
J2
U29
XU10
U9
XU9
U8
XU8
U7
XU7
XU5
XU3
Z4
Z5
U17
U20
C27
Z8
C36
C23
C22
C21
C20
C16
C9
C10
C18
C56
U26
U21
C28
U30
U34
Z14
U45
U36
Z22
U38
U42
U32
Z19
Z9
U31
Z20
Z24
C66
C65
C48
C46
C44
C42
C40
C38
R9
R10
13
14
J7
9
10
J1
C35
C62
C61
C54
C60
C59
R8
R7
C69
C64
C63
C68
C67
C47
C45
C43
C41
C39
C49
C50
Q1
R5
R4
R3
J8
10
9
6082A-1643

Figure 8-13. A13 Controller PCA

Table 8-14. A14 FM PCA
(See Figure 8-14.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	NOTE
C	1, 8		CAP,AL,100UF,+50-20%,35V	416982	62643	SM35VB1008X11LL	2	
C	2, 4, 10,		CAP,CER,5.6PF,+-0.25PF,63V,U2J	853403	19701	R569C13U2JHWHAP	4	
C	11			853403				
C	5, 7, 22,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	29	
C	27, 29, 30,			837526				
C	35, 37, 40-			837526				
C	42, 61, 65,			837526				
C	66, 77- 87,			837526				
C	90- 92, 97			837526				
C	6, 12, 16,		CAP,CER,1000PF,+-2%,50V,C0G	807966	04222	SR595A102GAATR1A	10	
C	23, 25, 26,			807966				
C	28, 31, 71,			807966				
C	76			807966				
C	9		CAP,VAR,1 TO 10PF,250V,AIR	733212	91293	8052	1	
C	13		CAP,CER,56PF,+-2%,100V,C0G	512970	04222	SR151A560GAT	1	
C	14		CAP,CER,560PF,+-5%,50V,C0G	528505	04222	SR215A561JAT	1	
C	17, 18		CAP,TA,82UF,+-20%,20V	357392	56289	199D826X0020FA2	2	
C	19		CAP,CER,1.2PF,+-0.25PF,100V,C0K	543256	51406	RPE110C0K1R2C1	1	
C	20, 24		CAP,CER,100PF,+-2%,100V,C0G	837609	04222	SR151A101GAATR1A	2	
C	21		CAP,CER,3.9PF,+-0.25PF,100V,C0J	812149	04222	SR071A3R9CAATR1A	1	
C	32, 33, 60		CAP,TA,68UF,+-20%,16V	875422	56289	199D686X016EE2	3	
C	34, 59, 68,		CAP,TA,10UF,+-20%,35V	816512	56289	199D106X0035DG2	4	
C	69			816512				
C	36		CAP,TA,68UF,+-5%,25V	446450	56289	199D686X5025FA2	1	
C	38		CAP,CER,270PF,+-5%,50V,C0G	658898	04222	SR595A271JAATR1A	1	
C	39		CAP,CER,3300PF,+-5%,50V,C0G	528554	04222	SR215A332JAA	1	
C	43		CAP,TA,15UF,+-20%,20V	807610	56289	199D156X0020DG2	1	
C	44		CAP,CER,2000PF,+-5%,50V,C0G	832618	04222	SR215A202JAT	1	
C	45		CAP,POLYES,1UF,+-10%,50V	733089	60935	185-2/1/K/0050/R/A/B	1	
C	46		CAP,POLYES,0.01UF,+-10%,50V	715037	60935	185-2/0.01/K/0050/R/A/B	1	
C	47		CAP,POLYPR,470PF,+-1%,100V	844811	68919	FKP2 471F 100V	1	
C	48		CAP,POLYES,0.022UF,+-10%,50V	715268	60935	185-2/.022/K/0050/R/A/B	1	
C	49, 52, 53,		CAP,CER,330PF,+-5%,100V,C0G	838474	04222	SR071A331JAATR1A	5	
C	64, 67			838474				
C	50		CAP,POLYPR,2200PF,+-1%,100V	866889	68919	FKP2 222F 100V	1	
C	51, 88		CAP,POLYPR,4700PF,+-5%,63V	854513	68919	FKP2472J63V	2	
C	54- 56		CAP,TA,22UF,+-20%,15V	519074	56289	199D226X0015DA2	3	
C	57, 58		CAP,TA,22UF,+-20%,25V	845149	56289	199D226X0025DG2	2	
C	62		CAP,POLYPR,7150PF,+-1%,50V	422980	84411	JF-86 7150 F 50	1	
C	63		CAP,CER,47PF,+-2%,100V,C0G	812123	04222	SR291A470GAATR1A	1	
C	70		CAP,POLYPR,0.0786UF,+-1%,50V	422998	84411	JF-86 7862 F 50	1	
C	72, 89		CAP,POLYES,0.47UF,+-10%,50V	697409	60935	185-2/0.47/K/0050/R/A/B	2	
C	73		CAP,POLYPR,680PF,+-1%,100V	866892	68919	FKP2 681F 100V	1	
C	75		CAP,VAR,10-120PF,50V,CER	631416	51406	TZ03R121FR174	1	
C	93		CAP,TA,1UF,+-20%,35V	697417	56289	199D105X0035AG2	1	
C	94		CAP,CER,680PF,+-5%,50V,C0G	743351	04222	SR595A681JAATR1A	1	
C	95, 96,101,		CAP,TA,10UF,+-20%,25V	714774	56289	199D106X0025CG2	4	
C	102			714774				
C	98		CAP,CER,3300PF,+-5%,50V,C0G	830612	04222	SR595A332JAATR1A	1	
C	99		CAP,CER,6800PF,+-5%,100V,C0G	816710	04222	SR301A682JAATR1A	1	
C	100		CAP,CER,120PF,+-5%,50V,C0G	721142	04222	SR595A121JAAR1AT	1	
C	103,107		CAP,TA,22UF,+-20%,10V	658971	56289	199D226X0010CG2	2	
C	104		CAP,CER,1800PF,+-5%,50V,C0G	832717	04222	SR595A182JAATR1A	1	
C	105,106		CAP,TA,33UF,+-10%,6V	866897	56289	199D336X9006CG2	2	
CR	1- 8		DIODE,SI,VARACTOR,PIV= 28V	741504	25403	BB405B	8	
CR	13	*	DIODE,SI,PIN,RF SWITCHING	875591	OGNL3	BA483-143	1	
CR	14	*	ZENER,COMP,6.3V,3%,10PPM,2MA	357848	04713	SZF2018	1	
CR	15, 17, 20-	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	313247	28480	5082-6264 T25	8	
CR	24, 33	*		313247				
CR	18, 19, 25,	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	4	
CR	26	*		698720				
CR	27, 28, 30-	*	DIODE,SI,BV= 75.0V,RADIAL INSERTED	659516	03508	1N4448	5	
CR	32	*		659516				
CR	35	*	ZENER,UNCOMP,5.1V,5%,20MA,0.4W	866772	04713	IN751ARR1	1	
CR	36	*	ZENER,UNCOMP,9.1V,5%,5MA,0.350W	853788	04713	1N5239BRR1	1	
J	2, 4, 6,		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	21	
J	7			866764				
J	3		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-14. A14 FM PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	NOTE
K	1, 2		RELAY,REED,1 FORM A,5VDC	461434	71707	1203-0085	2	
K	4		RELAY,ARMATURE,2 FORM C,5V	733063	61529	DS2E-S-DC5V	1	
L	1		VAR. 0.194UH INDUCTOR, MODIFIED	845057	02113	142-05J08S	1	
L	2, 3		INDUCTOR,3.3UH,+-10%,88MHZ,SHLD	174714	24759	MR-3.3	2	
L	4		INDUCTOR,3.9UH,+-5%,84MHZ,SHLD	413864	24759	MR-3.9	1	
L	5		INDUCTOR,6800UH,+-10%,1.5MHZ,SHLD	363184	24759	MR-6800	1	
L	6		INDUCTOR, VARIABLE, 4.61UH	861138	89536	861138	1	
L	7		INDUCTOR,2200UH,+-10%,2.2MHZ,SHLD	147801	24759	MR-2200	1	
L	8- 16, 18-		CHOKE,6TURN	320911	89536	320911	15	
L	20, 22- 24			320911				
L	17, 21		INDUCTOR,10 TURNS	463448	89536	463448	2	
MP	19- 21, 23-		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	11	
MP	28			267500				
Q	1, 2	*	TRANSISTOR,SI,N-JFET,UHF/VHF USE	403634	17856	J2765	2	
Q	3	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	832170	04713	MPS6520RLRA	1	
Q	4	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	844993	55464	MPS6522	1	
Q	5, 8, 9	*	TRANSISTOR,SI,PNP,T092	698290	04713	MPS6562RLRA	3	
Q	6, 7	*	TRANS,SI,NPN,SELECTED IEBO,SMALL SIG	685404	04713	SPS8763RLRA	2	
Q	10	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	875401	04713	MPS918RLRA	1	
Q	11	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	248351	04713	MPS918	1	
Q	12, 13	*	TRANSISTOR,SI,PNP,HI-SPEED SWTICH	875385	04713	2N5771RLRA	2	
Q	14, 15, 18	*	TRANSISTOR,SI,N-DMOS FET,TO-72	477729	18324	SD213EE	3	
Q	16	*	TRANSISTOR,SI,N-DMOS FET,TO-72	783308	17856	SD215DE	1	
Q	17	*	TRANSISTOR,SI,VMOS,PWR,TO-237,VN10KM	640516	17856	V11809	1	
R	1, 7		RES,CF,1.8K,+-5%,0.25W	866736	59124	CF1-4 VT 182 J B	2	
R	2, 3		RES,CF,360,+-5%,0.25W	573097	59124	CF1-4 361 J B	2	
R	4		RES,CC,10K,+-10%,0.125W	246975	01121	BB3035	1	
R	5, 6		RES,MF,2K,+-1%,0.125W,100PPM	719815	91637	CMF55 2001 F T-1	2	
R	8, 9,112,		RES,CF,47,+-5%,0.25W	822189	59124	CF1-4 VT 470 J B	4	
R	113			822189				
R	10		RES,CC,15,+-10%,0.125W	261800	01121	BB1531	1	
R	11, 21, 22		RES,CC,10,+-10%,0.125W	321125	01121	BB1001	3	
R	12, 15		RES,CC,68,+-10%,0.125W	261818	01121	BB6801	2	
R	13, 14, 16		RES,CC,100,+-10%,0.125W	261826	01121	BB1011	3	
R	17, 19		RES,CF,56,+-5%,0.25W	641068	59124	CF1-4 560 J B	2	
R	18, 20		RES,CC,220,+-5%,0.5W	186031	01121	EB2215	2	
R	24		RES,CF,13K,+-5%,.25W	875372	59124	CF1-4VT 133 J B	1	
R	25, 67, 86		RES,CF,1.5K,+-5%,0.25W	810432	59124	CF1-4 VT 152 J B	3	
R	26, 27		RES,CF,360,+-5%,0.25W	747527	59124	CF1-4 VT 361 J B	2	
R	28, 29, 73		RES,CF,2.2K,+-5%,0.25W	851840	59124	CF1-4 VT 222 J B	3	
R	30, 50		RES,CF,100K,+-5%,0.25W	658963	59124	CF1-4 VT 104 J B	2	
R	31, 32,108,		RES,MF,2K,+-1%,0.125W,100PPM	816629	59124	MF50DVT2001F REEL	5	
R	110,111			816629				
R	33		RES,CC,33,+-10%,0.125W	272914	01121	BB3301	1	
R	34		RES,CF,100,+-5%,0.25W	810465	59124	CF1-4 VT 101 J B	1	
R	35,107		RES,VAR,CERM,1K,+-10%,0.5W	393728	80294	3299W-1-102	2	
R	36		RES,MF,2.49K,+-1%,0.125W,100PPM	810523	59124	MF50DVT2491F REEL	1	
R	37		RES,MF,4.99K,+-1%,0.125W,100PPM	721548	59124	MF55D4991F	1	
R	38		RES,MF,5.49K,+-1%,0.125W,100PPM	721795	59124	MF50DVT5491F REEL	1	
R	39		RES,VAR,CERM,5K,+-10%,0.5W	493593	80294	3299W-1-502	1	
R	40,127		RES,MF,453,+-1%,0.125W,100PPM	866681	59124	MF50DVT4530F REEL	2	
R	41		RES,MF,68.1,+-1%,0.125W,100PPM	855270	91637	CMF55 68R1 F T-1	1	
R	42,137		RES,CF,2K,+-5%,0.25W	810457	59124	CF1-4 VT 202 J B	2	
R	43		RES,CF,12K,+-5%,0.25W	757799	59124	CF1-4 VT 123 J B	1	
R	44,119		RES,VAR,CERM,20K,+-20%,0.5W	234443	80294	3329H-1-203	2	
R	45		RES,VAR,CERM,50,+-20%,0.5W	320861	80294	3329H-1-500	1	
R	46		RES,CF,2.4K,+-5%,0.25W	866710	59124	CF1-4 VT 242 J B	1	
R	47		RES,CF,10K,+-5%,0.25W	697102	59124	CF1-4 VT 103 J B	1	
R	48		RES,CF,1K,+-5%,0.25W	780585	59124	CF1-4 VT 102 J B	1	
R	49, 63, 88,		RES,VAR,CERM,100K,+-30%,0.5W	193045	80294	3329H-1-104	4	
R	117			193045				
R	51		RES,CF,1.2K,+-5%,0.25W	573196	59124	CF1-4 122 J B	1	
R	52		RES,MF,36.5,+-1%,0.125W,100PPM	855259	91637	CMF55 36R5 F T-1	1	
R	53		RES,CC,43,+-5%,0.125W	715391	01121	BB4305	1	
R	54		RES,MF,39.2,+-1%,0.125W,100PPM	855262	91637	CMF55 39R2 F T-1	1	
R	55		RES,MF,182,+-1%,0.125W,100PPM	719757	91637	CMF55 1820 F T-1	1	
R	56		RES,CF,47K,+-5%,0.25W	721787	59124	CF1-4 VT 473 J B	1	
R	57		RES,CF,1.5K,+-5%,0.25W	573212	59124	CF1-4 152 J B	1	
R	58, 65, 90,		RES,CF,4.7K,+-5%,0.25W	721571	59124	CF1-4 VT 472 J B	5	
R	93,121			721571				
R	59		RES,CF,820,+-5%,0.25W	574970	59124	CF1-4 821 J B	1	
R	60		RES,CF,100,+-5%,0.25W	573014	59124	CF1-4 101 J B	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-14. A14 FM PCA (cont.)

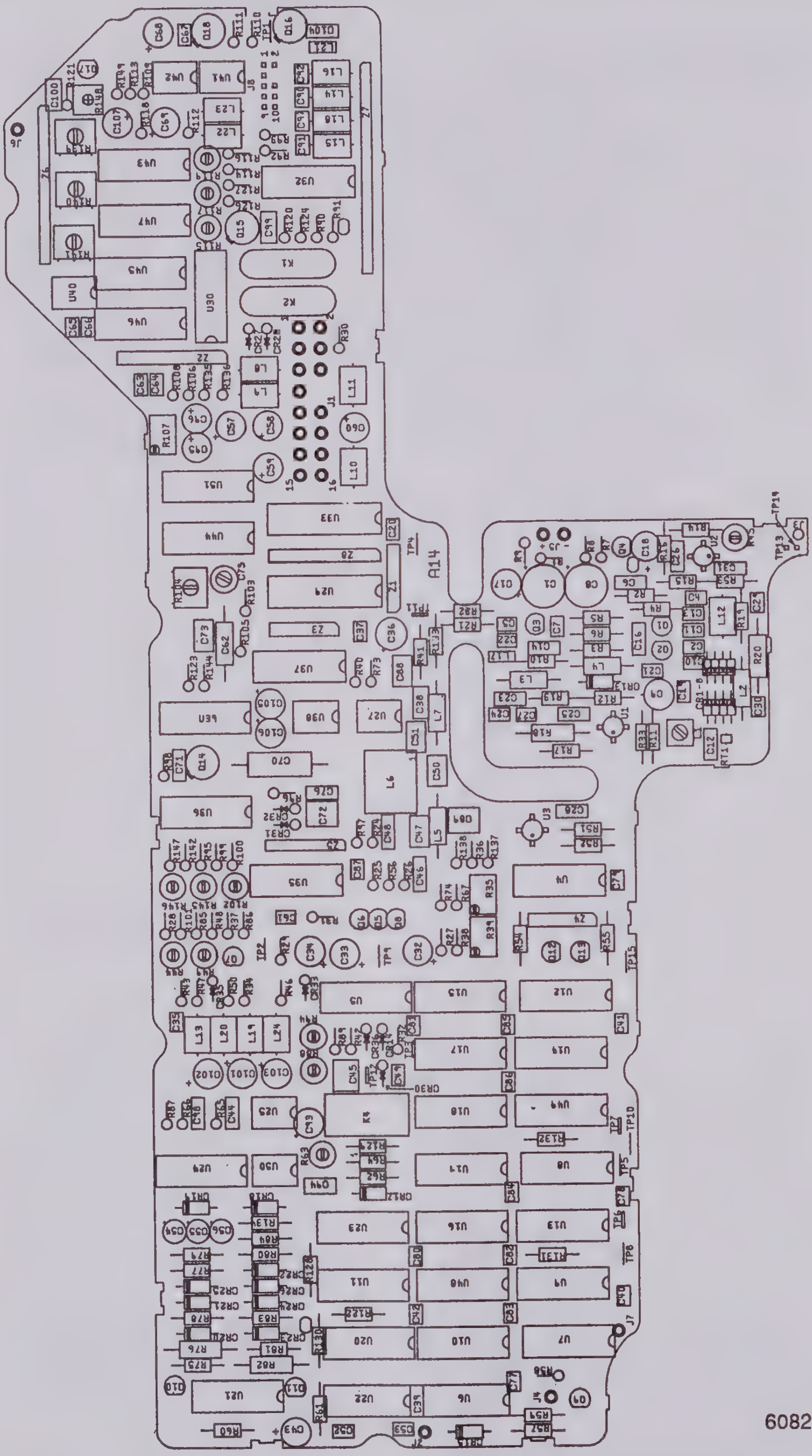
REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R 61		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4 103 J B	1	
R 62,128,130		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	3	
R 64		RES,MF,150K,+-1%,0.125W,100PPM	866327	91637	CMF55 1503 F T-1	1	
R 66		RES,MF,8.45K,+-1%,0.125W,100PPM	866673	59124	MF50DVT8451F REEL	1	
R 74		RES,MF,499,+-1%,0.125W,100PPM	866686	59124	MF50DVT4990F REEL	1	
R 75, 81		RES,CF,36,+-5%,0.25W	643817	59124	CF1-4 360 J B	2	
R 76, 82		RES,CC,510,+-5%,0.5W	108951	01121	EB5115	2	
R 77, 84		RES,MF,4.99K,+-1%,0.125W,100PPM	714923	91637	CMF55 4991 F T-1	2	
R 78, 83		RES,MF,10K,+-1%,0.125W,100PPM	719476	91637	CMF55 1002 F T-1	2	
R 79		RES,MF,22.6K,+-1%,0.125W,100PPM	866301	91637	CMF55 2262 F T-1	1	
R 80		RES,MF,44.2K,+-1%,0.125W,25PPM	844675	91637	CMF55 4422 F T-9	1	
R 85		RES,CF,3.6K,+-5%,0.25W	866715	59124	CF1-4 VT 362 J B	1	
R 87		RES,MF,47.5K,+-1%,0.125W,100PPM	866665	59124	MF50DVT4752F REEL	1	
R 89,123		RES,CF,33K,+-5%,0.25W	733667	59124	CF1-4 VT 333 J B	2	
R 91, 92		RES,CF,3.3K,+-5%,0.25W	854554	59124	CF1-4VT 332J B	2	
R 94,146		RES,VAR,CERM,100,+-20%,0.5W	193052	80294	3329H-1-101	2	
R 95		RES,MF,442K,+-1%,0.125W,100PPM	866678	59124	MF50DVT4423F REEL	1	
R 96		RES,CF,1M,+-5%,0.25W	649970	59124	CF1-4 VT 105 J B	1	
R 97		RES,CF,5.1K,+-5%,0.25W	866723	59124	CF1-4 VT 512 J B	1	
R 98,101		RES,MF,7.5K,+-1%,0.125W,100PPM	866660	59124	MF50DVT7501F REEL	2	
R 99		RES,CF,4.7M,+-5%,0.25W	866731	59124	CF1-4 VT 475 J B	1	
R 100		RES,CF,1.2M,+-5%,0.25W	866728	59124	CF1-4 VT 125 J B	1	
R 102		RES,VAR,CERM,200,+-20%,0.5W	226050	80294	3329H-1-201	1	
R 103,144		RES,MF,887,+-1%,0.125W,100PPM	866652	59124	MF50DVT8870F REEL	2	
R 104		RES,VAR,CERM,200,+-10%,0.5W	275743	80294	3386R-1-201	1	
R 105		RES,MF,2.15K,+-1%,0.125W,100PPM	866699	59124	MF50DVT2151F REEL	1	
R 106,109,135,		RES,CF,470,+-5%,0.25W	854567	59124	CF1-4 VT 471 J B	4	
R 136			854567				
R 114		RES,MF,3.01K,+-1%,0.125W,100PPM	866694	59124	MF50DVT3011F REEL	1	
R 115		RES,VAR,CERM,5K,+-20%,0.5W	226084	80294	3329H-1-502	1	
R 116		RES,CF,82K,+-5%,0.25W	655027	59124	CF1-4 VT 823 J B	1	
R 118		RES,MF,15K,+-1%,0.125W,100PPM	866702	59124	MF50DVT1502F REEL	1	
R 120		RES,MF,549,+-1%,0.125W,100PPM	820332	59124	MF50DVT5490F REEL	1	
R 122		RES,CC,100,+-10%,0.25W	193185	01121	CB1011	1	
R 124,142		RES,CF,330K,+-5%,0.25W	866707	59124	CF1-4 VT 334 J B	2	
R 126		RES,MF,49.9,+-1%,0.125W,100PPM	820266	59124	MF50DVT49R9F REEL	1	
R 129,131,132		RES,CF,200,+-5%,0.25W	573055	59124	CF1-4 201 J B	3	
R 133		RES,MF,499,+-1%,0.125W,100PPM	816462	91637	CMF55 4990 F T-1	1	
R 134		RES,MF,604,+-1%,0.125W,100PPM	832030	91637	CMF55 6040 F T-1	1	
R 138		RES,CF,3K,+-5%,0.25W	810366	59124	CF1-4 VT 302 J B	1	
R 139,141		RES,VAR,CERM,100,+-10%,0.5W	275735	80294	3386R-1-101	2	
R 140		RES,VAR,CERM,500,+-10%,0.5W	325613	80294	3386R-1-501	1	
R 145		RES,VAR,CERM,2K,+-20%,0.5W	226076	80294	3329H-1-202	1	
R 147		RES,MF,665,+-1%,.125W,100PPM	875398	59124	MF1-8VT 6650 F REEL	1	
R 148		RES,VAR,CERM,200K,+-20%,0.3W	757245	80294	3362U-1-204R	1	
R 149		RES,MF,200K,+-1%,0.125W,100PPM	719831	91637	CMF55 2003 F T-1	1	
RT 1		THERMISTOR,DISC,NEG.,10K,+-10%,25C	104596	15801	140-103LAG-A01	1	
TP 1, 2, 4,		JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	8	
TP 5, 8- 10,			816090				
TP 15			816090				
TP 3, 6, 7,		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	5	
TP 11, 12			512889				
U 1- 3	*	IC,BPLR,MONOLITHIC UWAVE AMP,SEL GAIN	867049	28480	QPMA-0385	3	
U 4	*	IC,ECL,DUAL D M/S F/F,W/SET&RESET	454959	04713	MC10131P	1	
U 5	*	IC,OP AMP,QUAD,LOW NOISE	851829	06665	OP470FY	1	
U 6	*	IC,ALSTTL,HEX INVERTERS	837716	01295	SN74ALS04BN	1	
U 7, 12, 19	*	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	3	
U 8, 22, 51	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LSOON	3	
U 9, 14	*	IC,LSTTL,DUAL DIV BY 2,DIV BY 5 CNTR	483594	01295	SN74LS390N	2	
U 10, 16, 17	*	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	3	
U 11	*	IC,LSTTL,SYNC DIVIDE BY 16 BIN CNTR	393231	01295	SN74LS193N	1	
U 13, 49	*	IC,FTTL,DUAL 4-INPUT MULTIPLEXER	659912	04713	MC74F153N	2	
U 15	*	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	04713	SN74LS27N	1	
U 18	*	IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LSO2N	1	
U 20	*	IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	412734	01295	SN74LS122N	1	
U 21	*	IC,FTTL,DUAL D F/F,+EDG TRG,W/CL&SET	659508	04713	MC74F74N	1	
U 23	*	IC,BPLR 10BIT DAC,10BIT ACCUR,CUR OUT	477760	24355	AD561D	1	
U 24	*	IC,CMOS,DUAL SPDT ANALOG SWITCH	853598	17856	DG303ACJ	1	
U 25	*	IC,OP AMP,LO-NOISE,PLASTIC DIP	854216	06665	OP27GP	1	
U 27	*	IC,COMPARATOR,GENERAL PURPOSE,DIP	845065	64155	LT1011ACN8	1	
U 29	*	IC,16V8,LOG ARRAY,6080A-90203	855056	12040	855056	1	
U 30	*	IC,CMOS,3-8 LINE DCDR W/ENABLE	773036	01295	SN74HC138N	1	

An * in 'S' column indicates a static-sensitive part.

Table 8-14. A14 FM PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	NOTE
U	32	*	IC,CMOS,8-1 LINE MUX/DEMUX ANALOG SW	836304	04713	MM74HC4051N	1	
U	33	*	IC,16V8,LOG ARRAY,6080A-90204	855143	12040	855143	1	
U	35	*	IC,CMOS,QUAD SPST ANALOG SWITCH	620948	24355	ADG201AKN	1	
U	36, 39, 43,	*	IC,DMOS,FET QUAD SWITCH	507228	17856	SSD500203	4	
U	47	*		507228				
U	37, 45, 46	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	3	
U	38	*	IC,OP AMP,DUAL,LOW NOISE,LOW CURRENT	855130	06665	OP270FZ	1	
U	40, 41	*	IC,OP AMP,PRECISION,LOW NOISE	816744	06665	OP-37GP	2	
U	42	*	IC,BPLR,ANALOG MULTIPLIER	845151	24355	AD42020-1	1	
U	44	*	IC,FTTL,HEX INVERTER	634444	04713	MC74F04N	1	
U	48	*	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	
U	50	*	IC,OP AMP,LO-NOISE,8 PIN DIP	477745	18324	NE5534AN	1	
Z	1		RES,CERM,SIP,6 PIN,5 RES,4.7K,+-2%	494690	91637	CSC06A-01-472G	1	
Z	2		RES,CERM,SIP,10 PIN,9 RES,100K,+-2%	461038	91637	CSC10A-01-104G	1	
Z	3		RES,CERM,SIP,6 PIN,5 RES,100K,+-2%	412726	91637	CSC06A-03-104G	1	
Z	4		RES,CERM,SIP,6 PIN,5 RES,510,+-2%	459974	91637	CSC06A-01-511G	1	
Z	5		RES NET THK FILM TESTED	858378	89536	858378	1	
Z	6		RES NET THK FILM TESTED	851118	89536	851118	1	
Z	7		RES NET THK FILM TESTED	851170	89536	851170	1	
Z	8		RES,CERM,SIP,10 PIN,9 RES,4.7K,+-2%	484063	91637	CSC10A-01-472G	1	

An * in 'S' column indicates a static-sensitive part.



6082A-1645

Figure 8-14. A14 fm PCA

Table 8-15. A15 Power Supply PCA
(See Figure 8-15.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	NOTE
C	1		CAP,AL,1000UF,+-20%,50V,SOLV PROOF	782391	62643	KME50VB102M16X25LL	1	
C	2, 3		CAP,AL,22000UF,+-20%,10V,SOLV PROOF	844725	62643	KME10VR223M35X30TV4	2	
C	4, 10, 17,		CAP,TA,4.7UF,+-20%,50V	832675	56289	199D475X0050DG2	9	
C	22, 24, 29,			832675				
C	32, 43, 47			832675				
C	5		CAP,AL,18000UF,+-20%,25V,SOLV PROOF	867937	62643	KME25VR183M35X40TV4	1	
C	6		CAP,AL,10000UF,+30-10%,35V,SOLV PROOF	614990	62643	KME35VN103K31X42LLV	1	
C	7		CAP,AL,470UF,+30-10%,80V,SOLV PROOF	574160	62643	KME80VN471K23X27LLV	1	
C	8, 13, 18,		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	10	
C	21, 23, 30,			837526				
C	41, 42, 44,			837526				
C	53			837526				
C	9, 28		CAP,TA,4.7UF,+-20%,25V	807644	56289	199D475X0025BG2	2	
C	11, 12, 19,		CAP,POLYES,0.22UF,+-10%,100V	436113	68919	MKS4224K100V	5	
C	26, 27			436113				
C	14, 40		CAP,AL,220UF,+50-20%,35V	460279	62643	SM35VB221M10X20FTV	2	
C	15		CAP,TA,220UF,+-20%,6V	408682	56289	199D227X006FA2	1	
C	16, 25		CAP,TA,22UF,+-20%,25V	357780	56289	199D220X0025DES	2	
C	20, 38		CAP,CER,470PF,+-10%,1000V,Z5F	368613	60705	562C0B0CK102EC471K	2	
C	31, 48		CAP,TA,10UF,+-20%,35V	417683	56289	199D106X0035DA2	2	
C	33, 34		CAP,TA,2.2UF,+-10%,35V	697433	56289	199D225X9035BG2	2	
C	35		CAP,TA,6.8UF,+-20%,35V	807602	56289	199D685X0035DG2	1	
C	36, 37, 50,		CAP,CER,1000PF,+-20%,100V,X7R	816181	04222	SR071C102MAATR1A	4	
C	51			816181				
C	39		CAP,CER,68PF,+-10%,1000V,S3N	706812	60705	561CR3LRE102EE680K	1	
C	46		CAP,CER,1800PF,+-5%,50V,C0G	528547	04222	SR215A182JAT	1	
C	49		CAP,AL,470UF,+-20%,50V,SOLV PROOF	747493	62643	KMC50VB471M16X25LLV	1	
CR	1, 13		DIODE,SI,RECT,BRIDGE,BV=200V,IO=1.5A	296509	30800	KBP 02M	2	
CR	2, 3	*	ZENER,UNCOMP,24.0V,5%,5.2MA,0.4W	267807	04713	1N970B	2	
CR	4, 8		DIODE,SI,45PIV,7.5A,DUAL SCHOTTKY	741322	04713	MBR1545CT	2	
CR	5, 9, 15	*	ZENER,UNCOMP,6.2V,5%,20.0MA,0.4W	698662	04713	1N753A-SR4348RL	3	
CR	6, 7, 12,		DIODE,SI,100 PIV,1.5 AMP	116111	04713	1N5392	4	
CR	14			116111				
CR	10	*	ZENER,UNCOMP,20.0V,5%, 6.2MA,0.4W	810275	65940	1N968BT-88	1	
CR	11	*	ZENER,UNCOMP,20.0V,5%,6.2MA,0.4W	832576	04713	1N968B	1	
CR	16	*	ZENER,COMP,6.3V,2%,50 PPM,7.5MA	172148	04713	CZG20121RL	1	
CR	17	*	ZENER,UNCOMP,3.3V,5%,20.0MA,0.4W	820423	04713	1N746ARR1	1	
CR	20	*	ZENER,UNCOMP,6.8V,10%,175.0MA,5.0W	483446	04713	1N5342B	1	
CR	21	*	DIODE,SI,BV= 75.0V,RADIAL INSERTED	659516	03508	1N4448	1	
H	1- 4, 14		WASHER,SHLDR,NYLON,.113,.245	485417	86928	5607-50	5	
H	5, 6, 13		NUT,LOCK,SS,4-40	558866	COMMERCIAL		3	
H	7, 10, 11,		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		4	
H	15			772236				
H	8, 9		SCREW,PH,P,STL,LOCK,4-40,.500	740761	COMMERCIAL		2	
H	12		SCREW,PH,P,STL,LOCK,4-40,.375	740753	COMMERCIAL		1	
H	16		NUT,PRESS,BROACH,STL,6-32	393785	24347	KF2-632ZC	1	
J	1		HEADER,1 ROW,.156CTR,12 PIN	512160	27264	09-80-1123	1	
J	2		HEADER,1 ROW,.156CTR,5 PIN	512186	27264	09-80-1053	1	
J	3, 4		HEADER,1 ROW,.100CTR,RT ANG,15 PIN	854807	00779	1-641216-5	2	
J	7		HEADER,1 ROW,.100CTR,2 PIN	602698	00779	640456-2	1	
MP	1, 3		HEAT DIS,PWB MTG,1.380,2.000,.500	386235	13103	6032D.380-2.000-.500	2	
MP	2		HEAT DIS,VERT,1.65X1.00X1.50,TO-220	853759	13103	6298B-2-P3-G5-1/BAG	1	
MP	4, 5		INSUL PART,POWER,SI,.750,.500	534453	55285	7403-09FR-54	2	
MP	7, 8		HEAT DIS,VERT,1.65X1.00X1.50,TO-220	853754	13103	6398B-P3-CNE62-GF-1/BAG	2	
MP	9		HEAT DIS,HORIZ,1.860X1.062X.50,TO-3	740738	91502	7-423BA	1	
MP	10, 11		SPACER,SWAGED,.250 RND,BR,6-32,.187	351882	9W423	9533B-B-0632	2	
MP	13- 30		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	18	
MP	31		POWER SUPPLY SHIELD	879205	89356	879205	1	1
Q	1, 2	*	TRANSISTOR,SI,NMOS,PWR FET,TO-220	831255	61752	1RC530-007	2	
Q	3	*	THYRISTOR,SI,TRIAC,VBO=200V,8.0A	413013	04713	T2800B	1	
Q	4	*	THYRISTOR,SI,SCR,VBO=100V,0.8A	742643	04713	2N5062	1	
Q	5	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	816298	04713	MPS8099RLRA	1	
R	1		RES,CF,220,+-5%,0.25W	342626	59124	CF1-4 221 J B	1	
R	2		RES,CC,6.8K,+-10%,0.5W	108399	01121	EB6821	1	
R	3		RES,CC,820,+-5%,0.25W	148015	01121	CB8215	1	
R	4		RES,CC,22K,+-5%,0.25W	148130	01121	CB2235	1	
R	5		RES,CC,43K,+-5%,0.25W	193367	01121	CB4335	1	
R	6		RES,MF,47.5,+-1%,0.125W,100PPM	306076	91637	CMF55 47R5 F T-1	1	

An * in 'S' column indicates a static-sensitive part.

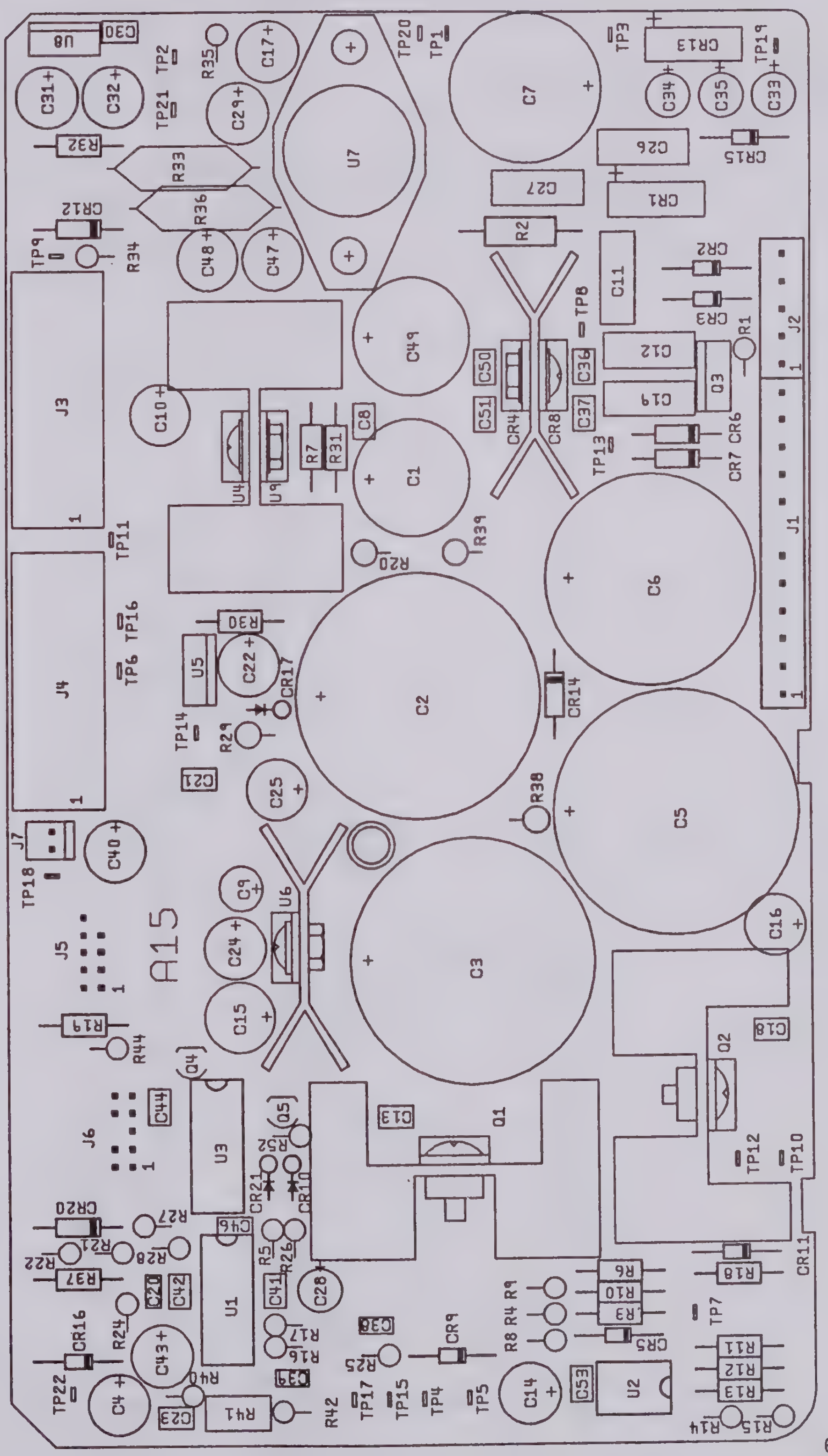
Table 8-15. A15 Power Supply PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
R	7		RES,MF,267,+-1%,0.125W,100PPM	866223	91637	CMF55 2670 F T-1	1	
R	8, 9, 14,		RES,MF,4.75K,+-1%,0.125W,100PPM	720276	91637	CMF55 4751 F T-1	5	
R	15, 31			720276				
R	10- 13		RES,MF,221K,+-1%,0.125W,25PPM	706465	91637	CMF55 2213 F T-9	4	
R	16		RES,MF,4.42K,+-1%,0.125W,100PPM	288514	91637	CMF55 4421 F T-1	1	
R	17, 25		RES,MF,2.21K,+-1%,0.125W,100PPM	347476	91637	CMF55 2211 F T-1	2	
R	18		RES,MF,57.6,+-1%,0.125W,100PPM	305946	91637	CMF55 57R6 F T-1	1	
R	19		RES,MF,66.5K,+-1%,0.125W,100PPM	866322	91637	CMF55 6652 F T-1	1	
R	20		RES,CC,2.4K,+-5%,0.5W	108902	01121	EB2425	1	
R	21, 34, 44		RES,CF,10K,+-5%,0.25W	697102	59124	CF1-4 VT 103 J B	3	
R	22, 28, 42		RES,MF,22.1K,+-1%,0.125W,100PPM	719898	91637	CMF55 2212 F T-1	3	
R	24		RES,CC,3K,+-5%,0.25W	193508	01121	CB3025	1	
R	26		RES,MF,732,+-1%,0.125W,100PPM	720508	91637	CMF55 7320 F T-1	1	
R	27		RES,MF,442,+-1%,0.125W,100PPM	340802	91637	CMF55 4420 F T-1	1	
R	29		RES,CC,100,+-10%,0.5W	108100	01121	EB1011	1	
R	30		RES,CF,1,+-5%,0.25W	572883	59124	CF1-4 1R0 J B	1	
R	32		RES,MF,115,+-1%,0.125W,100PPM	866186	91637	CMF55 1150 F T-1	1	
R	33		RES,MF,2.67K,+-1%,0.5W,100PPM	161430	91637	CMF65 2671 F T-1	1	
R	35		RES,MF,127,+-1%,0.125W,100PPM	866199	91637	CMF55 1270 F T-1	1	
R	36		RES,MF,3.65K,+-1%,0.5W,100PPM	247650	91637	CMF65 3651 F T-1	1	
R	37		RES,CC,2.4K,+-5%,0.25W	193433	01121	CB2425	1	
R	38, 39		RES,CC,1K,+-5%,0.5W	108597	01121	EB1025	2	
R	40		RES,MF,4.02K,+-1%,.125W,25PPM	851480	91637	CMF55 4021 F T-9	1	
R	41		RES,VAR,CERM,5K,+-10%,0.5W	355503	80294	3386W-W91-502	1	
R	52		RES,CF,20K,+-5%,0.25W	697110	59124	CF1-4 VT 203 J B	1	
TP	1- 22		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	22	
U	1	*	IC,OP AMP,QUAD,HIGH SPEED,LOW NOISE	845016	06665	OP471FY	1	
U	2	*	IC,OP AMP,SELECTED GBW 600KHZ	418566	18324	LM358	1	
U	3	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	1	
U	4	*	IC,VOLT REG,FIXED,+24 VOLTS,1.5 AMPS	604074	04713	MC7824CT	1	
U	5	*	IC,VOLT REG,FIXED,-5 VOLTS,1.5 AMPS	394551	04713	MC7905CT	1	
U	6	*	IC,VOLT REG,FIXED,-15 VOLTS,1.5 AMPS	413179	04713	MC7915CT	1	
U	7	*	IC,VOLT REG,HIGH VOLTAGE	723353	27014	LM317HVK	1	
U	8, 9	*	IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	27014	LM317T	2	

An * in 'S' column indicates a static-sensitive part.

NOTES:

NOTE 1 = Includes H1-H5. SPACER,BROACH,RND,SS,.143ID,.250 484865 24347 KFSE-.143-8 5


A15
U8
C30
C31
C32
TP2
TP21
R35
C17
C29
U7
TP20
TP1
C7
TP3
CR13
TP19
C34
C35
C33
R32
R33
R36
CR12
TP9
R34
C48
C47
C26
CR15
C27
CR1
R2
C11
CR2
CR3
R1
J2
TP8
C49
C50
C36
C12
Q3
C10
J3
C51
CR4
CR8
C37
C19
CR6
CR7
TP13
U4
U9
R7
R31
C8
C1
R39
R20
TP11
J1
C6
TP16
TP6
J4
R30
U5
C22
CR17
C2
CR14
TP14
R29
C21
C25
R38
C5
J7
TP18
C40
C9
U6
J5
C24
C16
C3
C15
R19
R44
Q4
C18
Q2
C44
J6
U3
Q5
R52
C13
Q1
TP12
TP10
CR20
R27
CR21
CR10
C46
R21
R28
R22
R37
R5
R26
R6
C20
C42
U1
C41
C28
R8
R4
R9
R10
R3
R18
CR11
CR16
R24
C43
R17
R16
C38
CR9
CR5
TP7
R11
R12
R13
R40
R25
C39
TP22
C4
C23
R41
R42
TP17
TP15
TP4
TP5
C14
C53
U2
R14
R15

6082A-1670

Figure 8-15. A15 Power Supply PCA

Table 8-16. A16 IEEE-488 Connector PCA
(See Figure 8-16.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
H 3, 4		SPACER,SWAGED/BROACH,RND,BR,6-32,.187	854666	55566	7332B-632-B-14	2	
J 2		CONN,MICRO-RIBBON,REC,PWB,24 POS	851675	52500	57-20240-23	1	
J 3		CONN,D-SUB,PWB,9 SCKT	811430	00779	747150-8	1	
MP 1- 34		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	34	
S 1, 2		SWITCH,SLIDE,SPDT,LOW PROFILE	810887	95146	SSB-12	2	
S 3		SWITCH,SLIDE,DPDT	452862	79727	GS113-(0018)-G20-32	1	

An * in 'S' column indicates a static-sensitive part.

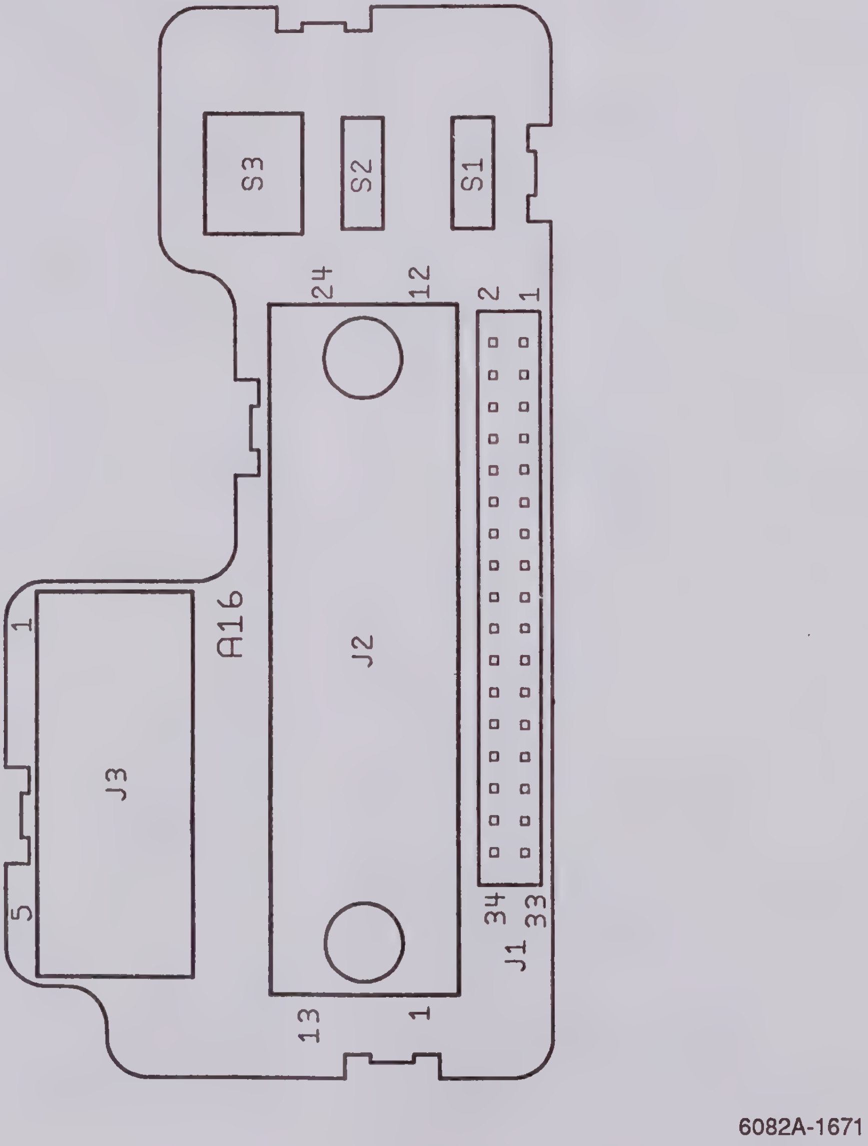


Figure 8-16. A16 IEEE-488 Connector PCA

Table 8-17. A19 Switch PCA
(See Figure 8-17.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
DT 1, 2	*	ISOLATOR,OPTO,OPTICAL SWITCH,INFRARED	523530	09214	H22A1	2	
MP 1		SOCKET,1 ROW,PWB,0.100CTR,16 POS	447102	30035	SS-109-1-16	1	
MP 2		SOCKET,1 ROW,PWB,0.100CTR,7 POS	520809	30035	SS-109-1-07	1	
MP 3		HEADER,1 ROW,.100CTR,RT ANG,36 PIN	563403	22526	65524-136	1	

An * in 'S' column indicates a static-sensitive part.

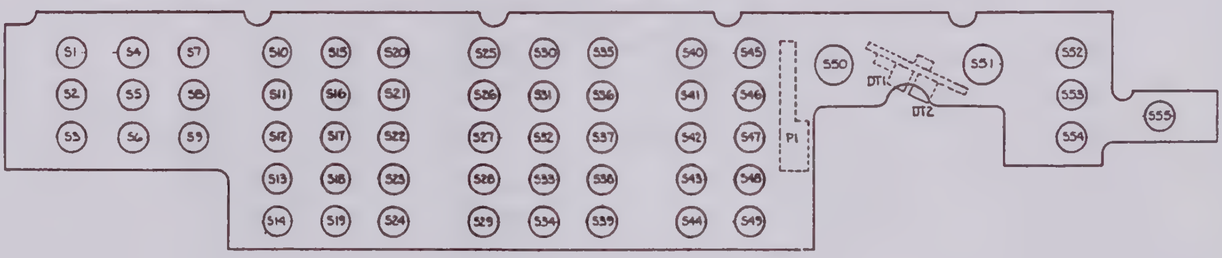

S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
S36
S37
S38
S39
S40
S41
S42
S43
S44
S45
S46
S47
S48
S49
P1
S50
DT1
DT2
S51
S52
S53
S54
S55
6080A-1651

Figure 8-17. A19 Switch PCA

Table 8-18. A20 Attenuator/RPP Assembly
(See Figure 8-18.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	----DESCRIPTION----	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
A 7	*	RELAY DRIVER PCA	882022	89536	882022	1	
A 21	*	ATTENUATOR PCA				1	1
H 301-309		SCREW,PH,P,MAG,SS,LOCK,6-32,.375	783225	COMMERCIAL		9	
MP 1	*	ATTENUATOR HOUSING, FILTER ASSY	868948	89536	868948	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

NOTE 1 = A21 can not be replaced separately. Order entire A20 assembly Fluke P/N 860812.

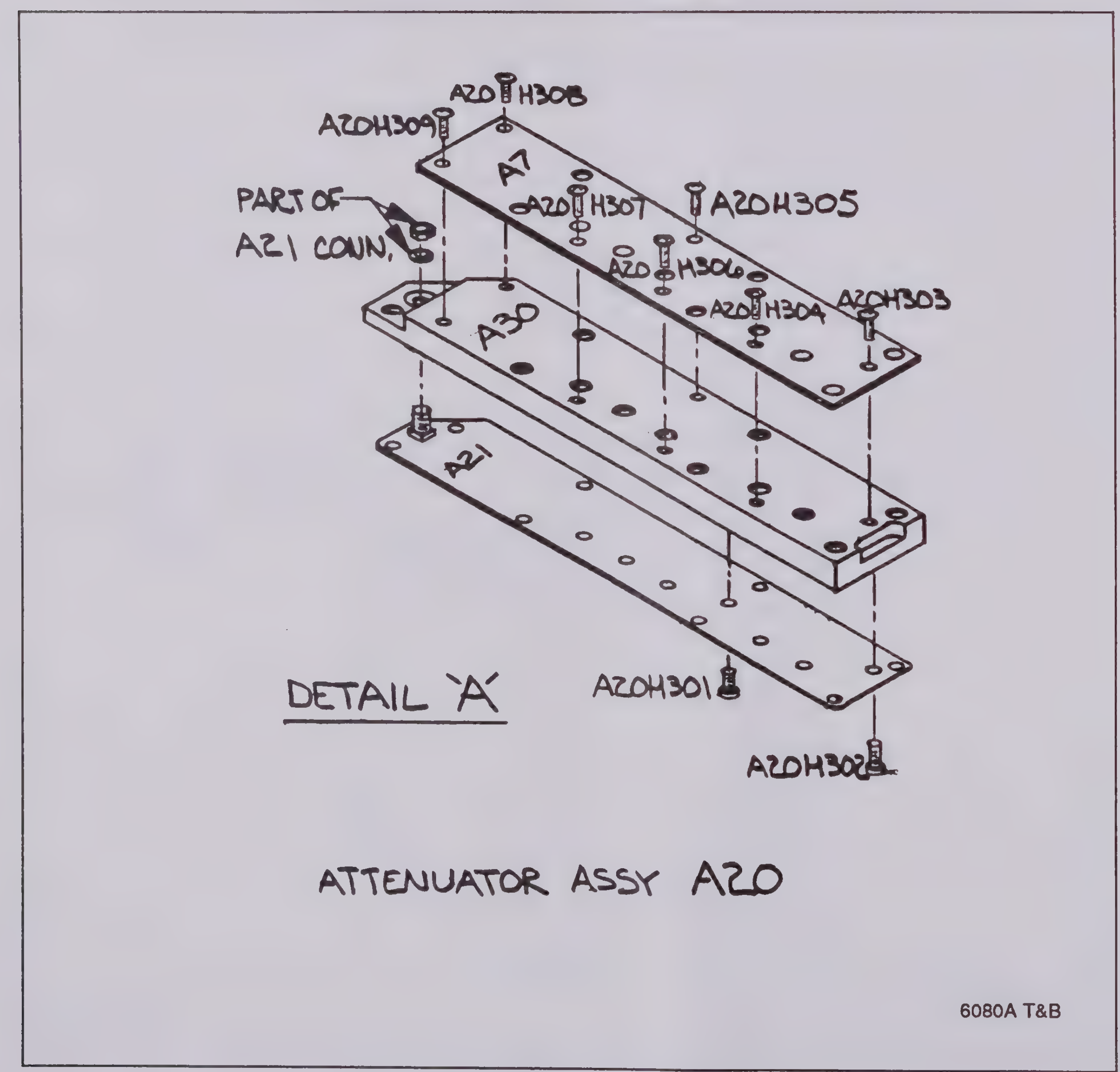
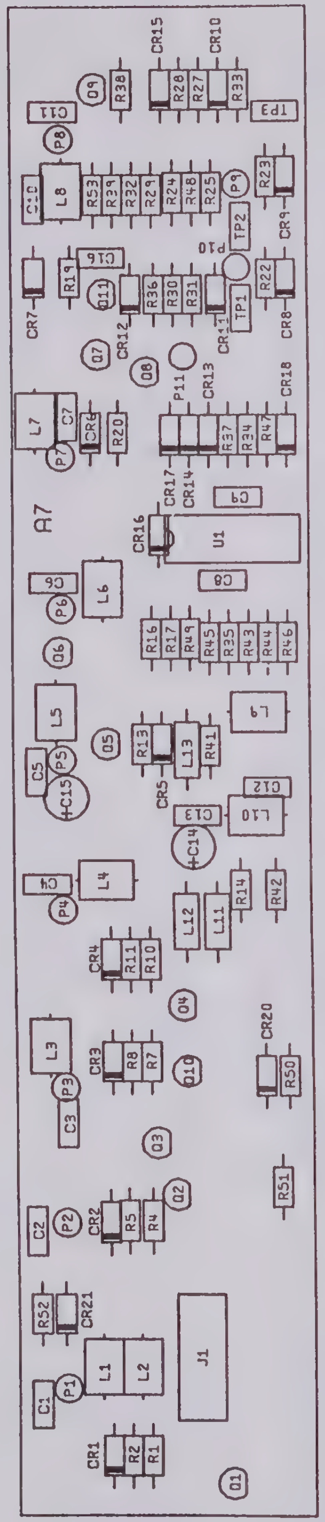

A20 H308
A20H309
A7
PART OF A21 CONN.
A20 H307
A20H305
A20 H306
A20 H304
A20H303
A30
A21
DETAIL 'A'
A20H301
A20H302
ATTENUATOR ASSY A20
6080A T&B

Figure 8-18. A20 Attenuator/ RPP Assembly PCA

Table 8-19. A20A7 Relay Driver PCA
(See Figure 8-19.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	NOTE -E-
C	1- 7, 11		CAP,POLYES,0.1UF,+-20%,50V	837526	40402	MKT1823 104 05 6	8	
C	8, 9, 12,		CAP,CER,0.01UF,+-20%,50V,X7R	816249	04222	SR075C103MAATR1A	4	
C	13			816249				
C	10, 16		CAP,CER,0.22UF,+-20%,50V,Z5U	831982	04222	SR295E224MAATR1A	2	
C	14		CAP,AL,22UF,+-20%,35V,SOLV PROOF	851766	62643	KRE35VB22RM6X5RP	1	
C	15		CAP,AL,4.7UF,+-20%,50V,SOLV PROOF	851774	62643	KRE50VB4R7M5X5RP	1	
CR	1- 7, 15	*	ZENER,UNCOMP,30.0V,10%,4.2MA,0.4W	272633	04713	1N972A	8	
CR	8, 9	*	ZENER,UNCOMP,7.5V,5%,20.0MA,0.4W	698688	04713	1N755A-SR4348RL	2	
CR	10	*	ZENER,UNCOMP,9.1V,5%,14.0MA,0.4W	386557	04713	1N960B	1	
CR	11- 14, 16,	*	DIODE,SI,BV= 75.0V,IO=150MA,500MW	698720	65940	1N4448	8	
CR	17, 20, 21	*		698720				
CR	18	*	ZENER,UNCOMP,4.7V,5%,20.0MA,0.4W	524058	04713	1N750A	1	
H	1- 7		SPACER,SWAGE,.250 RND,BR,.150ID,.150	631861	9W423	9L505-B-0256	7	
J	1		HEADER,2 ROW,.100CTR,RT ANG,16 PIN	417030	00779	87230-8	1	
L	1- 10		CHOKE,6TURN	320911	89536	320911	10	
L	11		INDUCTOR,82UH,+-10%,14MHZ,SHLD	542290	24759	MR-82	1	
L	12, 13		INDUCTOR,47UH,+-5%,26.5MHZ,SHLD	147850	24759	MR-47	2	
P	1- 11		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	866764	00779	645991-3	11	
Q	1- 7, 9	*	TRANSISTOR,SI,PNP,TO92	698290	04713	MPS6562RLRA	8	
Q	8, 10, 11	*	TRANS,SI,NPN,SELECTED IEBO,SMALL SIG	685404	04713	SPS8763RLRA	3	
R	1, 4, 7,		RES,CF,510,+-5%,0.25W	573139	59124	CF1-4 511 J B	8	
R	10, 13, 16,			573139				
R	19, 38			573139				
R	2, 5, 8,		RES,CF,4.7K,+-5%,0.25W	573311	59124	CF1-4 472 J B	9	
R	11, 14, 17,			573311				
R	20, 39, 41			573311				
R	22, 23		RES,CF,750,+-5%,0.25W	573162	59124	CF1-4 751 J B	2	
R	24		RES,CF,30K,+-5%,0.25W	574251	59124	CF1-4 303 J B	1	
R	25, 30, 31,		RES,CF,10K,+-5%,0.25W	573394	59124	CF1-4 103 J B	5	
R	37, 49			573394				
R	27, 28		RES,MF,422,+-1%,0.125W,100PPM	720235	91637	CMF55 4220 F T-1	2	
R	29, 35, 36,		RES,CF,1K,+-5%,0.25W	573170	59124	CF1-4 102 J B	5	
R	42, 45			573170				
R	32		RES,MF,1.5K,+-1%,0.125W,100PPM	719682	91637	CMF55 1501 F T-1	1	
R	33		RES,CF,56,+-5%,0.25W	641068	59124	CF1-4 560 J B	1	
R	34		RES,CF,100K,+-5%,0.25W	573584	59124	CF1-4 104 J B	1	
R	43		RES,CF,13K,+-5%,0.25W	573410	59124	CF1-4 133 J B	1	
R	44, 51- 53		RES,CF,2K,+-5%,0.25W	573238	59124	CF1-4 202 J B	4	
R	46		RES,CF,470,+-5%,0.25W	573121	59124	CF1-4 471 J B	1	
R	47		RES,CF,12K,+-5%,0.25W	573402	59124	CF1-4 123 J B	1	
R	48		RES,CF,4.3K,+-5%,0.25W	641100	59124	CF1-4 432 J B	1	
R	50		RES,CF,5.1K,+-5%,0.25W	573329	59124	CF1-4 512 J B	1	
TP	1		HEADER,1 ROW,.100CTR,6 PIN	478669	00779	103747-6	1	
U	1	*	IC,OP AMP,QUAD,JFET INPUT,14 PIN DIP	483438	01295	TL084CN	1	

An * in 'S' column indicates a static-sensitive part.


CR15
CR10
Q9
R38
R28
R27
R33
C11
TP3
P8
C10
L8
R53
R39
R32
R29
R24
R48
R25
P9
R23
CR9
TP2
P10
C16
R19
CR7
Q11
CR12
R36
R30
R31
CR11
TP1
R22
CR8
Q7
Q8
P11
CR13
CR18
L7
C7
CR6
R20
P7
R37
R34
R47
CR17
CR14
C9
A7
CR16
U1
C6
L6
C8
P6
R16
R17
R49
R45
R35
R43
R44
R46
Q6
L5
L9
Q5
R13
L13
R41
C5
P5
C15
C12
CR5
C13
L10
C14
C4
L4
P4
R14
R42
L12
L11
CR4
R11
R10
Q4
CR20
L3
CR3
R8
R7
Q10
R50
P3
C3
Q3
R51
Q2
C2
P2
CR2
R5
R4
R52
CR21
J1
L1
L2
P1
C1
CR1
R2
R1
Q1

6082A-1632

Figure 8-19. A20A7 Relay Driver PCA

Table 8-20. A20A21 Attenuator PCA
(See Figure 8-20.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	N O T -E-
C	1, 2, 4		CAP,CER,1000PF,+-20%,50V,X7R,0805	514059	04222	08055C102MAT060B	3	
C	3, 5		CAP,TA,4.7UF,+-10%,15V	519363	56289	193D475X9015C2	2	
C	6, 7		CAP,TA,3.3UF,+-20%,50V	772848	56289	195D335X00200E2B	2	
CR	1	*	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNL	535195	28480	5082-2800	1	
CR	2- 9	*	DIODE,SI,BV= 70.0V,500 MW	454181	07263	1N4606	8	
H	1- 8		RELAY WASHER	803247	89536	803247	8	
J	1		SOCKET,SINGLE,PWB,FOR 0.034-0.037 PIN	732826	00779	2-332070-7	1	
J	2		CONN,COAX,SMA(M),PWB OR PANEL	512087	21845	2985-6011	1	
K	1- 8		RELAY, SCREENED, HIGH FREQUENCY	812669	89536	812669	8	
P	1- 11		SOCKET,SINGLE,PWB,FOR .042-.049 PIN	544056	00779	50871-1	11	
R	1, 4, 7,		RES,MF,402,+-0.5%,0.125W,50PPM	461632	03888	PME60ASAP04	5	
R	10, 19			461632				
R	2, 3, 5,		RES,MF,56.9,+-0.5%,0.125W,50PPM	461590	03888	PME60A3AP04	10	
R	6, 8, 9,			461590				
R	11, 12, 20,			461590				
R	21			461590				
R	13		RES,MF,37.4,+-0.5%,0.125W,50PPM	461079	64537	PME60-A3AP04	1	
R	14, 15		RES,MF,150,+-0.5%,0.125W,50PPM	461624	64537	PME60A3AP04	2	
R	16		RES,MF,94.2,+-0.5%,0.125W,50PPM	461616	64537	PME60A3AP04	1	
R	17, 18		RES,MF,83.5,+-0.5%,0.125W,50PPM	461608	64537	PME60A3AP04	2	
R	22		RES,MF,10K,+-1%,0.25W,100PPM	799635	91637	CCF-501002F	1	
R	23		RES,CF,51,+-5%,0.25W	572990	59124	CF1-4 510 J B	1	

An * in 'S' column indicates a static-sensitive part.

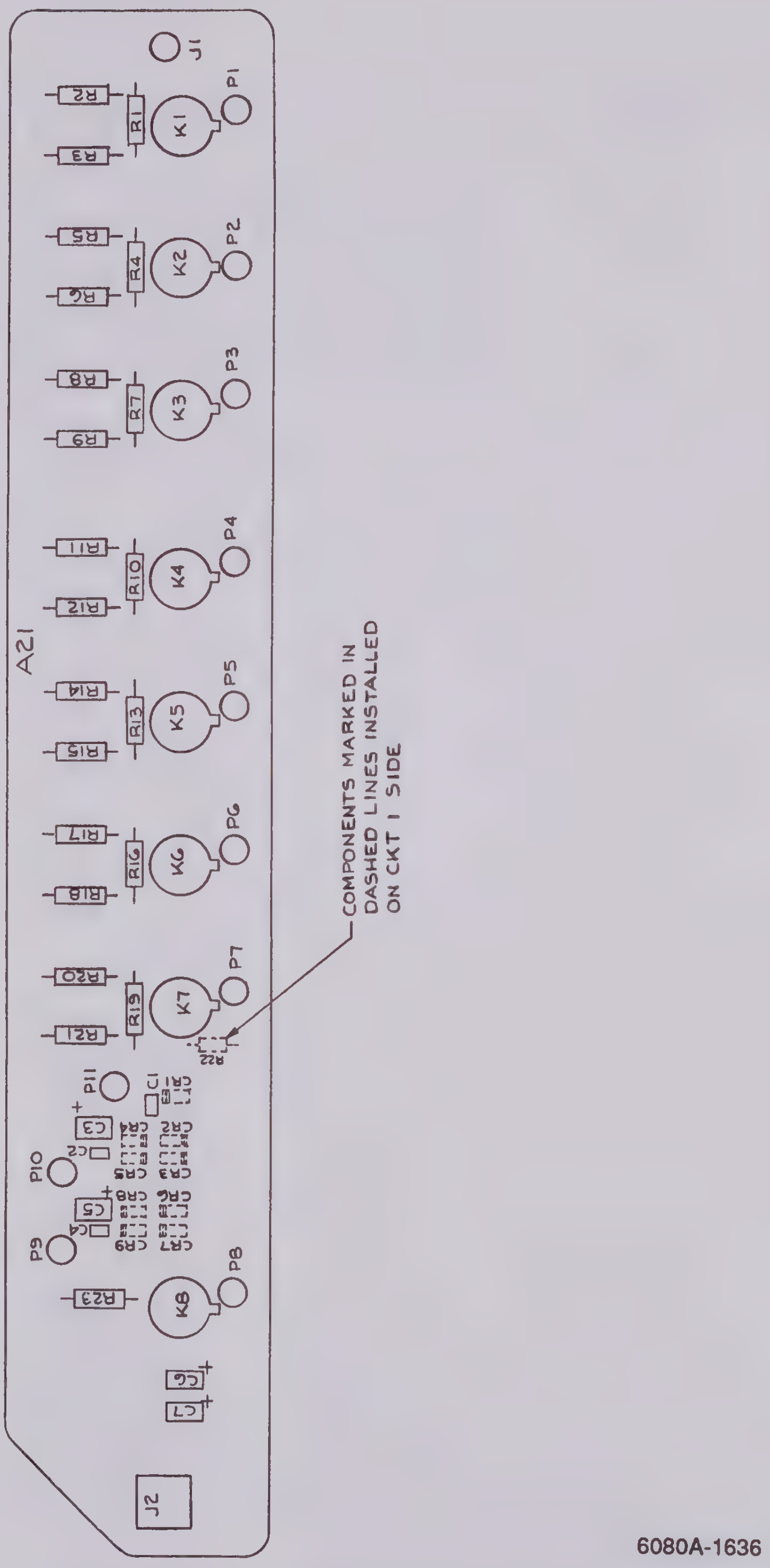
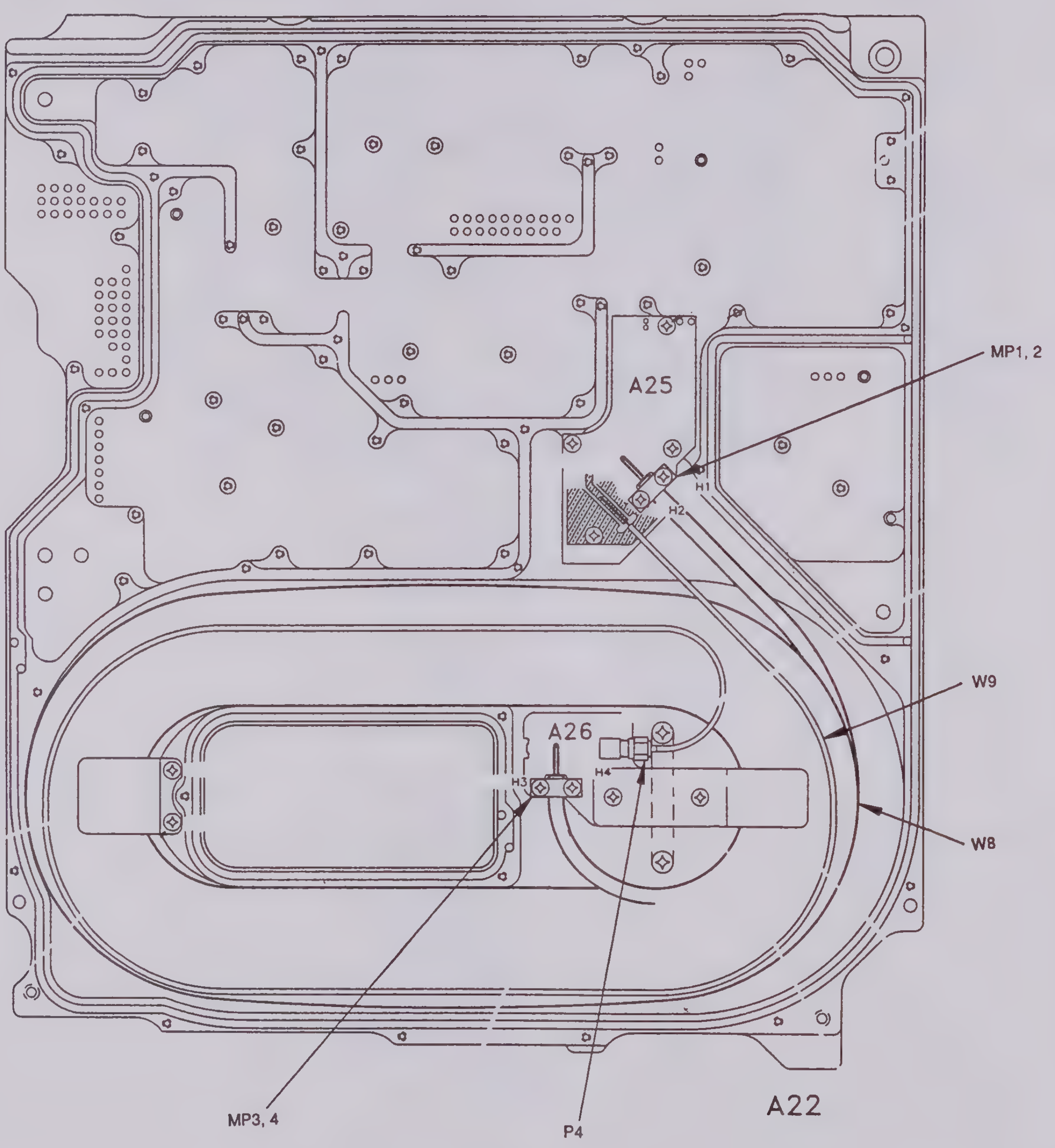

A21
J1
P1
R2
R1
K1
R3
P2
R5
R4
K2
R6
P3
R8
R7
K3
R9
P4
R11
R10
K4
R12
P5
R14
R13
K5
R15
P6
R17
R16
K6
R18
P7
R20
R19
K7
R21
R22
COMPONENTS MARKED IN DASHED LINES INSTALLED ON CKT 1 SIDE
P11
C1
CR1
C3
CR4
CR2
C2
CR5
CR3
P10
C5
CR8
CR6
C4
CR9
CR7
P9
P8
R23
K8
C6
C7
J2
6080A-1636

Figure 8-20. A20A21 Attenuator PCA

Table 8-21. A22 Delay Line Assembly
(See Figure 8-21.)

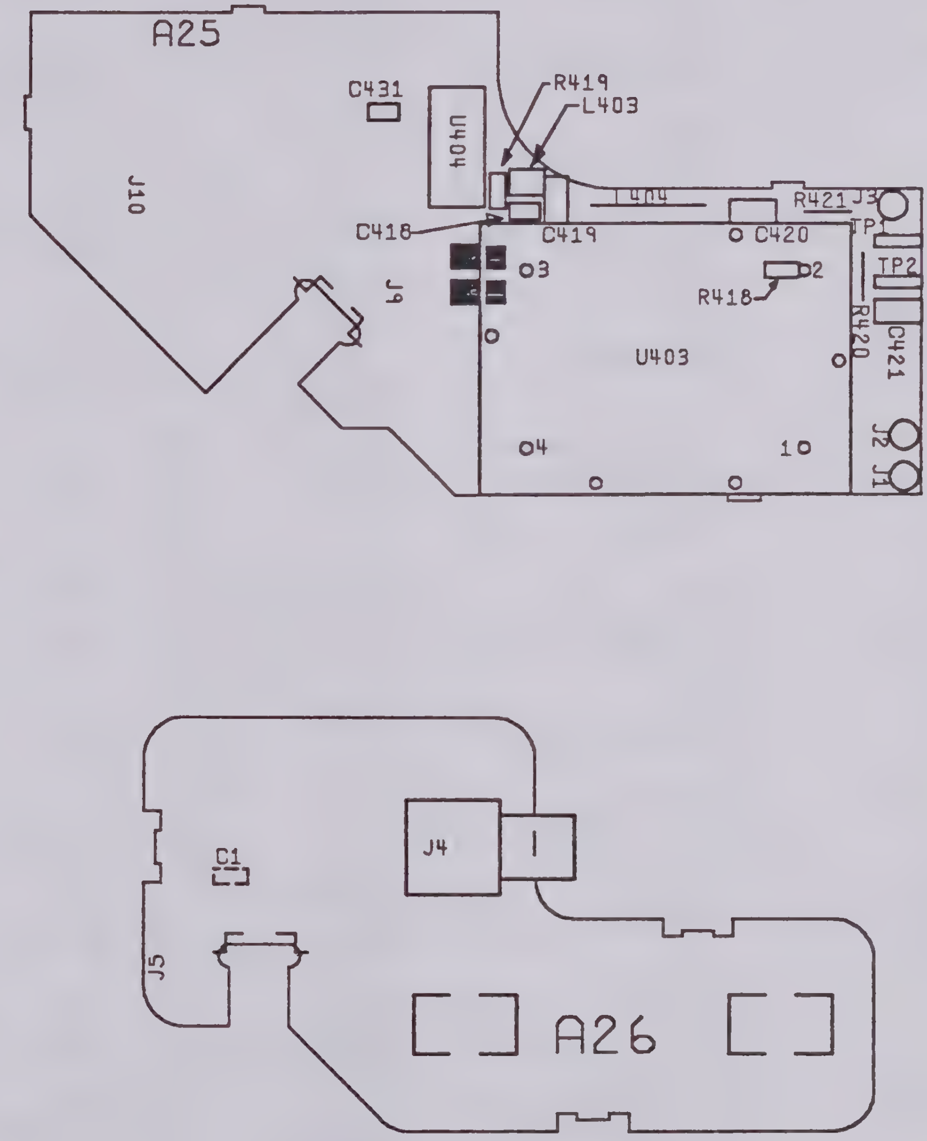
REFERENCE DESIGNATOR -A>	NUMERICS	S	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTE
C	1		CAP,PORC,0.4PF,+-0.1PF,50V	807206	51406	MA180R4BPT	1	
C	418		CAP,CER,10PF,+-5%,50V,COG,0805	494781	51406	GRH708C0G100J200VPT	1	
C	419,420		CAP,CER,33PF,+-2%,100V,COG	513226	04222	SR151A330GAA	2	
C	421		CAP,CER,68PF,+-2%,100V,COG	362756	04222	SR291A680GAATR1A	1	
C	431		CAP,CER,100PF,+-5%,50V,COG,0805	514133	51406	GRH708C0G101J200VPT	1	
H	1- 4		SCREW,PH,P,MAG,SS,LOCK,6-32,.500	853986	COMMERCIAL		4	
J	1- 3		SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	3	
J	4		CONN,COAX,SMA(F),PWB,RT ANG	512855	74970	142-0299-046	1	
L	403		INDUCTOR,0.056UH,+-5%,1000MHZ	844907	52763	5087226-613	1	
L	404		INDUCTOR,0.10UH,+-10%,400MHZ,SHLD	257154	24759	MR-0.10	1	
MP	1, 3		DELAY CABLE CLAMP, TOP, PLATED	861096	89536	861096	2	
MP	2, 4		DELAY CABLE CLAMP, BOTTOM, PLATED	868901	89536	868901	2	
MP	5		SLEEV,POLYOL,SHRINK,.093-.046ID,BLACK	149443	89536	149443	5	
MP	6- 14		PIN,SINGLE,PWB,0.025 SQ	277418	00779	1-87022-3	9	
P	4		CONN,COAX,SMA(M),CABLE	520114	7K354	2001-7585-00	1	
R	418,419	*	RES,CERM,51,+-5%,.125W,200PPM,1206	746271	91637	CRCW1206-51R0JB02	2	
R	420		RES,MF,51.1,+-1%,0.25W,100PPM	799650	91637	CCF-5051R1F	1	
R	421		RES,MF,10K,+-1%,0.25W,100PPM	799635	91637	CCF-501002F	1	
TP	1, 2		TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	2	
U	403	*	3DB COUPLER FOR COARSE LOOP	860650	89536	860650	1	
U	404		MIXER,DOUBLE BALANCED,5 - 1000 MHZ	512103	1AV65	TFM-2H-8	1	
W	8		A22,DELAY LINE CABLE ASSEMBLY	860783	89536	860783	1	
W	9		CABLE,COAX,50 OHM,SEMI-RIGID,24 AWG	267567	89536	267567	1	

An * in 'S' column indicates a static-sensitive part.


MP1, 2
A25
H1
H2
W9
A26
H4
H3
W8
MP3, 4
P4
A22

6082A-2701

Figure 8-22. A22 Delay Line Assembly


A25
C431
U404
R419
L403
J10
L404
R421
J3
C418
C419
C420
TP
TP2
O3
J9
R418
2
R420
C421
U403
O4
1
J2
J1
J4
C1
J5
A26

6080A-1668

Figure 8-22. A22 Delay Line Assembly (cont)

MANUFACTURER'S FEDERAL SUPPLY CODES

00779
AMP, Inc.
Harrisburg, PA

01121
Allen Bradley Co.
Milwaukee, WI

01295
Texas Instruments Inc.
Semiconductor Group
Dallas,TX

01526
Genicom
Waynesboro, VA

02113
Coilcraft Inc.
Cary, IL

03508
General Electric Co.
Semiconductor Products
& Batteries
Auburn, NY

04222
AVX Corp.
AVX Ceramics Div.
Myrtle Beach, SC

04713
Motorola Inc.
Semiconductor Group
Phoenix, AZ

05791
Lyn-Tron
Burbank, CA

06383
Panduit Corp.
Tinley Park, IL

06665
Precision Monolithics
Sub of Bourns Inc.
Santa Clara, CA

06915
Richco Plastic Co.
Chicago, IL

07047
Ross Milton Co., The
Southampton, PA

07263
Fairchild Semiconductor
North American Sales
Ridgeview, CT

080A9
Dallas Semiconductor
Dallas, TX

09214
General Electric Co.
Semiconductor Products Dept.
Auburn, NY

0A5E9
MC Engineering
Greer, SC

0BW21
Noritake Co. Inc.
Burlington, MA

10059
Barker Engineering Corp.
Kenilworth, NJ

12040
National Semiconductor Corp.
Danbury, CT

12581
Hitachi Metals Inernational Ltd.
Hitachi Magna-Lock Div.
Big Rapids, MO

13103
Thermalloy Co., Inc.
Dallas, TX

13715
Fairchild Semiconductor Corp.
Components Group
Formerly Fairchild Camera &
Instrument
San Rafael, CA

15801
Fenwal Eletronics Inc.
Div. of Kidde Inc.
Framingham, MA

17856
Siliconix Inc.
Santa Clara, CA

18310
Concord Electronics
New York, NY

18324
Signetics Corp.
Sacramento, CA

18565
Chomerics Inc.
Woburn, MA

19701
Philips Components
Formerly Mepco/Centralab Inc.
A N. American Philips Co.
Mineral Wells, TX

1AV65
Mini-Circuits
c/o Robotron Inc.
Brooklyn, NY

1L965
Lord Industrial
Cambridge Springs, PA

20584
Enochs Mfg. Inc.
Indianapolis, IN

21845
Solitron Devices Inc.
Semiconductor Group
Rivera Beach, FL

22526
DuPont, El DeNemours & Co. Inc.
DuPont Connector Systems
Advanced Products Div.
New Cumberland, PA

22670
GM Nameplate
Seattle, WA

24347
Penn Engineering Co.
S. El Monte, CA

24355
Analog Devices Inc.
Norwood, MA

24759
Lenox-Fugle Electronics Inc.
South Plainfield, NJ

25088
Siemen Corp.
Isilen, NJ

25403
Amperex Electronic Corp.
Semiconductor & Micro-Circuit Div.
Slatersville, RI

27014
National Semiconductor Corp.
Santa Clara, CA

27264
Molex Inc.
Lisle, IL

28213
Minnesota Mining & Mfg. Co.
Consumer Products Div.
3M Center
Saint Paul, MN

28480
Hewlett Packard Co.
Corporate HQ
Palo Alto, CA

30035
Jolo Industries Inc.
Garden Grove, CA

30800
General Instrument Corp.
Capacitor Div.
Hicksville, NY

31091
Alpha Industries Inc.
Microelectronics Div.
Hatfield, PA

31918
ITT-Schadow
Eden Prairie, MN

32997
Bourns Inc.
Trimpot Div.
Riverside, CA

33025
M/A ComOmni Spectra, Inc.
(Replacing Omni Spectra)
Microwave Subsystems Div.
Tempe, AZ

33297
NEC Electronics USA Inc.
Electronic Arrays Inc. Div.
Mountain View, CA

34371
Harris Corp.
Harris Semiconductor
Products Group
Melbourne, FL

34641
Instrument Specialties
Euless, TX

40402
Roderstein Electronics Inc.
Statesville, NC

50472
Metal Masters, Inc.
City of Industry, CA

50579
Litronix Inc.
Cupertino, CA

51406
Murata Erie, No. America Inc.
Symrna, GA

51984
NEC America Inc.
Falls Church, VA

52500
Amphenol, RF Operations
Burlington, MA

52763
Stettner-Electronics Inc.
Chattanooga, TN

53217
Technical Wire Products Inc.
Was Tecknit - 6A566
Santa Barbara, CA

54583
TDK
Garden City, NY

55267
Hughes Aircraft Co.
Semiconductor Div.
Newport Beach, CA

MANUFACTURER'S FEDERAL SUPPLY CODES

55285
Bercquist Co.
Minneapolis, MN

55464
Central Semiconductor Corp.
Hauppauge, NY

55566
R A F Electronic Hardware Inc.
Seymour, CT

55787
Gas Spring
Montgomeryville, PA

56289
Sprague Electric Co.
North Adams, MA

57693
Oscillalek Corp
Olathe, KS

59124
KOA-Speer Electronics Inc.
Bradford, PA

59365
Metelics Corp.
Sunnyvale, CA

59660
Tusonix Inc.
Tucson, AZ

5T512
Interconnect Devices
Kansas City, KS

60204
Fleck Co., Inc.
Auburn, WA

60705
Cera-Mite Corp.
(formerly Sprague)
Grafton, WI

60935
Westlake Capacitor Inc.
Tantalum Div.
Greencastle, IN

61271
Fujitsu Microelectronics Inc
San Jose, CA

61529
Aromat Corp.
New Providence, NJ

61752
IR-ONICS Inc
Warwick, RI

62643
United Chemicon
Rosemont, IL

64155
Linear Technology
Milpitas, CA

64537
KDI Electronics
Whippany, NJ

65940
Rohm Corp
Irvine, CA

66419
Exel
San Jose, CA

68919
Wima (International)
Harry Levinson
Seattle, WA

6E283
Packaging Commodities
Kent, WA

70903
Cooper-Belden Corp.
Geneva, IL

71034
Bliley Electric Co.
Erie, PA

71400
Bussman Div.-Cooper
Industries Inc.
St. Louis, MO

71707
Coto Corp.
Providence, RI

72259
Nytronics Inc.
New York, NY

72962
Elastic Stop Nut
Div. of Harrard Industries
Union, NJ

72982
Erie Specialty Products, Inc
Formerly: Murata Erie
Erie, PA

73734
Federal Screw Products Inc.
Chicago, IL

74970
Johnson EF Co.
Waseca, MN

79727
C - W Industries
Southampton, PA

7E751
Avantek Inc.
Santa Clara, CA

7K354
Omni Spectra Inc
Los Altos, CA

80294
Bourns Instruments Inc.
Riverside, CA

84411
American Shizuki
TRW Capacitors Div.
Ogallala, NE

86928
Seastrom Mfg. Co. Inc.
Glendale, CA

88978
Philips (Now Fluke)
Mahwah, NJ

89536
John Fluke Mfg. Co., Inc.
Everett, WA

91247
Illinois Transformer Co.
Chicago, IL

91293
Johanson Mfg. Co.
Boonton, NJ

91502
Associated Machine
Santa Clara, CA

91506
Augat Alcoswitch
N. Andover, MA

91637
Dale Electronics Inc.
Columbus, NE

91984
Maida Development Co.
Hampton, VA

95146
Alco Electronic Products Inc.
Switch Div.
North Andover, MA

95275
Vitramon Inc.
Bridgeport, CT

98159
Rubber-Teck Inc.
Gardena, CA

98291
Sealectro Corp.
BICC Electronics
Trumbill, CT

9W423
Amatom
El Mont, CA

H0002
OGNL3
Philips
Milipatas, CA

S4821
Tocos (Japan) Tokyo Cosmos
Arlington Heights, IL

SERVICE CENTERS

U.S.A

California

Fluke Technical Center
46610 Landing Parkway
Fremont, CA 94538
Tel: (415) 651-5112

Fluke Technical Center
16715 Von Karman Avenue
Suite 110
Irvine, CA 92714
Tel: (714) 863-9031

Colorado
Fluke Technical Center
14180 East Evans Avenue
Aurora, CO 80014
Tel: (303) 695-1171

Florida
Fluke Technical Center
550 S. North Lake Blvd.
Altamonte Springs, FL 32701-5227
Tel: (407) 331-2929

Illinois
Fluke Technical Center
1150 W. Euclid Ave.
Palatine, IL 60067
Tel: (708) 705-0500

Maryland
Fluke Technical Center
5640 Fishers Lane
Rockville, MD 20852
Tel: (301) 770-1576

New Jersey
Fluke Technical Center
East 66 Midland Avenue
Paramus, NJ 07652-0930
Tel: (201) 599-9500

Texas
Fluke Technical Center
2104 Hutton Drive
Suite 112
Carrollton, TX 75006
Tel: (214) 406-1000

Washington
Fluke Technical Center
John Fluke Mfg. Co., Inc.
1420 75th St. S.W.
M/S 6-30
Everett, WA 98203
Tel: (206) 356-5560

INTERNATIONAL

Argentina
Coasin S.A.
Virrey del Pino 4071 DPTO E-65
1430 CAP FED
Buenos Aires
Tel: 54 1 522-5248

Australia
Philips Customer Support
Scientific and Industrial
23 Lakeside Drive
Tally Ho Technology Park
East Burwood
Victoria 3151

Philips Customer Support
Scientific & Industrial
25-27 Paul St. North
North Ryde, N.S.W. 2113
Tel: 61 02 888 8222

Austria
Oesterreichische Philips Industrie
Unternehmensbereich Prof. Systeme
Triesterstrasse 66
Postfach 217
A-1101 Wein
Tel: 43 222-60101, x1388

Belgium
Philips Professional Systems S.A.
I & E Division
Service Department
Rue des deux Gares 80
1070 Brussels
Tel: 32 2 525 6111

Brazil
Hi-Tek Electronica Ltda.
Al. Amazonas 422, Alphaville
CEP 06400 Barueri
Sao Paulo
Tel: 55 011 421-5477

Canada
Fluke Electronics Canada Inc.
400 Britannia Rd. East, Unit #1
Mississauga, Ontario
L4Z 1X9
Tel: 416-890-7600

Chile
Intronsa Inc.
Casilla 16158
Santiago 9
Tel: 56 2 232-1886, 232-4308

China
Fluke International Corp.
P.O. Box 9085
Beijing
Tel: 86 01 512-3436

Colombia
Sistemas E Instrumentacion, Ltda.
Carrera 21, No. 39A-21, Of. 101
Ap. Aereo 29583
Bogota
Tel: 57 287-5424

Denmark
Philips Eleltronix Systemer A/S
Strandlodsvejj 4B
DK-2300
Copenhagen
Tel: 45 32 882531

Ecuador
Proteco Coasin Cia., Ltda.
P.O. Box 228-A
Ave. 12 de Octubre
2285 y Orellana
Quito
Tel: 593 2 529684

Egypt
Philips Egypt
10, Abdel Rahman el Rafei st.
el. Mohandessin
P.O. Box 242
Dokki Cairo
Tel: 20-2-490922

England
Philips Scientific
Test & Measuring Division
Colonial Way
Watford
Hertfordshire WD2 4TT
Tel: 44 923-240511

Federal Republic of Germany
Philips GmbH
Service VSF
Unternehmensbereich Electronik
fuer Wissenschaft und Industrie
Oskar-Messter-Strasse 18
D-8045 Ismaning
49 89 9605 261

Finland
OY PHILIPS AB
Central Service
Sinikalliontie 1-3
P.O. Box 11
SF-02631 ESPOO
Tel: 358-0-52572

France
S.A. Philips Industrielle
et Comerciale,
Science et Industry
105 Rue de Paris BP 62
93002 Bobigny, Cedex
Tel: 33-1-4942-8040

Greece
Philips S.A. Hellenique
15, 25th March Street
177 78 Tavros
10210 Athens
Tel: 30 1 4894911

Hong Kong
Schmidt & Co (H.K.) Ltd.
18/FL., Great Eagle Centre
23 Harbour Road
Wanchai
Tel: 852 5 8330222

India
Hinditron Services Pvt. Inc.
33/44A Raj Mahal Villas Extn.
8th Main Road
Bangalore 560 080
Tel: 91 812 363139

Hinditron Services Pvt. Ltd
1st Floor, 17-B,
Mahal Industrial Estate
Mahakali Road, Andheri East
Bombay 400 093
Tel: 91 22 6300043

Hindtron Services Pvt. Ltd.
15 Community Centre
Panchshila Park
New Delhi 110 017
Tel: 011-6433675

Field Service Center
Hinditron Services Pvt. Ltd.
Emerald Complex 1-7-264
5th Floor
114 Sarojini Devi Road
Secunderabad 500 003
Tel: 08 42-821117

Israel
R.D.T. Electronics Engineering, Ltd.
P.O. Box 43137
Tel Aviv 61430
Tel: 972 3 483211

Italy
Philips S.p.A.
Sezione I&E / T&M
Viale Elvezia 2
20052 Monza
Tel: 39-39-363-5315

Japan
John Fluke Mfg. Co., Inc.
Japan Branch
Sumitomo Higashi Shinbashi Bldg.
1-1-11 Hamamatsucho
Minato-ku
Tokyo 105
Tel: 81 3 434-0181

Korea
Myoung Corporation
Yeo Eui Do P.O. Box 14
Seoul 150
Tel: 82 2 784-9942

Malaysia
Mecomb Malaysia Sdn. Bhd.
P.O. Box 24
46700 Petaling Jaya
Selangor
Tel: 60 3 774-3422

Mexico
Mexel Mexicana De Electronica
Industrial, S.A. De C.V.
Calle Diagonal #27 3er.
Col. Del Valle
C. P. 03100, Mexico D.F.
Tel: 52-5-682-8040

Netherlands
Philips Nederland
Test & Measurement Division
Postbox 115
5000 AC Tilburg
Tel: 31-13-390172

New Zealand
Philips Customer Support
Scientific & Industrial
2 Wagener Place
Mt. Albert
Auckland
Tel: 64 9 894-160

Norway
Norsk A/S Philips
I&E Service
Sandstuveien 70
Postboks 1 Manglerud
N 0680 OSLO 6
Tel: 47-2-680200

Pakistan
International Operations (PAK) Ltd.
505 Muhammadi House
I.I. Chundrigar Road
P.O. Box 5323
Karachi
Tel: 92 21 221127, 239052

Peru
Importaciones & Representaciones
Electronicas S.A.
Avad Franklin D. Roosevelt 105
Lima 1
Tel: 51 14 288650

Philippines
Spark Electronics Corp.
P.O. Box 610, Greenhills
Metro Manila 1502
Tel: 63-2-700-621

SERVICE CENTERS (cont)

Portugal
Philips Portuguese S.A.
I&E Division
Estrada de Outurela-Carnaxide
2795 Linda-A-Velha
Tel: 418 00 71

Singapore
Rank O'Connor's Singapore Pte Ltd
98 Pasir Panjang Road
Singapore 0511
Tel: 65 4737944

South Africa
South African Philips (Pty) Ltd.
Service Department
195 Main Rd
Martindale, Johannesburg 2092
Tel: 27 11 470-5255

Spain
Philips Iberica Sae
Depto. Tecnico Instrumentacion
c/Martinez Villergas 2
28027 Madrid
Tel: 34 1 4042200

Sweden
Philips Kistaindustrier AB
I&E Technical Customer Support
Borgarfjordsgatan 16
S 164 93 Kista
Tel: 46-8-703-1000

Switzerland
Philips A.G.
Technischer Kundendienst
Postfach 670
Allmendstrasse 140
CH-8027 Zurich
Tel: 41 1 488 29 63

Taiwan, R.O.C.
Schmidt Electronics Corp.
5th Floor, Cathay Min Sheng
Commercial Building,
344 Min Sheng East Road
Taipei
Tel: 886 2 501-3468

Thailand
Measuretronix Ltd.
2102/31 Ramkamhaeng Rd.
Bangkok 10240
Tel: 66 2 375-2733, 375-2734

Turkey
Turk Philips Ticaret A.S.
Inonu Caddesi 78/80
Posta Kutusu 504-Beyoglu
Istanbul
Tel: 90 1 1435891

Uruguay
Coasin Uruguaya S.A
Casilla de Correo 1400
Libertad 2525
Montevideo
Tel: 598-2-789015

Venezuela
Coasin C.A.
Calle 9 Con Calle 4, Edif. Edinurbi
Apartado de Correos Nr-70-136
Los Ruices
Caracas 1070-A
Tel: 58 2 241-0309, 241-1248

Section 9
Options

INTRODUCTION 9-1.

This section includes operation notes, a description, and maintenance instructions for each option. Each of these options must be installed at the factory or at one of the Fluke Technical Service Centers listed in Section 8. Each of these options is used interchangeably for Model 6080A or 6082A.

6080A-130 HIGH-STABILITY REFERENCE 9-2.

With the rear panel REF INT/EXT switch set to INT, the 6080A-130 Option takes over the 10-MHz internal reference function. Stability specifications are enhanced as defined in the Specifications in Section 1.

The High-Stability Reference consists of an ovened oscillator (Y1), mounting hardware, and cables. The ovened oscillator is not field repairable.

NOTE

The oscillator oven stays energized whenever line power is connected to an ac outlet. The oven stays warmed to the correct temperature regardless of the POWER switch or internal/external reference setting.

Adjusting the Reference Frequency 9-3.

CAUTION

THIS ADJUSTMENT REQUIRES OPERATING THE INSTRUMENT WITH THE TOP COVER REMOVED. USE CARE TO AVOID ELECTRIC SHOCK. ONLY QUALIFIED PERSONNEL SHOULD PERFORM THIS PROCEDURE.

You can adjust the frequency of the High-Stability Reference. The following test equipment is required:

- 10 MHz frequency standard
- Dual-trace oscilloscope
- Two 3-ft 50Ω coaxial cables and 50Ω BNC feedthrough terminations

NOTE

Operate the Signal Generator at room temperature for at least three hours before adjusting the High-Stability Reference frequency.

Proceed as follows to adjust the High-Stability Reference frequency:

1. Remove the top instrument cover and the two FREQ ADJ access screws from the side of the ovened oscillator facing the front panel.
2. Connect the frequency standard to the oscilloscope vertical input channel 1 using a 50Ω feedthrough termination at the oscilloscope input.
3. Connect the Signal Generator rear panel 10 MHz OUT BNC connector to the oscilloscope vertical input channel 2 using a 50Ω feedthrough termination at the oscilloscope input.
4. Set the Signal Generator rear panel REF INT/EXT switch to INT.
5. Set the vertical controls of the oscilloscope to display the Signal Generator's 10-MHz internal reference signal and the signal from the frequency standard.
6. Set the oscilloscope for internal triggering on channel 1, and adjust the timebase for 0.1 μs/div.
7. Adjust the High-Stability Reference COARSE control for the best match of the frequencies displayed on the oscilloscope.
8. Adjust the High-Stability Reference FINE control for a drift of less than one cycle in 10 seconds (for 0.01 ppm) or better if desired.

List of Replaceable Parts 9-4.

A list of replaceable parts for the 6080A-130 Option is provided in Table 9-1. Figure 9-1 shows the location of the ovened oscillator and its associated parts.

6080A-132 MEDIUM-STABILITY REFERENCE 9-5.

With the rear panel REF INT/EXT switch set to INT, the 6080A-130 Option takes over the 10-MHz internal reference function. Stability specifications are enhanced as defined in the Specifications in Section 1.

The Medium-Stability Reference consists of an ovened oscillator (Y1), mounting hardware, and cables. The ovened oscillator is not field repairable.

NOTE

The oscillator oven stays energized whenever line power is connected to an ac outlet. The oven stays warmed to the correct temperature regardless of the POWER switch or internal/external reference setting.

Adjusting the Reference Frequency 9-6.

CAUTION

THIS ADJUSTMENT REQUIRES OPERATING THE INSTRUMENT WITH THE TOP COVER REMOVED. USE CARE TO AVOID ELECTRIC SHOCK. ONLY QUALIFIED PERSONNEL SHOULD PERFORM THIS PROCEDURE.

You can adjust the frequency of the Medium-Stability Reference. The following test equipment is required:

- 10 MHz frequency standard
- Dual-trace oscilloscope
- Two 3-ft 50Ω coaxial cables and 50Ω BNC feedthrough terminations.

NOTE

Operate the Signal Generator at room temperature for at least three hours before adjusting the Medium-Stability Reference frequency.

Proceed as follows to adjust the Medium-Stability Reference frequency:

1. Remove the top instrument cover and the FREQ ADJ COARSE adjustment access screw from the side of the ovened oscillator facing the front panel.

2. Connect the frequency standard to the oscilloscope vertical input channel 1 using a 50Ω feedthrough termination at the oscilloscope input.

3. Connect the Signal Generator rear panel 10 MHz OUT BNC connector to the oscilloscope vertical input channel 2 using a 50Ω feedthrough termination at the oscilloscope input.

4. Set the Signal Generator rear panel REF INT/EXT switch to INT.

5. Set the vertical controls of the oscilloscope to display the Signal Generator's 10-MHz internal reference signal and the signal from the frequency standard.

6. Set the oscilloscope for internal triggering on channel 1, and adjust the timebase for 0.1 μs/div.

7. Adjust the Medium-Stability Reference FREQ ADJ COARSE control for a drift of less than one cycle in 10 seconds (for 0.01 ppm) or better if desired.

List of Replaceable Parts 9-7.

A list of replaceable parts for the 6080A-132 Option is provided in Table 9-2. Figure 9-1 shows the location of the ovened oscillator and its associated parts.

OPTION 6080A-830 REAR OUTPUT/MODULATION INPUT 9-8.

Option 6080A-830 moves the RF OUTPUT, MOD OUTPUT, and MODULATION INPUT connectors from the front panel to the rear panel. This option does not change the operation, specifications, performance tests, calibration, adjustment, or service of the Signal Generator.

Theory of Operation 9-9.

When the 6080A-830 Option is installed, a longer internal semi-rigid coaxial SMA cable assembly replaces the standard internal cable for the Signal Generator's RF output. The option switch on the A13 Controller PCA is set to indicate that the option is installed. The setting of the Controller PCA option switch causes the additional signal loss of this longer cable to be compensated with instrument-independent correction data stored in compensation memory.

List of Replaceable Parts 9-10.

A list of replaceable parts for the 6080A-830 Option is provided in Table 9-3. Figure 9-2 shows the internal cabling differences from the standard front panel input/output configuration.

Table 9-1. Option -130 High Stability Reference
(See Figure 9-1.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	NOTE
H	1- 4		SCREW,FH,P,STL,LOCK,4-40,.250	114884	COMMERCIAL		4	
H	5, 6		SCREW,PH,P,STL,LOCK,6-32,.187	381087	COMMERCIAL		2	
H	7- 10		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		4	
MP	1- 18		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	18	
MP	19		BRACKET, HI/MED STABILITY OSCILLATOR	812776	89536	812776	1	
MP	20		CABLE ACCESSORY,CLAMP,ADHESIVE,NYLON	838300	06915	MWSSEB-1-01A	1	
W	24		CABLE ASSY,HIGH-MED STABILITY, POWER	868856	89536	868856	1	
W	25		CABLE ASSY HIGH-MED STABILITY,CONTROL	868864	89536	868864	1	
W	26		CABLE,COAX. ASSY. R.F.	205807	89536	205807	1	
Y	1		OSCILLATOR,10MHZ,OVENIZED	855044	12040	OSC49-91	1	

An * in 'S' column indicates a static-sensitive part.

Table 9-2. Option -132 Medium Stability Reference
(See Figure 9-1.)

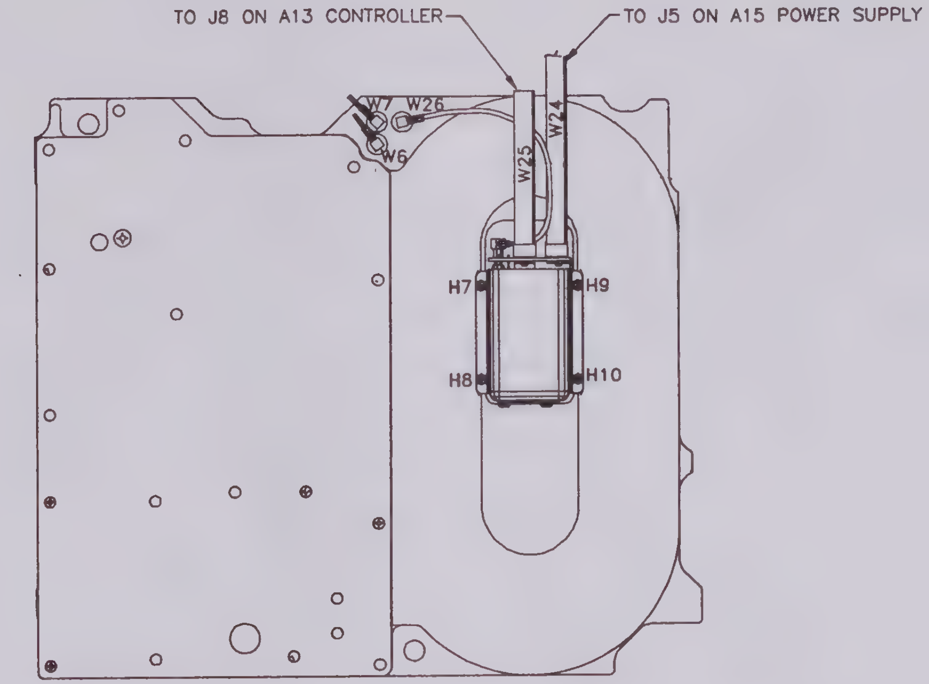
REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	NOTE
H	1- 4		SCREW,FH,P,STL,LOCK,4-40,.250	114884	COMMERCIAL		4	
H	5, 6		SCREW,PH,P,STL,LOCK,6-32,.187	381087	COMMERCIAL		2	
H	7- 10		SCREW,PH,P,MAG,SS,LOCK,6-32,.281	772236	COMMERCIAL		4	
MP	1- 18		PIN,SINGLE,PWB,0.025 SQ	267500	00779	87623-1	18	
MP	19		BRACKET, HI/MED STABILITY OSCILLATOR	812776	89536	812776	1	
MP	20		CABLE ACCESSORY,CLAMP,ADHESIVE,NYLON	838300	06915	MWSSEB-1-01A	1	
W	24		CABLE ASSY,HIGH-MED STABILITY, POWER	868856	89536	868856	1	
W	25		CABLE ASSY HIGH-MED STABILITY,CONTROL	868864	89536	868864	1	
W	26		CABLE,COAX. ASSY. R.F.	205807	89536	205807	1	
Y	1		OSCILLATOR,10MHZ,OVENIZED	866751	12040	OSC83-19	1	

An * in 'S' column indicates a static-sensitive part.

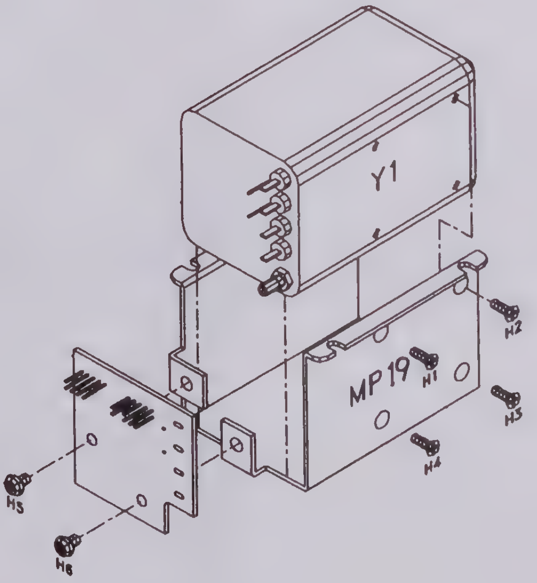
Table 9-3. Option -830 Rear Panel RF Output and Modulation Input
(See Figure 9-2.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	NOTE
E	1- 9		CORE,TOROID,FERRITE,20X14.5X7.5MM	493551	54583	H5C2-T20-7.5-14.5	9	
H	1		NUT,HEX,ELAST STOP,STL,6-32,.125	110841	72962	22NTM-62	4	
H	2		SCREW,FHU,P,STL,LOCK,4-40,.312	268193	COMMERCIAL		4	
H	3		SCREW,PH,P,SS,LOCK,8-32,.750	335109	COMMERCIAL		3	
MP	1		PLATE, REAR RF OUTPUT, PLATED	861104	89536	861104	1	
MP	2		CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	11	
MP	3		CABLE ACC,CLAMP,.187 ID,SCREW MOUNT	101345	06915	N3B	3	
MP	4		SPACER,RND,NYL,.187ID,.250	158634	55566	1186-.187-N	3	
MP	5		FRONT TOROID BRACKET	882753	89536	882753	1	
W	1		CABLE ASSY, SR, REAR RF OUTPUT	868898	89536	868898	1	
W	2- 5		RF INTERCONNECT HARNESS	868851	89536	868851	1	

An * in 'S' column indicates a static-sensitive part.

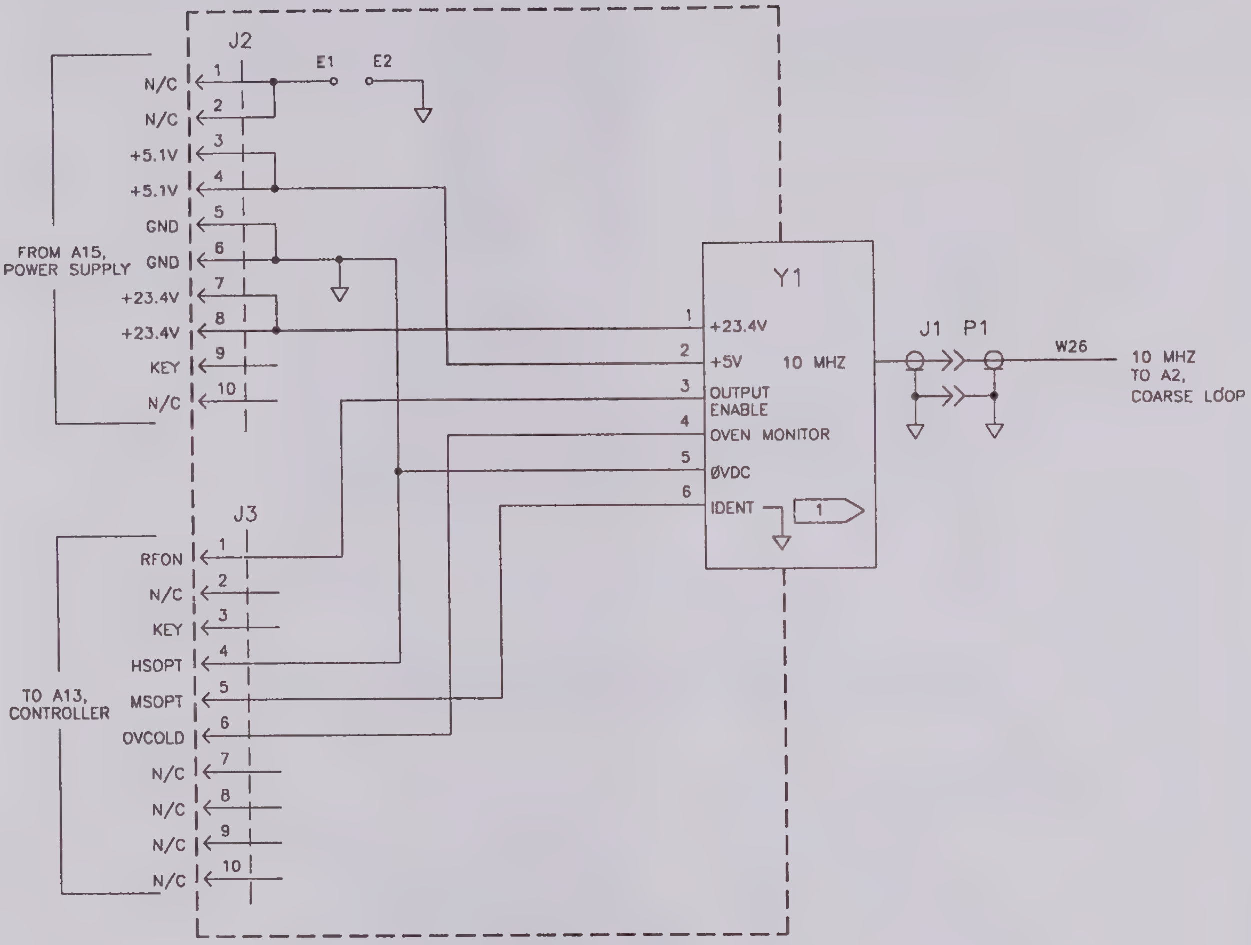

TO J8 ON A13 CONTROLLER
TO J5 ON A15 POWER SUPPLY
W7
W26
W6
W25
W24
H7
H9
H8
H10

INSTALLATION OF OPTION INTO A60 SYNTHESIZER MODULE


Y1
MP19
H1
H2
H3
H4
H5
H6

6080A-130

Figure 9-1. Option -130 High and -132 Medium Stability Reference


J2
E1
E2
N/C 1
N/C 2
+5.1V 3
+5.1V 4
GND 5
GND 6
+23.4V 7
+23.4V 8
KEY 9
N/C 10
FROM A15, POWER SUPPLY
J3
RFON 1
N/C 2
KEY 3
HSOPT 4
MSOPT 5
OVCOLD 6
N/C 7
N/C 8
N/C 9
N/C 10
TO A13, CONTROLLER
Y1
1 +23.4V
2 +5V
10 MHZ
3 OUTPUT ENABLE
4 OVEN MONITOR
5 ØVDC
6 IDENT
1
J1
P1
W26
10 MHZ TO A2, COARSE LOOP

NOTES: UNLESS OTHERWISE SPECIFIED,

1 THIS SCHEMATIC DESCRIBES BOTH A28, OPTION −130, HIGH STABILITY REF, AND A29, OPTION −132, MEDIUM STABILITY REF. THE HIGH STABILITY OSCILLATOR IS ILLUSTRATED; IN THE MEDIUM STABILITY OSCILLATOR, PIN 6 IS NOT INTERNALLY GROUNDED. THE TABLE BELOW SHOWS THE STATE OF THE SIGNALS ON A13, CONTROLLER, WHEN EITHER OR NO OPTION IS INSTALLED:

SIGNAL		
HSOPT	MSOPT	
0	0	OPTION −130 (HIGH STABILITY)
0	1	OPTION −132 (MEDIUM STABILITY)
1	1	NO OPTION

6082A-1074

Figure 9-1. Option -130 High and -132 Medium Stability Reference (cont)

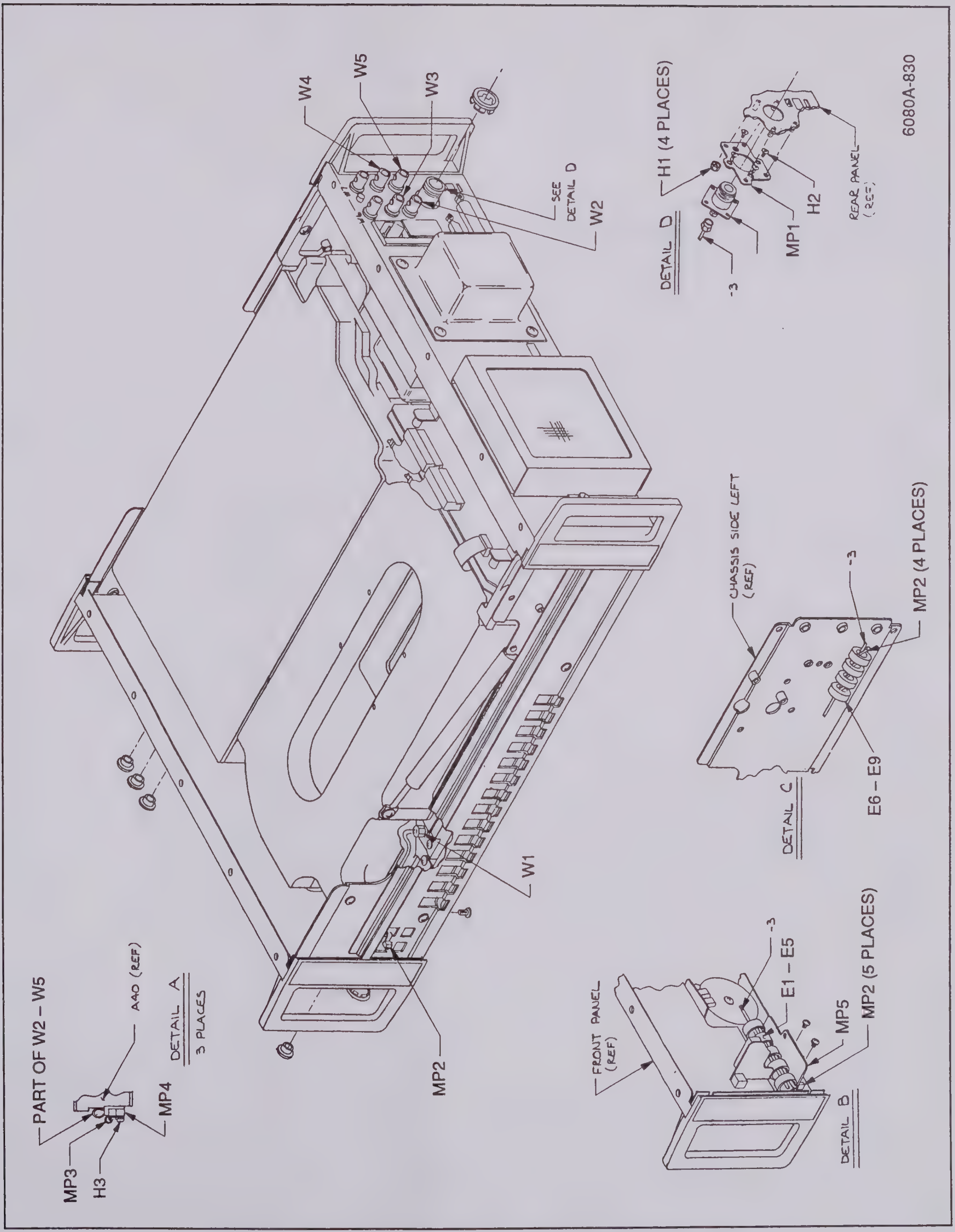
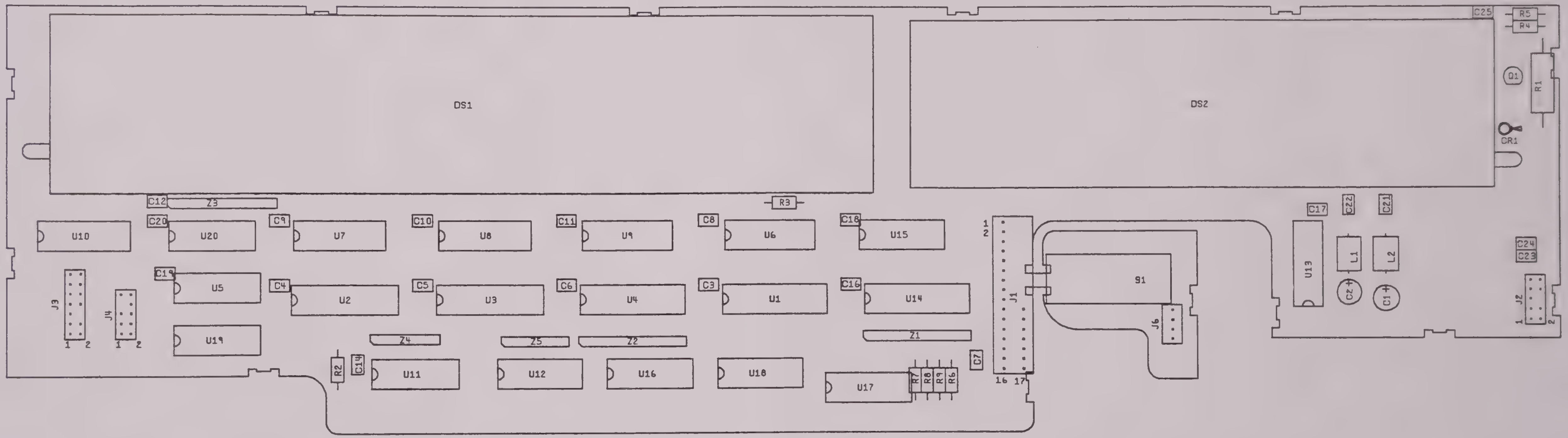

W4
W5
W3
SEE DETAIL D
W2
H1 (4 PLACES)
DETAIL D
-3
MP1
H2
REAR PANEL (REF)
6080A-830
CHASSIS SIDE LEFT (REF)
-3
MP2 (4 PLACES)
E6 - E9
DETAIL C
W1
PART OF W2 - W5
A40 (REF)
DETAIL A
3 PLACES
MP4
MP3
H3
MP2
FRONT PANEL (REF)
-3
E1 - E5
MP5
MP2 (5 PLACES)
DETAIL B

Figure 9-2. Option -830 Rear Panel RF Output and Modulation Input

Section 10
Schematic Diagrams

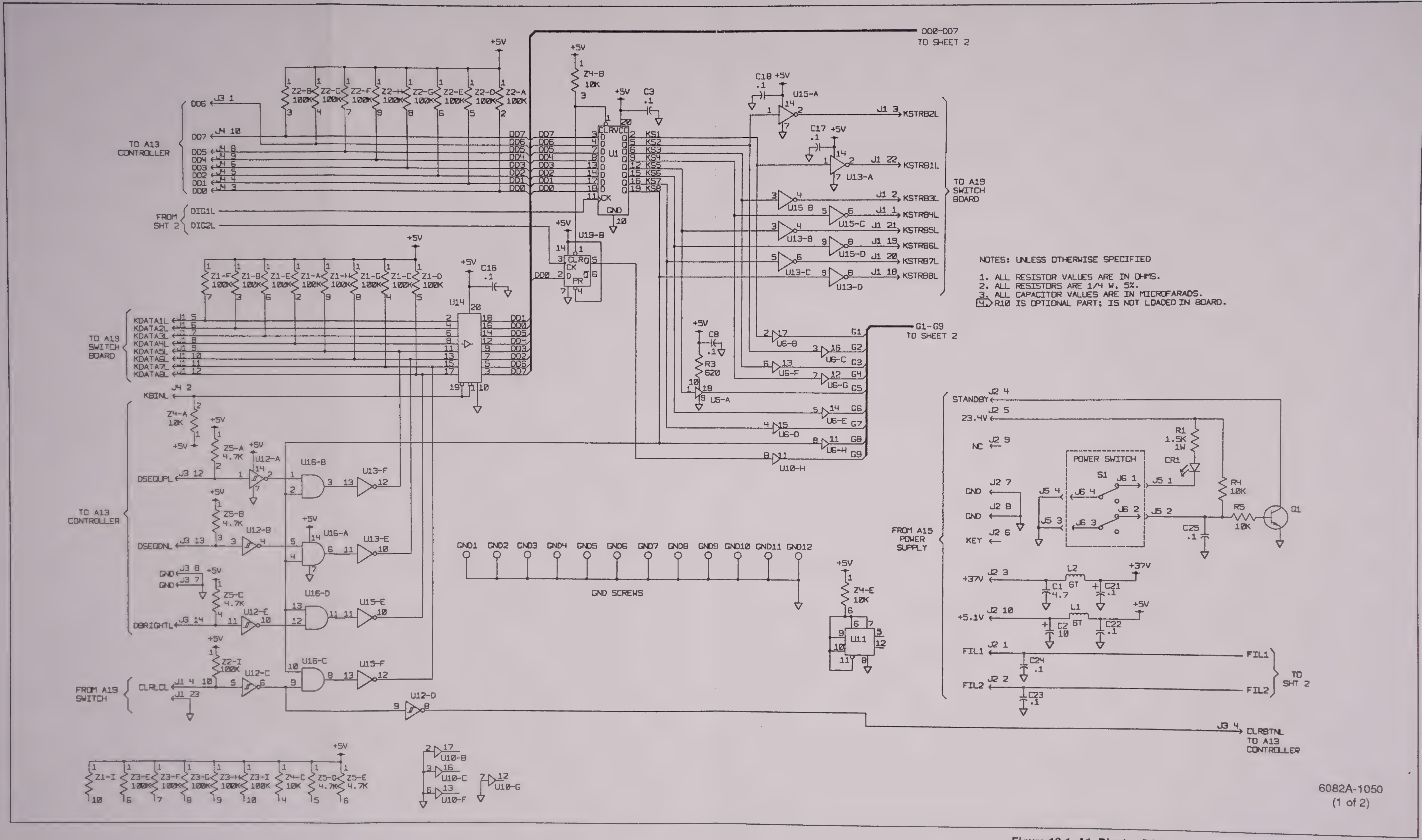
TABLE OF CONTENTS

FIGURE	TITLE	PAGE
10-1.	A1 Display PCA	10-3
10-2.	A2 Coarse Loop PCA	10-6
10-3.	A3 Subsynthesizer VCO PCA	10-11
10-4.	A4 Subsynthesizer PCA	10-13
10-5.	A5 Coarse Loop VCO PCA	10-17
10-6.	A6 Mod Oscillator PCA	10-19
10-7.	A8 Output PCA	10-22
10-8.	A9 Sum Loop VCO PCA	10-26
10-9.	A10 Premodulator PCA	10-28
10-10.	A11 Modulation Control PCA	10-32
10-11.	A12 Sum Loop PCA	10-36
10-12.	A13 Controller PCA	10-40
10-13.	A14 FM PCA	10-45
10-14.	A15 Power Supply PCA	10-50
10-15.	A16 IEEE Connector PCA	10-53
10-16.	A17 Cable Transition PCA	10-54
10-17.	A18 Cable Transition PCA	10-55
10-18.	A19 Switch PCA	10-56
10-19.	A20A7 Relay Driver PCA	10-58
10-20.	A20A21 Attenuator PCA	10-60
10-21.	A22 Delay Line Assembly	10-61


C25
R5
R4
DS1
DS2
Q1
R1
CR1
C12
Z3
R3
C17
C22
C21
C20
U10
U20
C9
U7
C10
U8
C11
U9
C8
U6
C18
U15
1
2
U13
L1
L2
C24
C23
C19
U5
C4
U2
C5
U3
C6
U4
C3
U1
C16
U14
J1
S1
C2
C1
J2
1
2
J3
J4
1 2
1 2
U19
Z4
Z5
Z2
Z1
J6
R2
C14
U11
U12
U16
U18
C7
R7
R8
R9
R6
U17
16
17

6082A-1650

Figure 10-1. A1 Display PCA


DD0-DD7
TO SHEET 2
G1-G9
TO SHEET 2
TO A13 CONTROLLER
DD6
DD7
DD5
DD4
DD3
DD2
DD1
DD0
FROM SHT 2
DIG1L
DIG2L
TO A19 SWITCH BOARD
KDATA1L
KDATA2L
KDATA3L
KDATA4L
KDATA5L
KDATA6L
KDATA7L
KDATA8L
KBINL
TO A13 CONTROLLER
DSEQUPL
DSEQDNL
DBRIGHTL
FROM A19 SWITCH
CLRLCL
Z2-B 100K
Z2-C 100K
Z2-F 100K
Z2-H 100K
Z2-G 100K
Z2-E 100K
Z2-D 100K
Z2-A 100K
Z1-F 100K
Z1-B 100K
Z1-E 100K
Z1-A 100K
Z1-H 100K
Z1-G 100K
Z1-C 100K
Z1-D 100K
Z4-B 10K
Z4-A 10K
Z5-A 4.7K
Z5-B 4.7K
Z5-C 4.7K
Z2-I 100K
Z4-E 10K
U1
U11
U14
U19-B
U12-A
U12-B
U12-C
U12-D
U12-E
U16-A
U16-B
U16-C
U16-D
U13-A
U13-B
U13-C
U13-D
U13-E
U13-F
U15-A
U15 B
U15-C
U15-D
U15-E
U15-F
U6-A
U6-B
U6-C
U6-D
U6-E
U6-F
U6-G
U6-H
U10-B
U10-C
U10-F
U10-G
U10-H
C3 .1
C16 .1
C17 .1
C18 .1
C8 .1
R3 620
KS1
KS2
KS3
KS4
KS5
KS6
KS7
KS8
KSTRB2L
KSTRB1L
KSTRB3L
KSTRB4L
KSTRB5L
KSTRB6L
KSTRB7L
KSTRB8L
TO A19 SWITCH BOARD
G1
G2
G3
G4
G5
G6
G7
G8
G9
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND SCREWS
FROM A15 POWER SUPPLY
STANDBY
23.4V
NC
GND
GND
KEY
+37V
+5.1V
FIL1
FIL2
R1 1.5K 1W
CR1
POWER SWITCH
S1
R4 10K
R5 10K
Q1
C25 .1
L2 6T
L1 6T
C1 4.7
C21 .1
C2 10
C22 .1
C24 .1
C23 .1
+37V
+5V
TO SHT 2
CLRBTNL
TO A13 CONTROLLER
Z1-I
Z3-E 100K
Z3-F 100K
Z3-G 100K
Z3-H 100K
Z3-I 100K
Z4-C 10K
Z5-D 4.7K
Z5-E 4.7K
6082A-1050
(1 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL RESISTORS ARE 1/4 W, 5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. R10 IS OPTIONAL PART; IS NOT LOADED IN BOARD.

Figure 10-1. A1 Display PCA (cont)

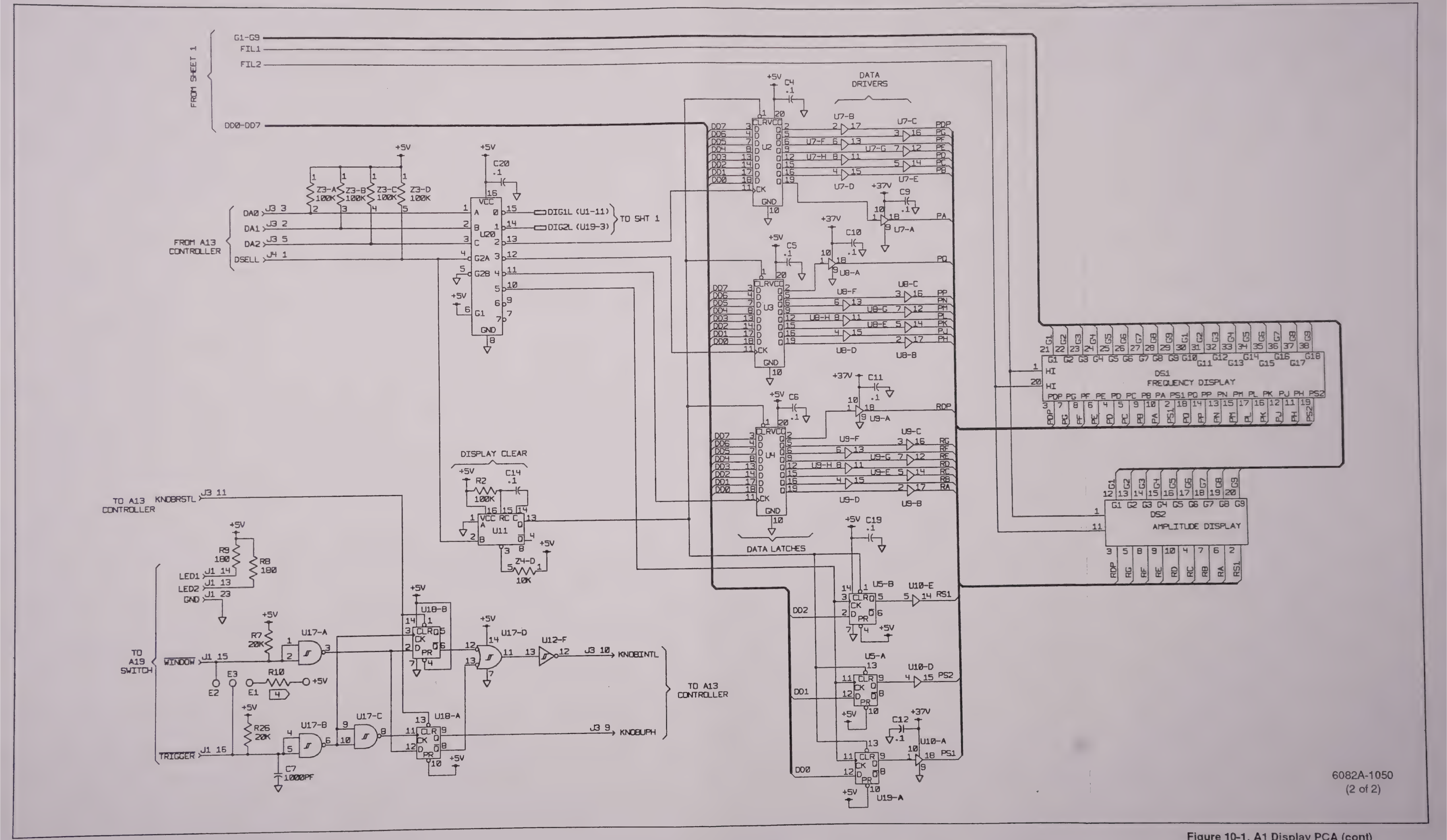

FROM SHEET 1
G1-G9
FIL1
FIL2
DD0-DD7
FROM A13 CONTROLLER
DA0
DA1
DA2
DSELL
Z3-A 100K
Z3-B 100K
Z3-C 100K
Z3-D 100K
+5V
C20 .1
U20
VCC
GND
DIG1L (U1-11)
DIG2L (U19-3)
TO SHT 1
DATA DRIVERS
DATA LATCHES
U2
U3
U4
CLR
VCC
CK
C4 .1
C5 .1
C6 .1
C9 .1
C10 .1
C11 .1
C12 .1
C19 .1
+37V
U7-A
U7-B
U7-C
U7-D
U7-E
U7-F
U7-G
U7-H
U8-A
U8-B
U8-C
U8-D
U8-E
U8-F
U8-G
U8-H
U9-A
U9-B
U9-C
U9-D
U9-E
U9-F
U9-G
U9-H
PDP PG PF PE PD PC PB PA PQ PP PN PM PL PK PJ PH
RDP RG RF RE RD RC RB RA
DS1
FREQUENCY DISPLAY
HI
PS1
PS2
DS2
AMPLITUDE DISPLAY
RS1
DISPLAY CLEAR
R2 100K
C14 .1
U11
Z4-D 10K
TO A13 CONTROLLER
KNOBRSTL
R9 180
R8 180
LED1
LED2
GND
TO A19 SWITCH
WINDOW
TRIGGER
R7 20K
R10
E1
E2
E3
R26 20K
C7 1000PF
U17-A
U17-B
U17-C
U17-D
U18-A
U18-B
U12-F
KNOBINTL
KNOBUPH
U5-A
U5-B
U10-A
U10-D
U10-E
U19-A
DD0
DD1
DD2
6082A-1050
(2 of 2)

Figure 10-1. A1 Display PCA (cont)

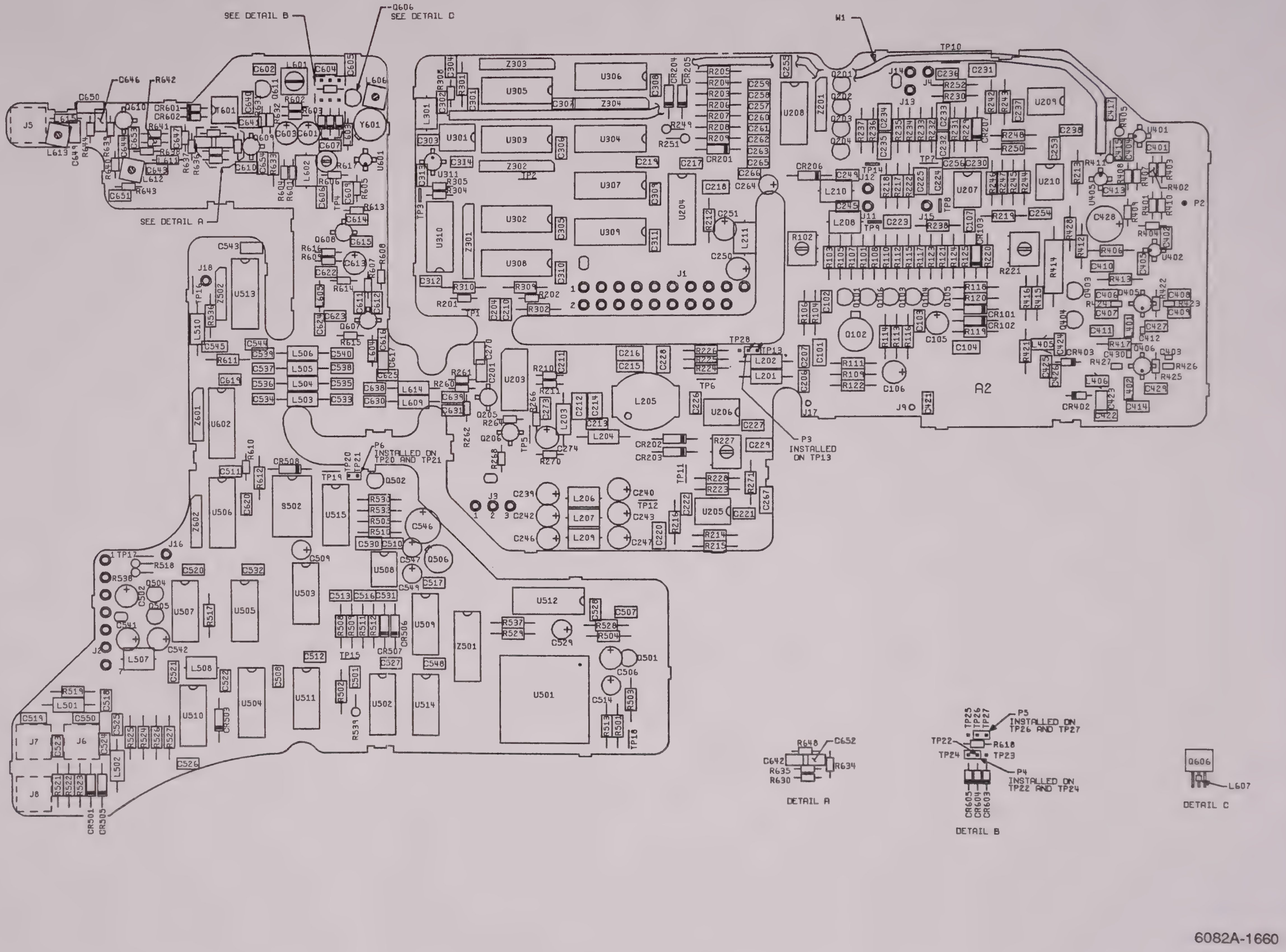

SEE DETAIL B
Q606
SEE DETAIL C
SEE DETAIL A
W1
TP10
J5
J1
J3
J6
J7
J8
J9
A2
P6
INSTALLED ON
TP20 AND TP21
P3
INSTALLED
ON TP13
P5
INSTALLED ON
TP26 AND TP27
P4
INSTALLED ON
TP22 AND TP24
DETAIL A
DETAIL B
DETAIL C
L607
6082A-1660

Figure 10-2. A2 Coarse Loop PCA

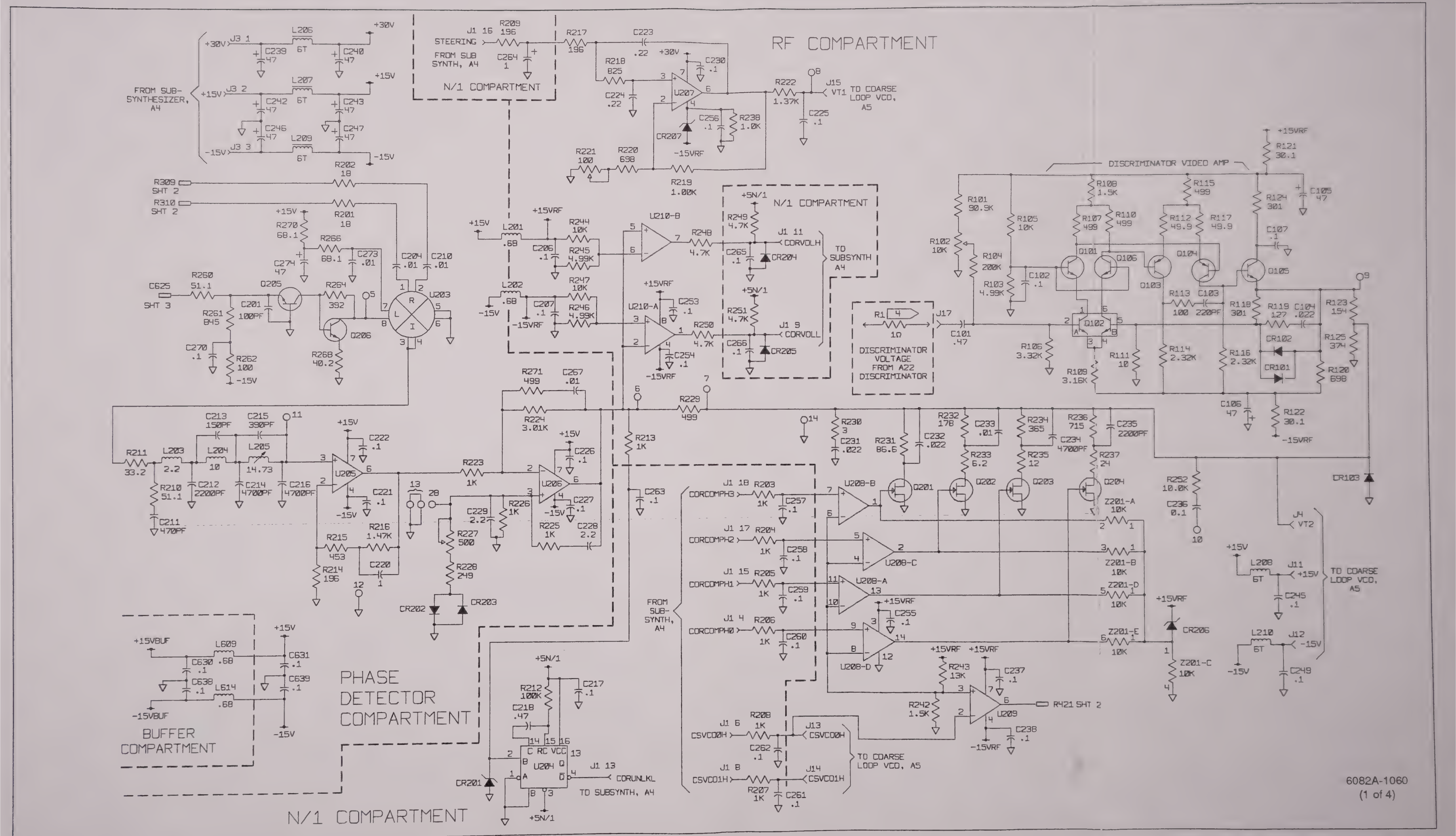

RF COMPARTMENT
N/1 COMPARTMENT
PHASE DETECTOR COMPARTMENT
BUFFER COMPARTMENT
DISCRIMINATOR VIDEO AMP
FROM SUB-SYNTHESIZER, A4
STEERING FROM SUB SYNTH, A4
TO COARSE LOOP VCO, A5
TO SUBSYNTH A4
DISCRIMINATOR VOLTAGE FROM A22 DISCRIMINATOR
FROM SUB-SYNTH, A4
TO SUBSYNTH, A4
R309 SHT 2
R310 SHT 2
C625 SHT 3
R421 SHT 2
CORVOLH
CORVOLL
CORUNLKL
CORCOMPH3
CORCOMPH2
CORCOMPH1
CORCOMPH0
CSVCO0H
CSVCO1H
VT1
VT2
U203
U204
U205
U206
U207
U208-A
U208-B
U208-C
U208-D
U209
U210-A
U210-B
Q101
Q102
Q103
Q104
Q105
Q106
Q201
Q202
Q203
Q204
Q205
Q206
+30V
+15V
-15V
+15VRF
-15VRF
+5N/1
+15VBUF
-15VBUF
6082A-1060
(1 of 4)

Figure 10-2. A2 Coarse Loop PCA (cont)

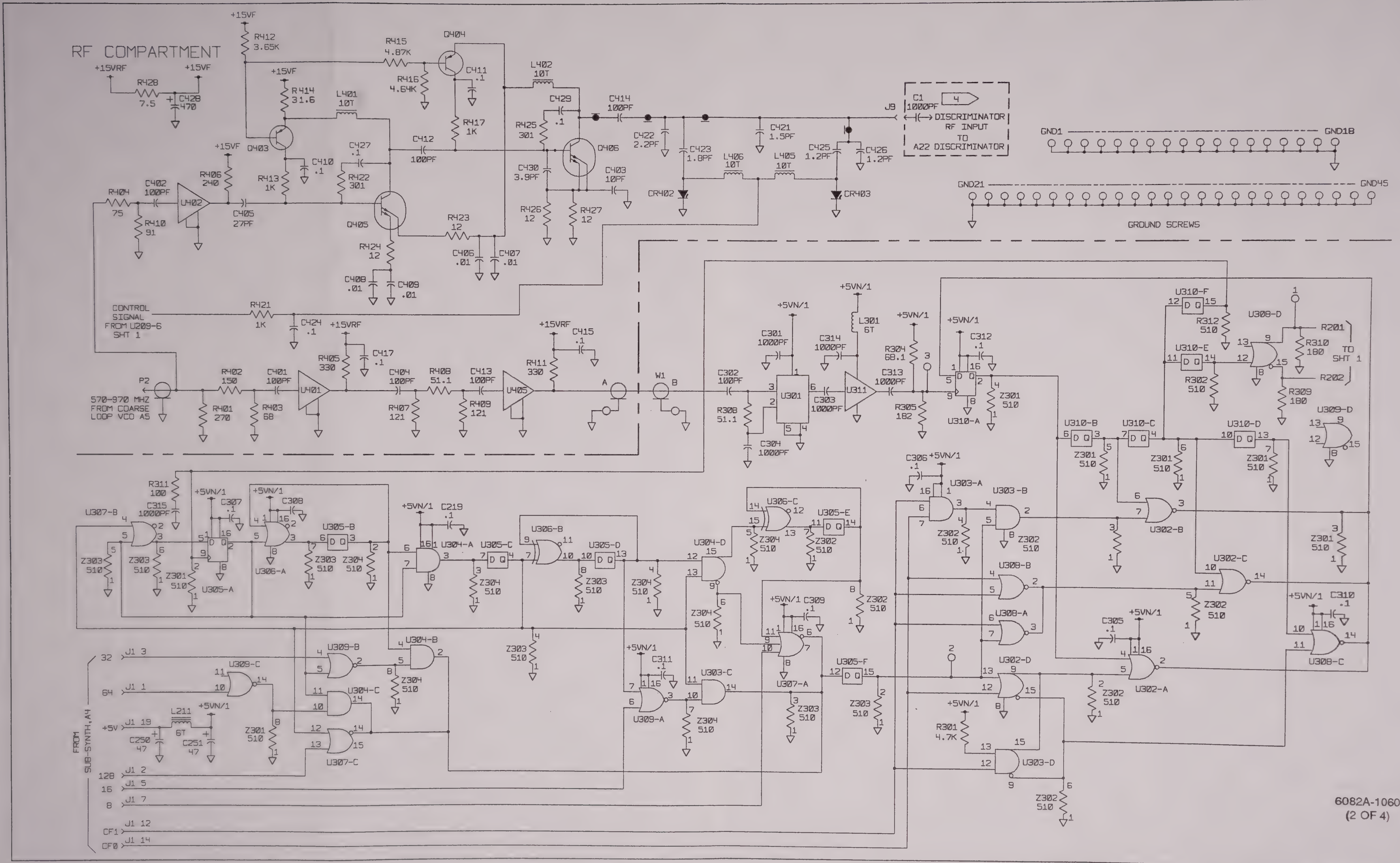

RF COMPARTMENT
+15VRF
+15VF
R428 7.5
C428 470
R412 3.65K
R414 31.6
L401 10T
R415 4.87K
Q404
R416 4.64K
C411 .1
R417 1K
L402 10T
C429 .1
C414 100PF
R425 301
Q406
C403 10PF
C422 2.2PF
C423 1.8PF
C421 1.5PF
C425 1.2PF
C426 1.2PF
L406 10T
L405 10T
CR402
CR403
J9
C1 1000PF
4
DISCRIMINATOR RF INPUT TO A22 DISCRIMINATOR
GND1
GND18
GND21
GND45
GROUND SCREWS
Q403
C410 .1
C427 .1
C412 100PF
R422 301
R413 1K
R406 240
R404 75
C402 100PF
U402
R410 91
C405 27PF
Q405
R423 12
R424 12
C406 .01
C407 .01
C408 .01
C409 .01
C430 3.9PF
R426 12
R427 12
CONTROL SIGNAL FROM U209-6 SHT 1
R421 1K
C424 .1
P2
570-970 MHZ FROM COARSE LOOP VCO A5
R402 150
R401 270
R403 68
C401 100PF
U401
R405 330
C417 .1
C404 100PF
R407 121
R408 51.1
C413 100PF
R409 121
U405
R411 330
C415 .1
A
W1
B
C302 100PF
R308 51.1
C304 1000PF
C301 1000PF
+5VN/1
U301
C303 1000PF
C314 1000PF
L301 6T
U311
C313 1000PF
R304 68.1
R305 182
3
C312 .1
U310-A
Z301 510
U310-F
R312 510
U310-E
R302 510
U308-D
R310 180
R309 180
R201
R202
TO SHT 1
1
U310-B
U310-C
U310-D
U309-D
R311 100
C315 1000PF
U307-B
C307 .1
C308
U306-A
U305-A
U305-B
Z303 510
Z304 510
C219 .1
U304-A
U305-C
U306-B
U305-D
U304-D
U306-C
U305-E
Z302 510
C306 .1
U303-A
U303-B
U302-B
U308-B
U302-C
U308-A
C305 .1
C310 .1
U308-C
U302-D
U302-A
U303-D
R301 4.7K
2
U305-F
U307-A
C309 .1
C311 .1
U303-C
U309-A
U304-B
U309-B
U309-C
U304-C
U307-C
L211 6T
C250 47
C251 47
FROM SUB-SYNTH, A4
32 J1 3
64 J1 1
+5V J1 19
128 J1 2
16 J1 5
8 J1 7
CF1 J1 12
CF0 J1 14
6082A-1060 (2 OF 4)

Figure 10-2. A2 Coarse Loop PCA (cont)

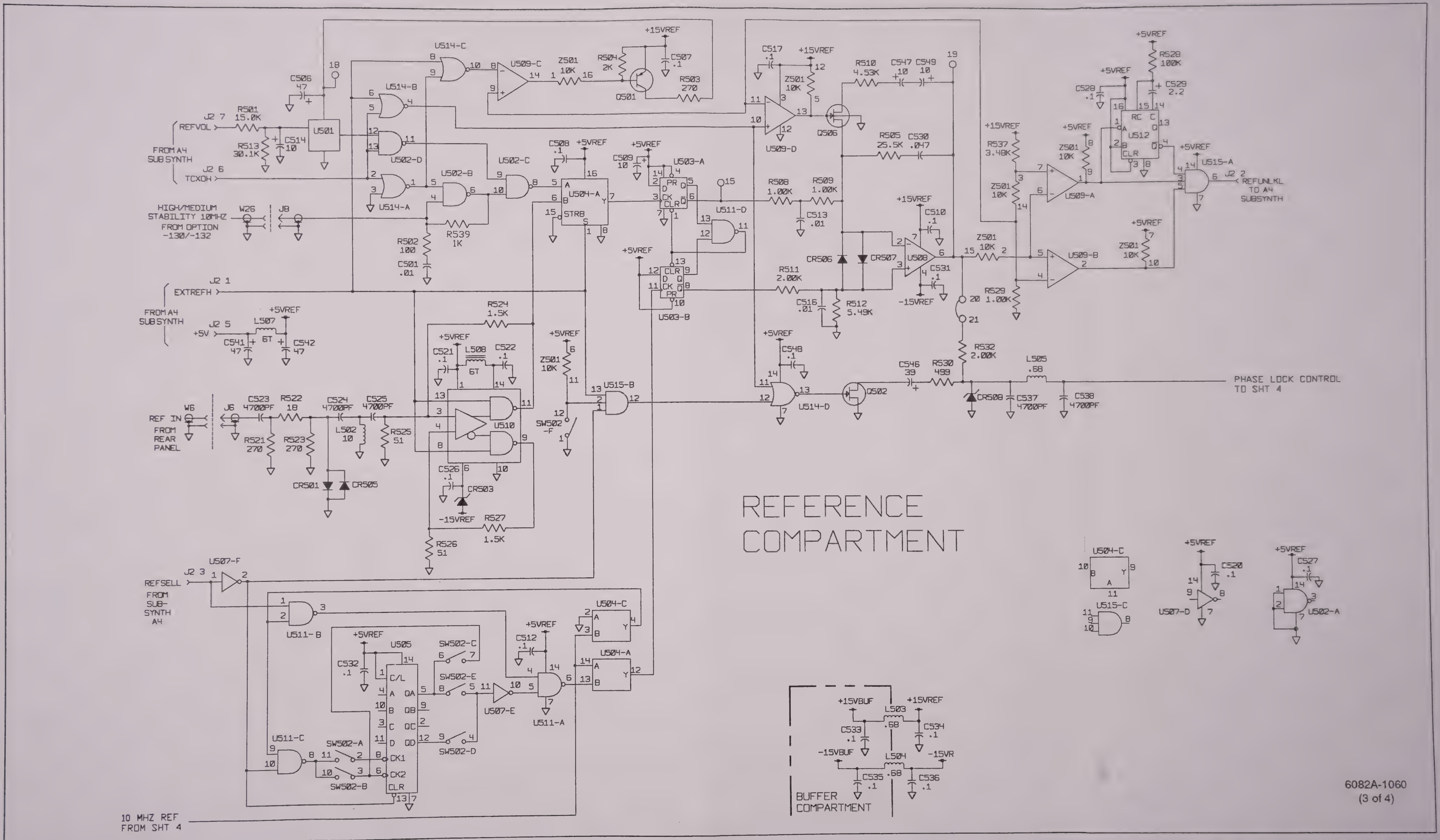
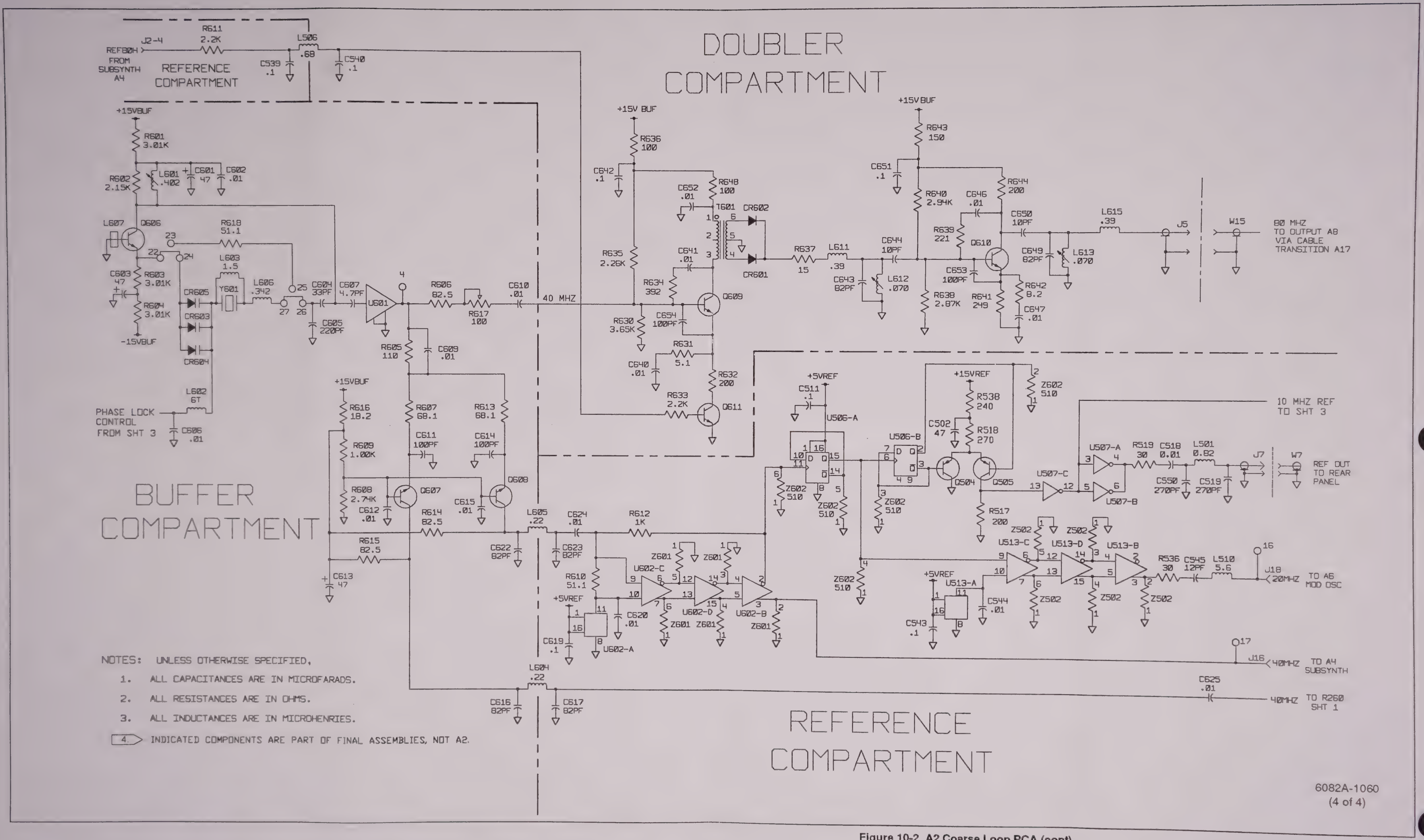

REFERENCE COMPARTMENT
BUFFER COMPARTMENT
REFVOL
J2 7
FROM A4 SUBSYNTH
J2 6
TCXOH
HIGH/MEDIUM STABILITY 10MHZ FROM OPTION -130/-132
W26
J8
J2 1
EXTREFH
FROM A4 SUBSYNTH
J2 5
+5V
REF IN FROM REAR PANEL
W6
J6
J2 3
REFSELL FROM SUB-SYNTH A4
10 MHZ REF FROM SHT 4
J2 2
REFUNLKL TO A4 SUBSYNTH
PHASE LOCK CONTROL TO SHT 4
R501 15.0K
R513 30.1K
C514 10
C506 47
U501
U514-C
U514-B
U514-A
U509-C
Z501 10K
R504 2K
Q501
C507 .1
R503 270
+15VREF
+5VREF
-15VREF
U502-D
U502-B
U502-C
U504-A
STRB
R502 100
C501 .01
R539 1K
C508 .1
C509 10
U503-A
U503-B
U511-D
C517 .1
U509-D
Q506
R510 4.53K
C547 10
C549 10
R505 25.5K
C530 .047
R508 1.00K
R509 1.00K
C513 .01
R511 2.00K
C516 .01
R512 5.49K
CR506
CR507
U508
C510 .1
C531 .1
R537 3.48K
R529 1.00K
U509-A
U509-B
R528 100K
C528 .1
C529 2.2
U512
U515-A
R524 1.5K
L507 6T
C541 47
C542 47
C521 .1
L508 6T
C522 .1
U510
C523 4700PF
R522 18
C524 4700PF
C525 4700PF
R521 270
R523 270
L502 10
R525 51
CR501
CR505
C526 .1
CR503
R527 1.5K
R526 51
U515-B
SW502-F
C548 .1
U514-D
Q502
C546 39
R530 499
R532 2.00K
L505 .68
CR508
C537 4700PF
C538 4700PF
U507-F
U511-B
U505
C532 .1
SW502-C
SW502-E
SW502-D
SW502-A
SW502-B
U511-C
U507-E
U511-A
C512 .1
U504-C
U504-A
U515-C
U507-D
C520 .1
C527 .1
U502-A
+15VBUF
-15VBUF
-15VR
L503 .68
L504 .68
C533 .1
C534 .1
C535 .1
C536 .1
6082A-1060
(3 of 4)

Figure 10-2. A2 Coarse Loop PCA (cont)

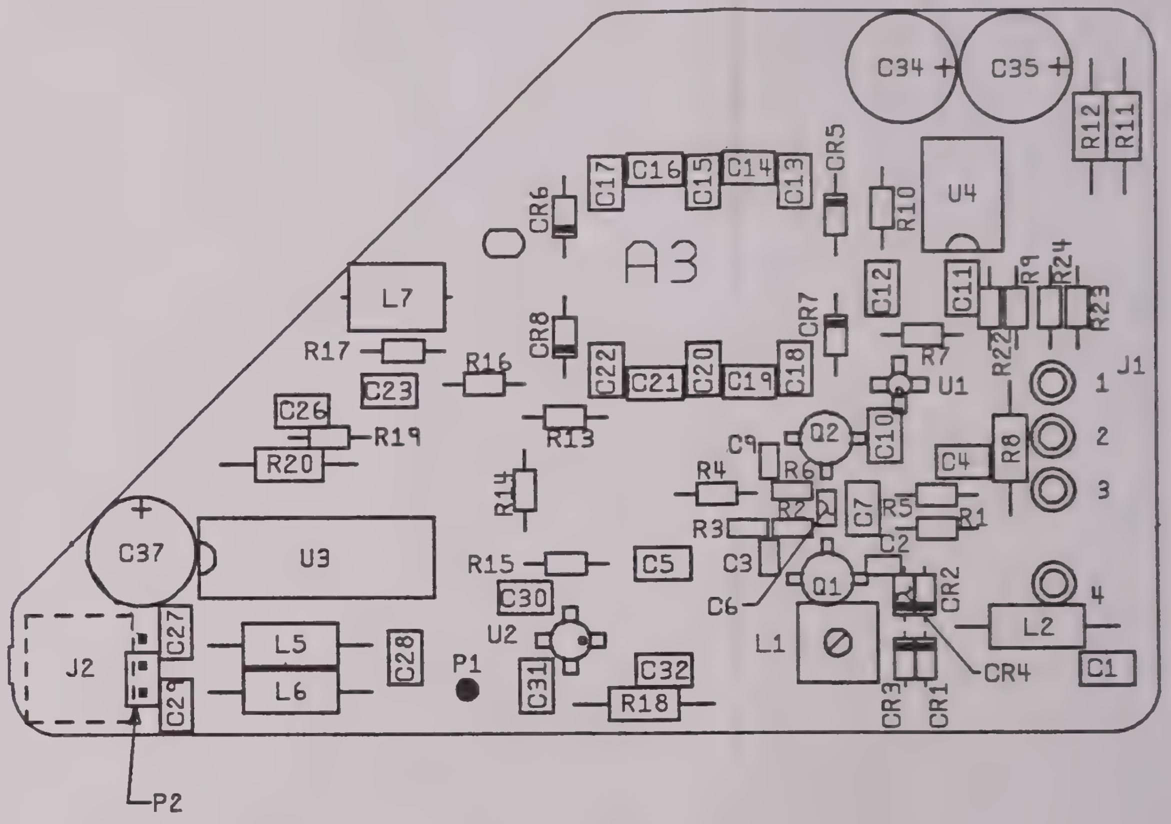

DOUBLER
COMPARTMENT
REFERENCE
COMPARTMENT
BUFFER
COMPARTMENT
REFERENCE
COMPARTMENT
REF80H
FROM
SUBSYNTH
A4
J2-4
R611
2.2K
L506
.68
C539
.1
C540
.1
+15VBUF
R601
3.01K
R602
2.15K
L601
.402
C601
47
C602
.01
L607
Q606
R618
51.1
23
22
24
C603
47
R603
3.01K
R604
3.01K
-15VBUF
L603
1.5
CR605
Y601
L606
.342
CR603
CR604
25
27
26
C604
33PF
C605
220PF
C607
4.7PF
U601
4
R606
82.5
R617
100
C610
.01
40 MHZ
R605
110
C609
.01
L602
6T
PHASE LOCK
CONTROL
FROM SHT 3
C606
.01
+15VBUF
R616
18.2
R609
1.00K
R607
68.1
R613
68.1
C611
100PF
C614
100PF
R608
2.74K
Q607
Q608
C612
.01
R614
82.5
C615
.01
R615
82.5
C613
47
L605
.22
C622
82PF
C624
.01
C623
82PF
R612
1K
R610
51.1
+5VREF
C619
.1
U602-A
C620
.01
Z601
U602-C
U602-D
U602-B
L604
.22
C616
82PF
C617
82PF
+15V BUF
R636
100
C642
.1
R648
100
C652
.01
T601
CR602
CR601
R635
2.26K
C641
.01
R634
392
Q609
R630
3.65K
C654
100PF
R631
5.1
C640
.01
R632
200
R633
2.2K
Q611
R637
15
L611
.39
C643
82PF
L612
.070
C644
10PF
+15VBUF
R643
150
C651
.1
R640
2.94K
C646
.01
R644
200
R639
221
C650
10PF
Q610
C653
100PF
R638
2.87K
R641
249
R642
8.2
C647
.01
C649
82PF
L613
.070
L615
.39
J5
W15
80 MHZ
TO OUTPUT A8
VIA CABLE
TRANSITION A17
+5VREF
C511
.1
U506-A
+15VREF
R538
240
C502
47
R518
270
Z602
510
U506-B
Q504
Q505
R517
200
10 MHZ REF
TO SHT 3
U507-A
R519
30
C518
0.01
L501
0.82
J7
W7
REF OUT
TO REAR
PANEL
U507-C
U507-B
C550
270PF
C519
270PF
Z502
U513-C
U513-D
U513-B
U513-A
C544
.01
C543
.1
R536
30
C545
12PF
L510
5.6
16
J18
20MHZ
TO A6
MOD OSC
17
J16
40MHZ
TO A4
SUBSYNTH
C625
.01
40MHZ
TO R260
SHT 1
6082A-1060
(4 of 4)

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTANCES ARE IN OHMS.
3. ALL INDUCTANCES ARE IN MICROHENRIES.

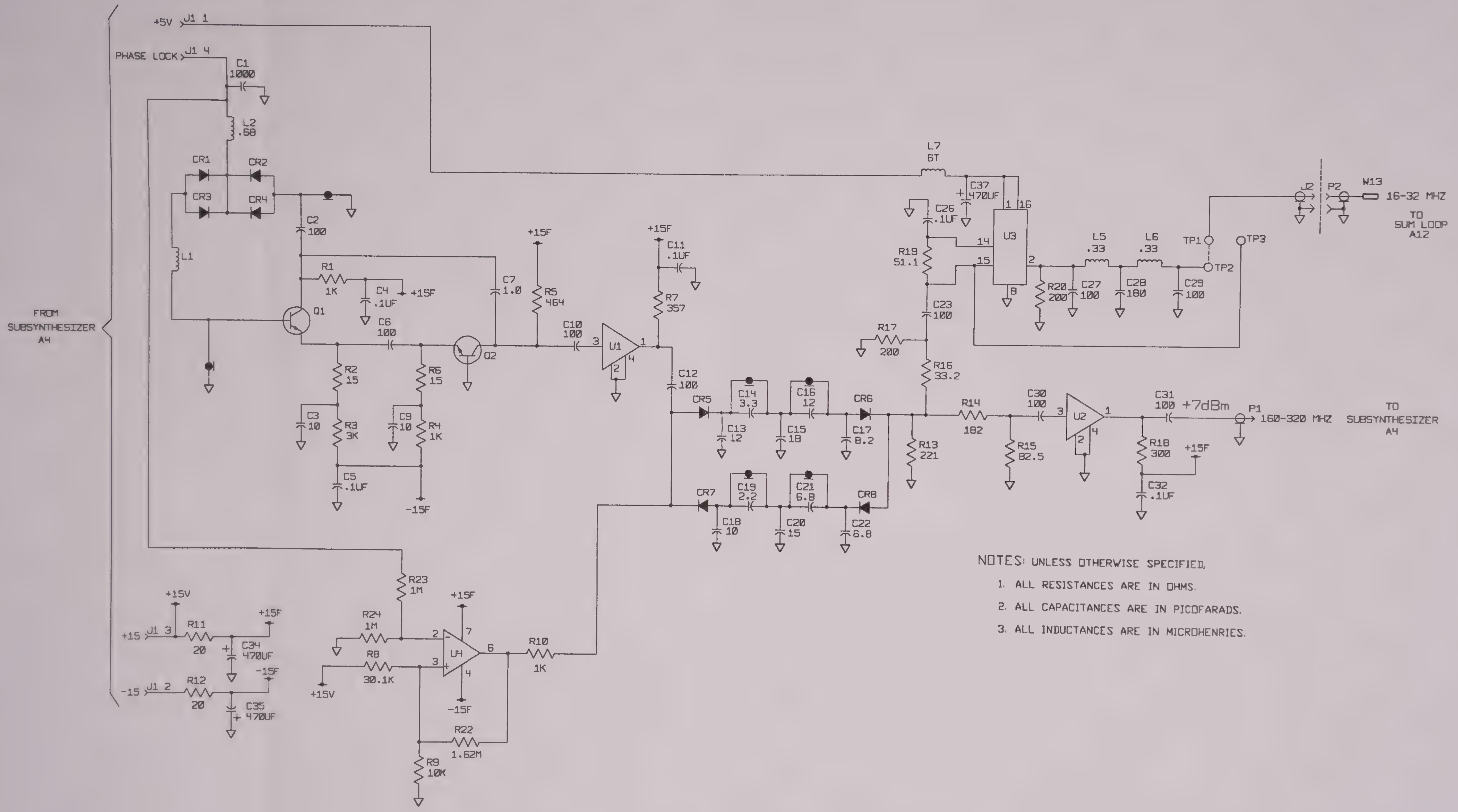
4. INDICATED COMPONENTS ARE PART OF FINAL ASSEMBLIES, NOT A2.

Figure 10-2. A2 Coarse Loop PCA (cont)


C34
C35
R12
R11
U4
CR5
R10
C17
C16
C15
C14
C13
CR6
A3
L7
CR8
CR7
C12
C11
R9
R24
R23
R22
J1
1
2
3
4
R17
R16
C22
C21
C20
C19
C18
R7
U1
C23
C26
R19
R13
C9
Q2
C10
C4
R8
R20
R4
R6
R14
R2
C7
R5
R1
R3
C2
C37
U3
R15
C5
C3
Q1
CR2
C30
C6
U2
L1
L2
J2
C27
L5
C28
P1
C32
CR4
C1
C29
L6
C31
R18
CR3
CR1
P2

6082A-1661

Figure 10-3. A3 Subsynthesizer VCO PCA


+5V J1 1
PHASE LOCK J1 4
C1 1000
L2 .68
CR1
CR2
CR3
CR4
C2 100
L1
R1 1K
C4 .1UF
+15F
C7 1.0
+15F
R5 464
Q1
C6 100
Q2
FROM SUBSYNTHESIZER A4
R2 15
R6 15
C3 10
R3 3K
C9 10
R4 1K
C5 .1UF
-15F
+15F
C11 .1UF
R7 357
C10 100
3
U1
1
2
4
C12 100
CR5
C14 3.3
C16 12
CR6
C13 12
C15 18
C17 8.2
CR7
C19 2.2
C21 6.8
CR8
C18 10
C20 15
C22 6.8
L7 6T
C37 470UF
C26 .1UF
1
16
U3
14
15
2
8
R19 51.1
C23 100
R17 200
R16 33.2
R20 200
C27 100
L5 .33
L6 .33
C28 180
C29 100
TP1
TP2
TP3
J2
P2
W13
16-32 MHZ
TO SUM LOOP A12
R13 221
R14 182
R15 82.5
C30 100
3
U2
1
2
4
C31 100 +7dBm
P1
160-320 MHZ
TO SUBSYNTHESIZER A4
R18 300
+15F
C32 .1UF
R23 1M
+15V
+15 J1 3
R11 20
+15F
C34 470UF
-15 J1 2
R12 20
-15F
C35 470UF
R24 1M
+15F
2
7
U4
6
R8 30.1K
3
4
+15V
-15F
R10 1K
R22 1.62M
R9 10K

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES ARE IN OHMS.
2. ALL CAPACITANCES ARE IN PICOFARADS.
3. ALL INDUCTANCES ARE IN MICROHENRIES.

6082A-1061

Figure 10-3. A3 Subsynthesizer VCO PCA (cont)

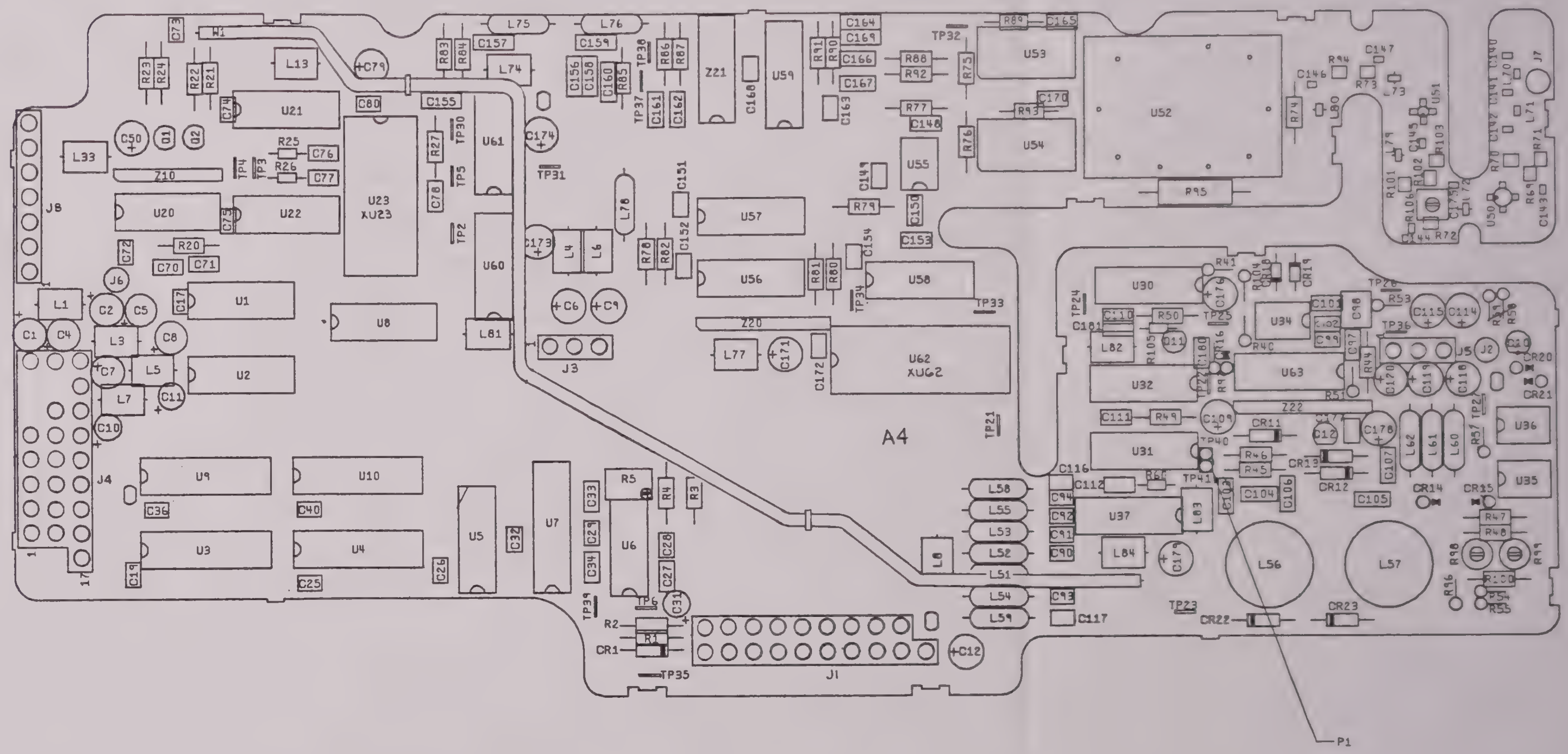
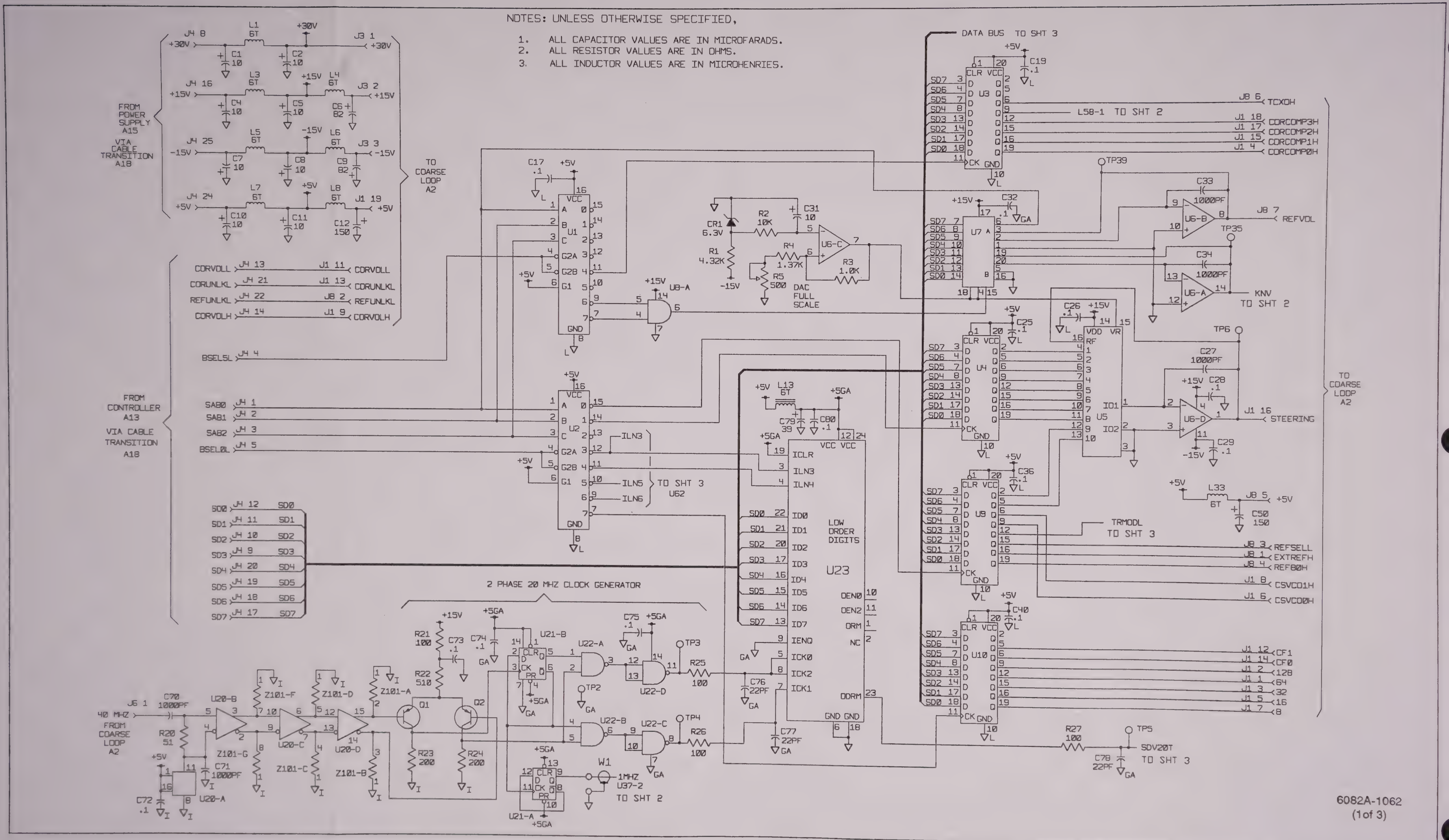

A4
J8
J4
J1
J3
J5
J6
J7
P1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U20
U21
U22
U23
XU23
U30
U31
U32
U34
U35
U36
U37
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
XU62
U63
Z10
Z20
Z21
Z22
L1
L3
L4
L5
L6
L7
L13
L33
L51
L52
L53
L54
L55
L56
L57
L58
L59
L60
L61
L62
L74
L75
L76
L77
L78
L81
L82
L83
L84
TP2
TP3
TP4
TP5
TP6
TP21
TP22
TP23
TP24
TP25
TP26
TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39
TP40
TP41
CR1
CR11
CR12
CR13
CR14
CR15
CR19
CR20
CR21
CR22
CR23
R1
R2
R3
R4
R5
R20
R21
R22
R23
R24
R25
R26
R27
R45
R46
R47
R48
R49
R50
R53
R72
R73
R74
R75
R76
R77
R78
R79
R80
R81
R82
R83
R84
R85
R86
R87
R88
R89
R90
R91
R92
R93
R94
R95
R96
R98
R99
R100
R101
R102
R103
R105
R106
C1
C2
C4
C5
C6
C7
C8
C9
C10
C11
C12
C17
C19
C25
C26
C27
C28
C29
C31
C32
C33
C34
C36
C40
C50
C70
C71
C72
C73
C74
C75
C76
C77
C78
C79
C80
C90
C91
C92
C93
C94
C104
C105
C106
C107
C111
C112
C114
C115
C116
C117
C146
C147
C148
C149
C150
C151
C152
C153
C154
C155
C156
C157
C158
C159
C160
C161
C162
C163
C164
C165
C166
C167
C168
C169
C170
C171
C172
C173
C174
C175
C176
C177
C178
Q1
Q2
W1
1
17
6082A-1662

Figure 10-4. A4 Subsynthesizer PCA


NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

FROM POWER SUPPLY A15 VIA CABLE TRANSITION A18
J4 8 +30V
J4 16 +15V
J4 25 -15V
J4 24 +5V
L1 6T
L3 6T
L4 6T
L5 6T
L6 6T
L7 6T
L8 6T
C1 10
C2 10
C4 10
C5 10
C6 82
C7 10
C8 10
C9 82
C10 10
C11 10
C12 150
J3 1 +30V
J3 2 +15V
J3 3 -15V
J1 19 +5V
TO COARSE LOOP A2
CORVOLL J4 13 J1 11 CORVOLL
CORUNLKL J4 21 J1 13 CORUNLKL
REFUNLKL J4 22 J8 2 REFUNLKL
CORVOLH J4 14 J1 9 CORVOLH
BSEL5L J4 4
FROM CONTROLLER A13 VIA CABLE TRANSITION A18
SAB0 J4 1
SAB1 J4 2
SAB2 J4 3
BSEL0L J4 5
SD0 J4 12
SD1 J4 11
SD2 J4 10
SD3 J4 9
SD4 J4 20
SD5 J4 19
SD6 J4 18
SD7 J4 17
C17 .1
U1
U2
U8-A
ILN3
ILN5
ILN6
TO SHT 3 U62
CR1 6.3V
R1 4.32K
R2 10K
R3 1.0K
R4 1.37K
R5 500
C31 10
U6-C
DAC FULL SCALE
DATA BUS TO SHT 3
U3
C19 .1
L58-1 TO SHT 2
J8 6 TCXOH
J1 18 CORCOMP3H
J1 17 CORCOMP2H
J1 15 CORCOMP1H
J1 4 CORCOMP0H
TP39
U7
C32 .1
C33 1000PF
U6-B
J8 7 REFVOL
TP35
C34 1000PF
U6-A
KNV TO SHT 2
U4
C25 .1
C26 .1
U5
TP6
C27 1000PF
C28 .1
U6-D
C29 .1
J1 16 STEERING
TO COARSE LOOP A2
L13 6T
C79 39
C80 .1
U23
LOW ORDER DIGITS
U9
C36 .1
L33 6T
J8 5 +5V
C50 150
TRMODL TO SHT 3
J8 3 REFSELL
J8 1 EXTREFH
J8 4 REF80H
J1 8 CSVCO1H
J1 6 CSVCO0H
U10
C40 .1
J1 12 CF1
J1 14 CF0
J1 2 128
J1 1 64
J1 3 32
J1 5 16
J1 7 8
R27 100
TP5
C78 22PF
SDV20T TO SHT 3
2 PHASE 20 MHZ CLOCK GENERATOR
J6 1 40 MHZ FROM COARSE LOOP A2
C70 1000PF
R20 51
C71 1000PF
C72 .1
U20-A
U20-B
U20-C
U20-D
Z101-A
Z101-B
Z101-C
Z101-D
Z101-F
Z101-G
R21 100
R22 510
R23 200
R24 200
C73 .1
C74 .1
Q1
Q2
U21-A
U21-B
U22-A
U22-B
U22-C
U22-D
C75 .1
TP2
TP3
TP4
R25 100
R26 100
C76 22PF
C77 22PF
W1
1MHZ U37-2 TO SHT 2

6082A-1062
(1of 3)

Figure 10-4. A4 Subsynthesizer PCA (cont)

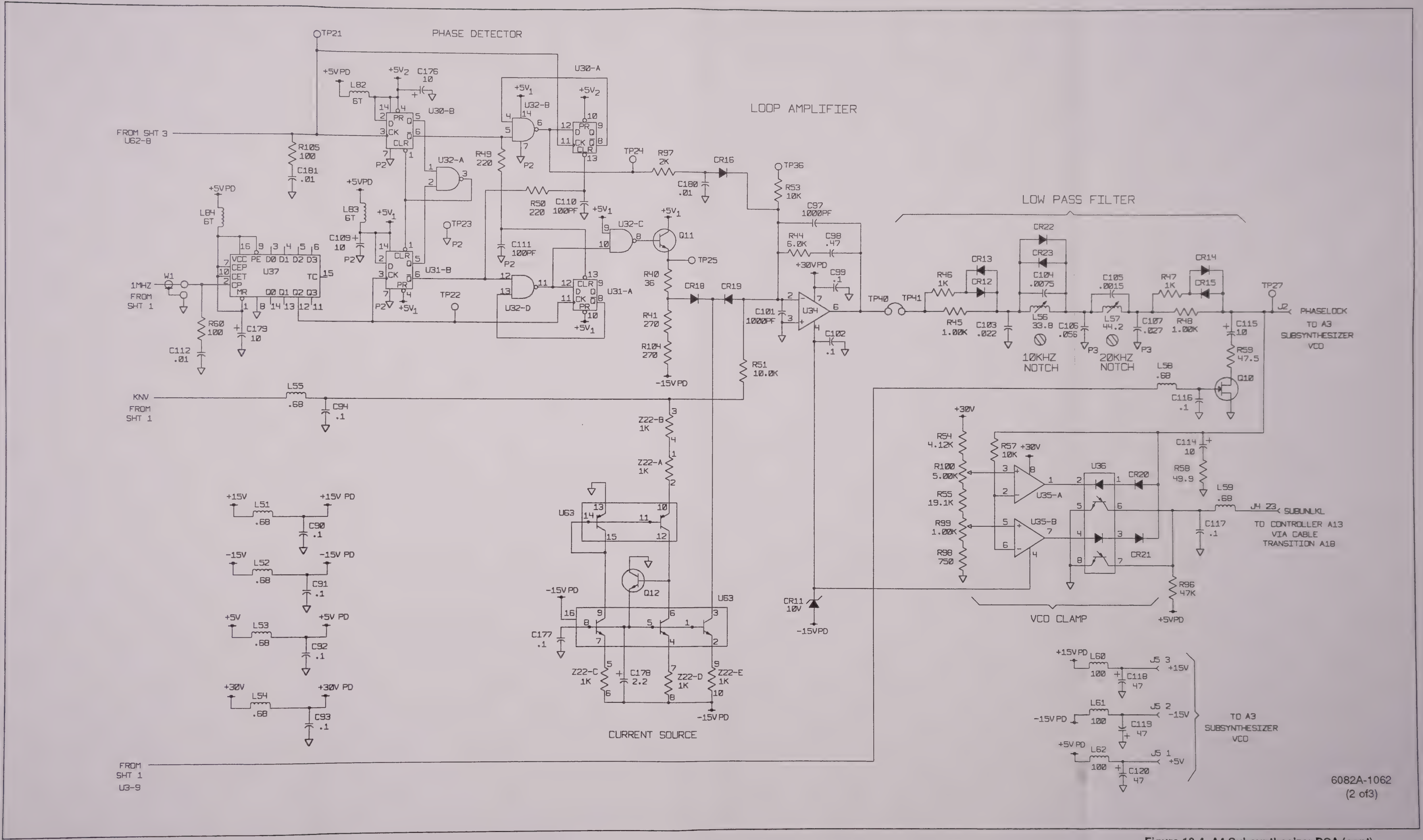

PHASE DETECTOR
TP21
U30-A
U30-B
U32-B
U32-A
U32-C
U32-D
U31-A
U31-B
U37
+5VPD
L82 6T
+5V2
C176 10
+5V1
FROM SHT 3 U62-8
R105 100
C181 .01
R49 220
R50 220
C110 100PF
C109 10
L83 6T
L84 6T
TP23
TP22
C111 100PF
P2
VCC PE D0 D1 D2 D3
CEP
CET
CP
MR Q0 Q1 Q2 Q3
TC
PR D CK Q CLR
1MHZ FROM SHT 1
W1
R60 100
C179 10
C112 .01
KNV FROM SHT 1
L55 .68
C94 .1
LOOP AMPLIFIER
TP24
R97 2K
CR16
C180 .01
TP36
R53 10K
C97 1000PF
R44 6.0K
C98 .47
+30VPD
C99 .1
Q11
TP25
R40 36
R41 270
R104 270
-15VPD
CR18
CR19
C101 1000PF
U34
C102 .1
R51 10.0K
CR11 10V
TP40
TP41
LOW PASS FILTER
R46 1K
CR13
CR12
R45 1.00K
C103 .022
CR22
CR23
C104 .0075
L56 33.8
C106 .056
10KHZ NOTCH
C105 .0015
L57 44.2
C107 .027
20KHZ NOTCH
P3
R47 1K
CR14
CR15
R48 1.00K
TP27
J2
PHASELOCK TO A3 SUBSYNTHESIZER VCO
C115 10
R59 47.5
L58 .68
Q10
C116 .1
+30V
R54 4.12K
R57 10K
R100 5.00K
R55 19.1K
R99 1.00K
R98 750
U35-A
U35-B
U36
CR20
CR21
C114 10
R58 49.9
L59 .68
J4 23
SUBUNLKL
TO CONTROLLER A13 VIA CABLE TRANSITION A18
C117 .1
R96 47K
+5VPD
VCO CLAMP
Z22-B 1K
Z22-A 1K
U63
Q12
C177 .1
Z22-C 1K
C178 2.2
Z22-D 1K
Z22-E 1K
CURRENT SOURCE
+15V
L51 .68
+15V PD
C90 .1
-15V
L52 .68
-15V PD
C91 .1
+5V
L53 .68
+5V PD
C92 .1
+30V
L54 .68
+30V PD
C93 .1
FROM SHT 1 U3-9
+15VPD
L60 100
C118 47
J5 3 +15V
L61 100
C119 47
J5 2 -15V
L62 100
C120 47
J5 1 +5V
TO A3 SUBSYNTHESIZER VCO
6082A-1062 (2 of3)

Figure 10-4. A4 Subsynthesizer PCA (cont)

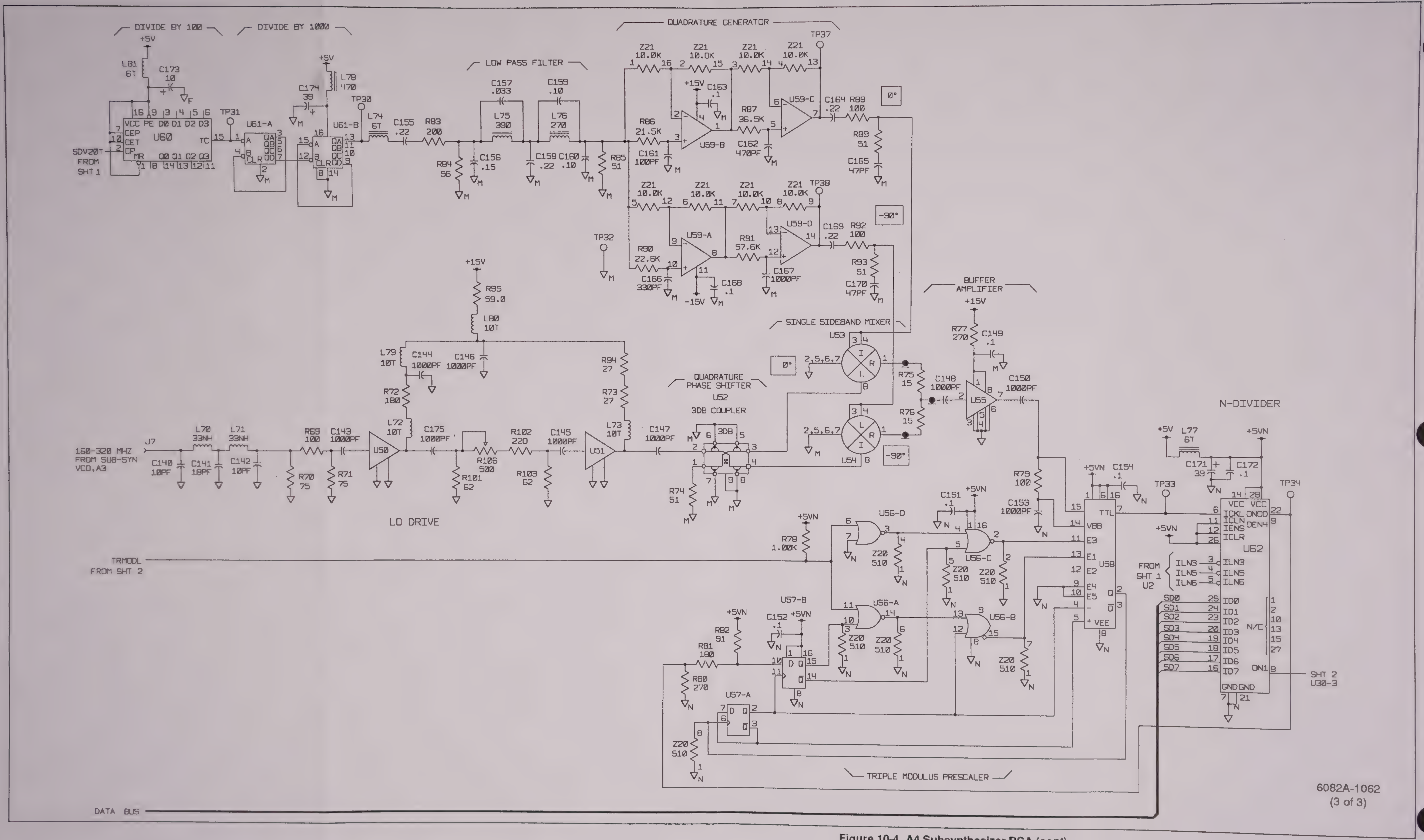
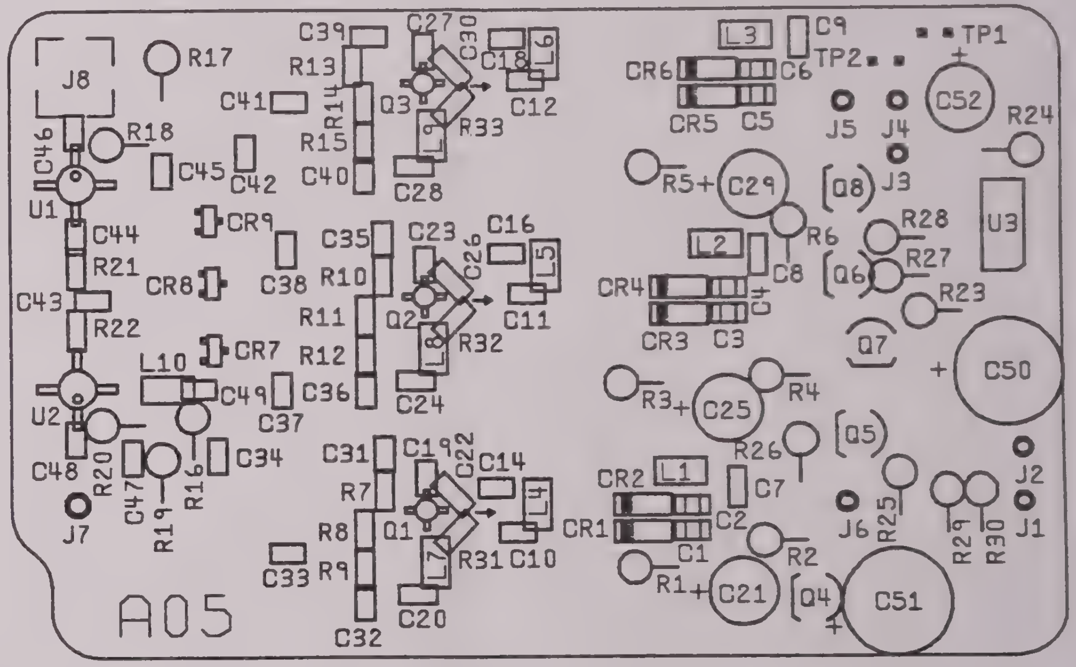
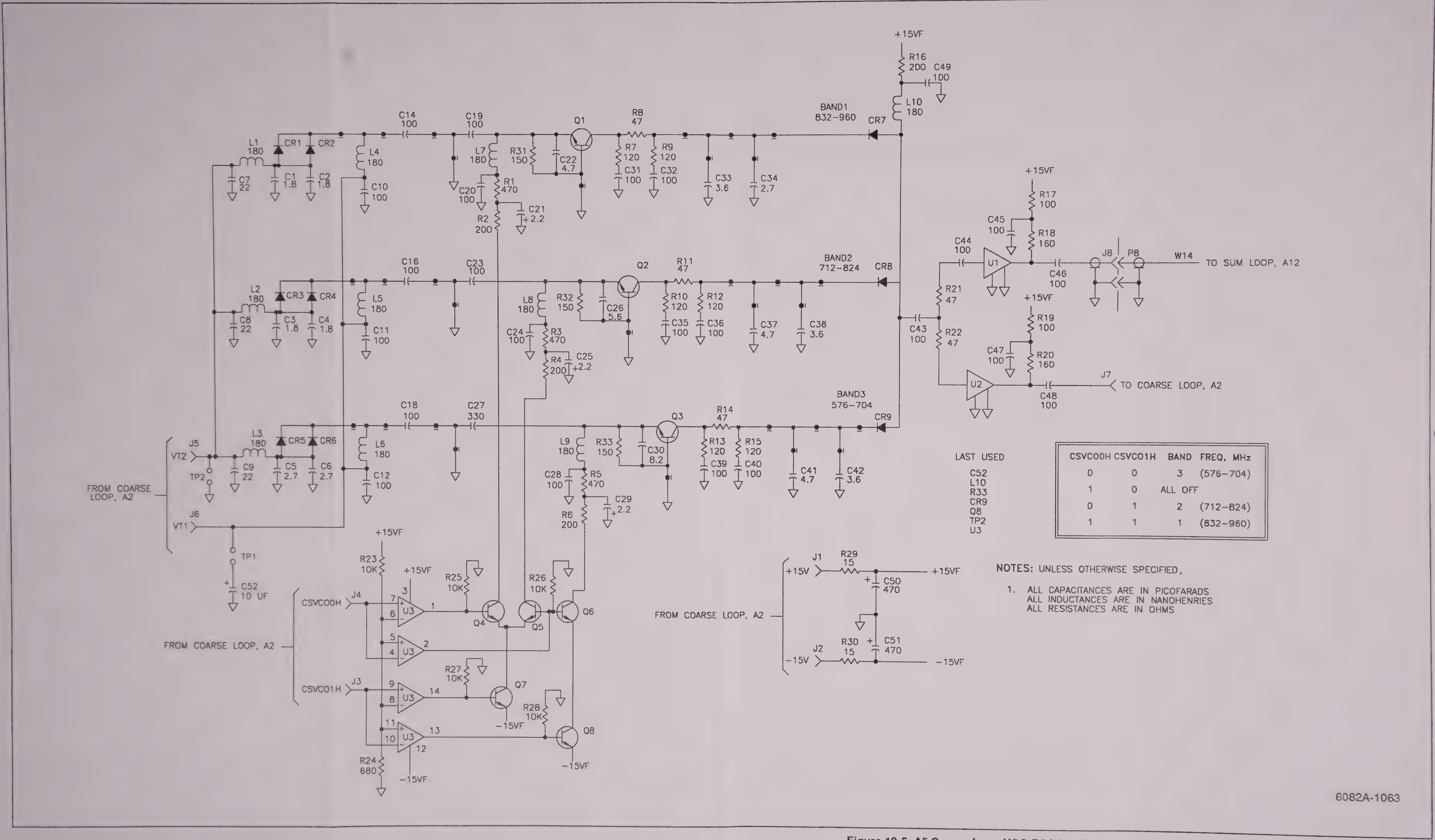

DIVIDE BY 100
DIVIDE BY 1000
LOW PASS FILTER
QUADRATURE GENERATOR
SDV20T FROM SHT 1
U60
U61-A
U61-B
TP30
TP31
TP32
TP37
TP38
U59-A
U59-B
U59-C
U59-D
0°
-90°
SINGLE SIDEBAND MIXER
U53
U54
BUFFER AMPLIFIER
U55
QUADRATURE PHASE SHIFTER
U52
3DB COUPLER
LO DRIVE
J7
160-320 MHZ FROM SUB-SYN VCO,A3
U50
U51
N-DIVIDER
U62
U58
U56-A
U56-B
U56-C
U56-D
U57-A
U57-B
TRMODL FROM SHT 2
FROM SHT 1 U2
SHT 2 U30-3
TRIPLE MODULUS PRESCALER
DATA BUS
TP33
TP34
6082A-1062
(3 of 3)

Figure 10-4. A4 Subsynthesizer PCA (cont)


J8
R17
C39
R13
C27
C30
C18
L6
C12
Q3
R14
C41
R15
C40
R33
L9
C28
L3
C9
TP1
TP2
CR6
C6
CR5
C5
J5
J4
C52
R24
J3
C46
R18
C45
C42
U1
R5
C29
Q8
R28
U3
CR9
C44
C35
C23
C16
C26
L5
L2
R6
C8
R27
Q6
R21
CR8
C38
R10
Q2
C11
CR4
C4
R23
C43
R11
R32
L8
CR3
C3
Q7
R22
CR7
R12
C50
L10
C49
C36
C24
R3
C25
R4
U2
C37
C31
C19
C22
C14
R26
Q5
J2
C48
R20
C47
C34
R7
L4
CR2
L1
C7
R19
R16
R8
Q1
CR1
C2
J6
R25
R29
R30
J1
J7
C1
R2
C33
R9
R31
C10
L7
R1
C21
Q4
C51
A05
C32
C20

6082A-1663

Figure 10-5. A5 Coarse Loop VCO PCA


+15VF
R16
200
C49
100
L10
180
BAND1
832–960
CR7
C14
100
C19
100
Q1
R8
47
L1
180
CR1
CR2
L4
180
L7
180
R31
150
C22
4.7
R7
120
R9
120
C31
100
C32
100
C33
3.6
C34
2.7
C7
22
C1
1.8
C2
1.8
C10
100
C20
100
R1
470
C21
+2.2
R2
200
+15VF
R17
100
C45
100
R18
160
C44
100
U1
J8
P8
W14
TO SUM LOOP, A12
C46
100
C16
100
C23
100
Q2
R11
47
BAND2
712–824
CR8
L2
180
CR3
CR4
L5
180
L8
180
R32
150
C26
5.6
R10
120
R12
120
C8
22
C3
1.8
C4
1.8
C11
100
C24
100
R3
470
C35
100
C36
100
C37
4.7
C38
3.6
R21
47
+15VF
R19
100
C43
100
R22
47
C47
100
R20
160
R4
200
C25
+2.2
U2
J7
TO COARSE LOOP, A2
C48
100
BAND3
576–704
C18
100
C27
330
Q3
R14
47
CR9
J5
VT2
L3
180
CR5
CR6
L6
180
L9
180
R33
150
C30
8.2
R13
120
R15
120
C39
100
C40
100
C41
4.7
C42
3.6
TP2
C9
22
C5
2.7
C6
2.7
C12
100
C28
100
R5
470
C29
+2.2
FROM COARSE LOOP, A2
J6
VT1
R6
200
TP1
C52
10 UF
+15VF
R23
10K
+15VF
3
R25
10K
R26
10K
CSVCO0H
J4
7
6
U3
1
Q4
Q5
Q6
FROM COARSE LOOP, A2
5
4
U3
2
R27
10K
Q7
CSVCO1H
J3
9
8
U3
14
R28
10K
-15VF
11
10
U3
13
12
Q8
R24
680
-15VF
-15VF
J1
+15V
R29
15
+15VF
C50
470
FROM COARSE LOOP, A2
J2
-15V
R30
15
C51
470
-15VF
6082A-1063

LAST USED

C52
L10
R33
CR9
Q8
TP2
U3

CSVCO0H	CSVCO1H	BAND	FREQ, MHz
0	0	3	(576–704)
1	0	ALL OFF	
0	1	2	(712–824)
1	1	1	(832–960)

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITANCES ARE IN PICOFARADS
   ALL INDUCTANCES ARE IN NANOHENRIES
   ALL RESISTANCES ARE IN OHMS

Figure 10-5. A5 Coarse Loop VCO PCA (cont)

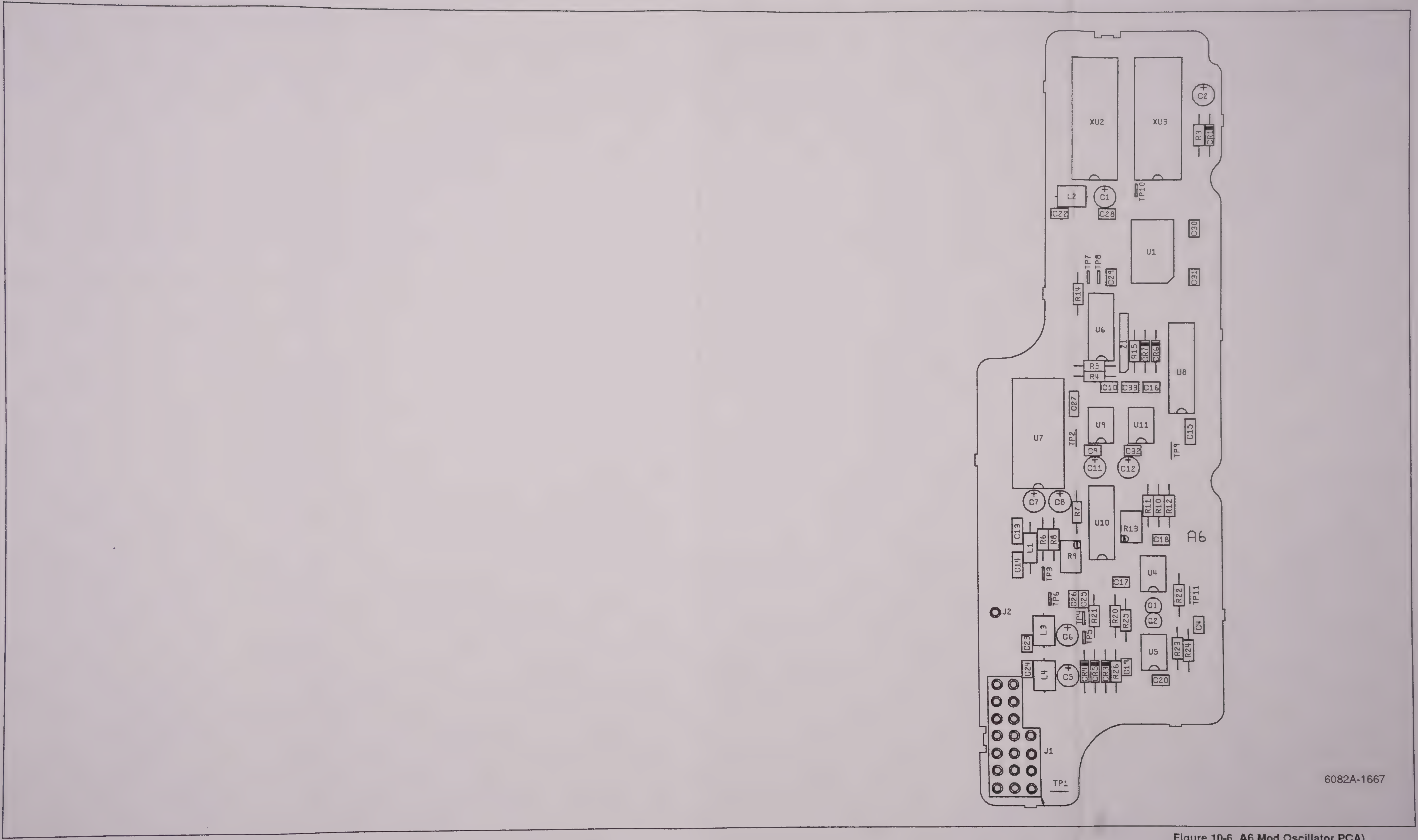
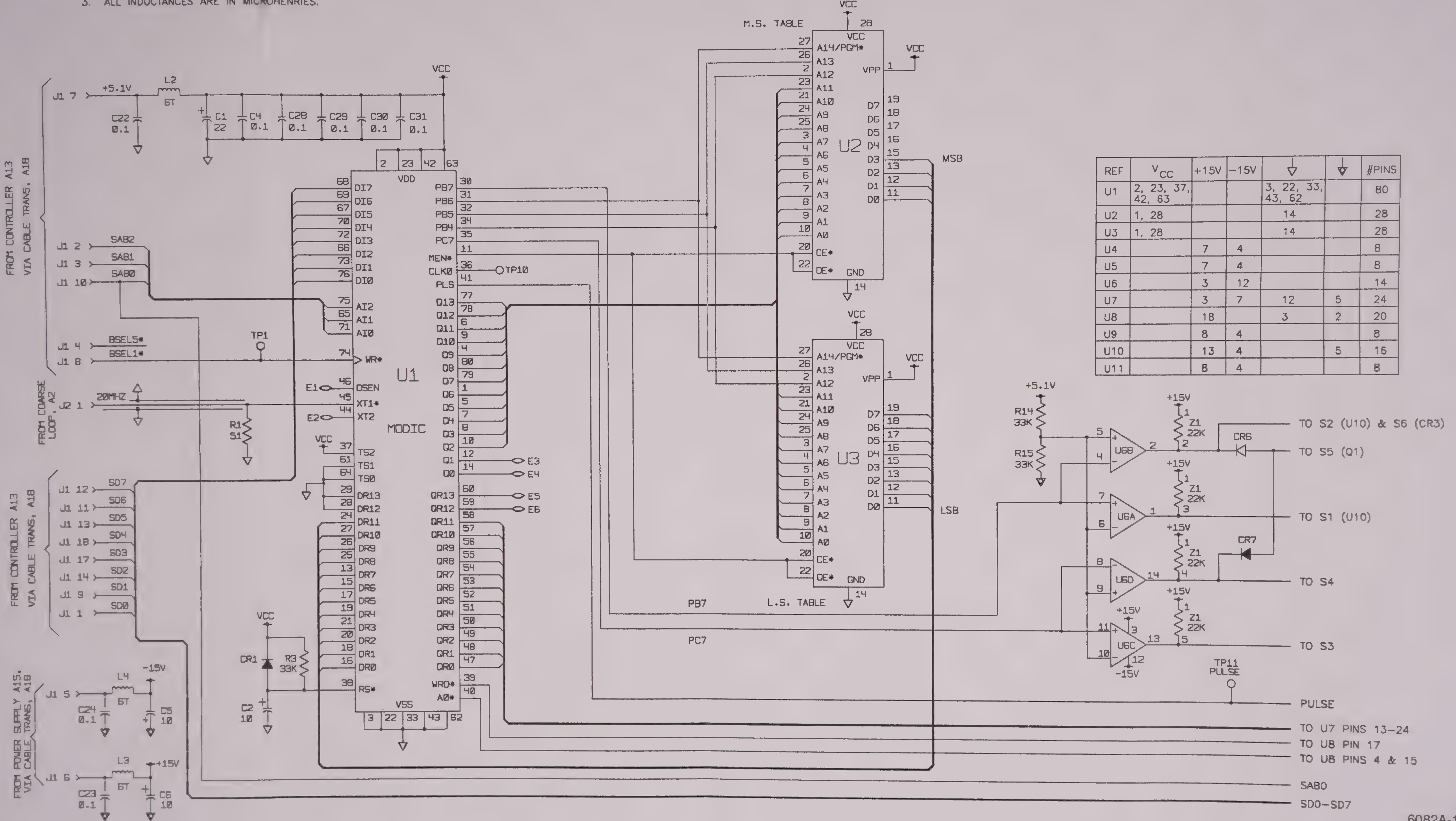

XU2
XU3
C2
R3
CR1
L2
C1
TP10
C22
C28
C30
U1
TP7
TP8
C29
C31
R14
U6
Z1
R15
CR7
CR6
U8
R5
R4
C10
C33
C16
U7
C27
U9
U11
TP2
C15
C9
C32
TP9
C11
C12
C7
C8
R7
U10
R11
R10
R12
R13
C13
R6
R8
L1
R9
C18
A6
C14
TP3
U4
C17
TP6
C26
C25
R22
TP11
J2
TP4
R21
R20
R25
Q1
Q2
L3
C6
TP5
C4
C23
U5
R23
R24
C24
L4
C5
CR4
CR5
CR3
R26
C19
C20
J1
TP1
6082A-1667

Figure 10-6. A6 Mod Oscillator PCA)

NOTES: UNLESS OTHERWISE SPECIFIED,

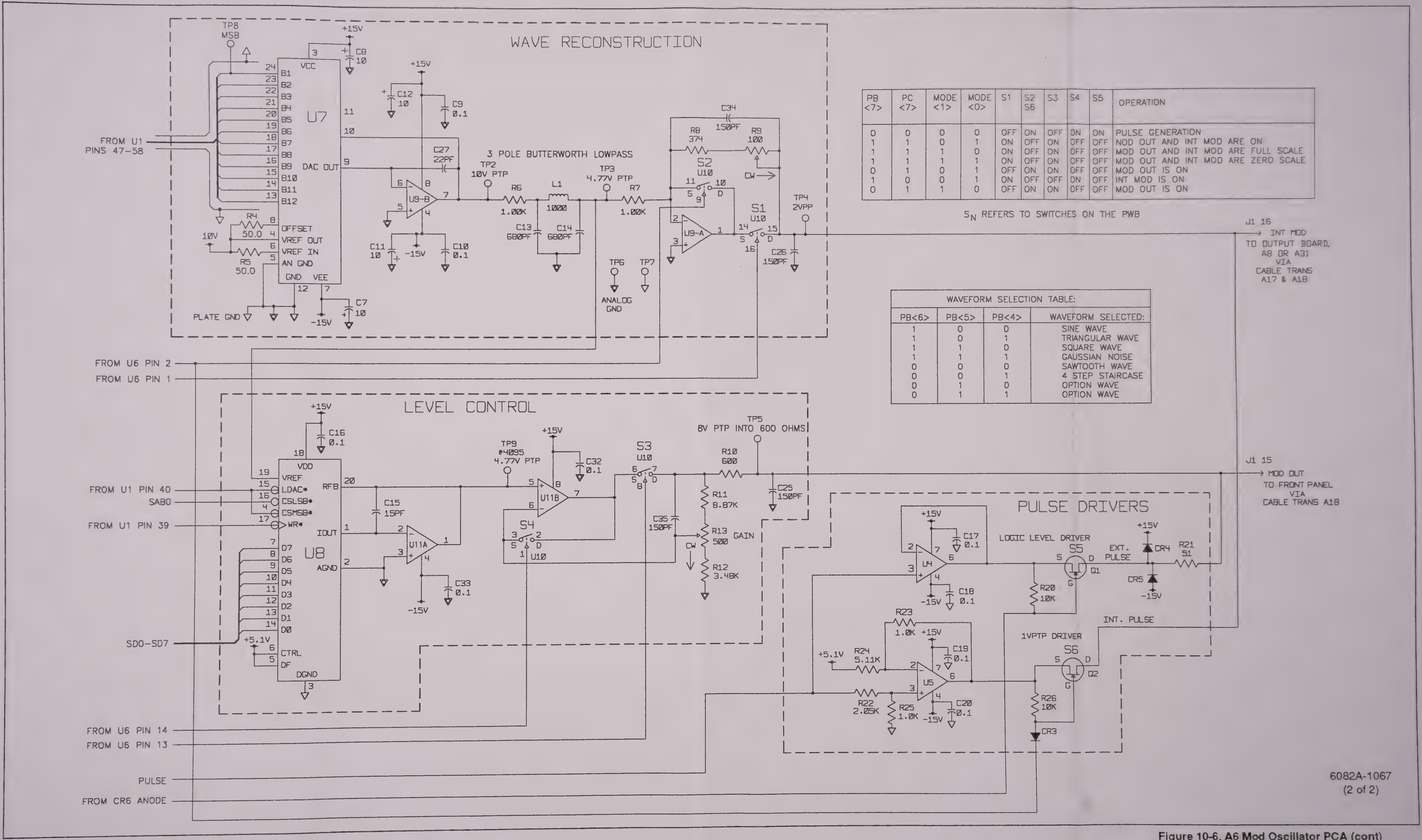
1. ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTANCES ARE IN OHMS.
3. ALL INDUCTANCES ARE IN MICROHENRIES.


FROM CONTROLLER A13 VIA CABLE TRANS, A18
J1 7
+5.1V
L2 6T
VCC
C22 0.1
C1 22
C4 0.1
C28 0.1
C29 0.1
C30 0.1
C31 0.1
J1 2 SAB2
J1 3 SAB1
J1 10 SAB0
J1 4 BSEL5*
J1 8 BSEL1*
TP1
FROM COARSE LOOP, A2
J2 1 20MHZ
R1 51
FROM CONTROLLER A13 VIA CABLE TRANS, A18
J1 12 SD7
J1 11 SD6
J1 13 SD5
J1 18 SD4
J1 17 SD3
J1 14 SD2
J1 9 SD1
J1 1 SD0
FROM POWER SUPPLY A15, VIA CABLE TRANS, A18
J1 5 L4 6T -15V
C24 0.1
C5 10
J1 6 L3 6T +15V
C23 0.1
C6 10
CR1
R3 33K
C2 10
U1
MODIC
VDD
VSS
DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0
AI2 AI1 AI0
WR*
DSEN
XT1*
XT2
TS2 TS1 TS0
DR13 DR12 DR11 DR10 DR9 DR8 DR7 DR6 DR5 DR4 DR3 DR2 DR1 DR0
RS*
PB7 PB6 PB5 PB4 PC7
MEN*
CLK0
PLS
Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
QR13 QR12 QR11 QR10 QR9 QR8 QR7 QR6 QR5 QR4 QR3 QR2 QR1 QR0
WRD*
A0*
TP10
E1 E2 E3 E4 E5 E6
M.S. TABLE
U2
A14/PGM* A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
CE* OE*
VPP
D7 D6 D5 D4 D3 D2 D1 D0
GND
MSB
L.S. TABLE
U3
LSB
PB7
PC7
+5.1V
R14 33K
R15 33K
U6B
U6A
U6D
U6C
Z1 22K
CR6
CR7
TO S2 (U10) & S6 (CR3)
TO S5 (Q1)
TO S1 (U10)
TO S4
TO S3
TP11 PULSE
PULSE
TO U7 PINS 13-24
TO U8 PIN 17
TO U8 PINS 4 & 15
SAB0
SD0-SD7

REF	V_{CC}	+15V	−15V	▽	▼	#PINS
U1	2, 23, 37, 42, 63			3, 22, 33, 43, 62		80
U2	1, 28			14		28
U3	1, 28			14		28
U4		7	4			8
U5		7	4			8
U6		3	12			14
U7		3	7	12	5	24
U8		18		3	2	20
U9		8	4			8
U10		13	4		5	16
U11		8	4			8

6082A-1067
(1 of 2)

Figure 10-6. A6 Mod Oscillator (cont)


WAVE RECONSTRUCTION
TP8
MSB
+15V
C8
10
U7
VCC
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
DAC OUT
OFFSET
VREF OUT
VREF IN
AN GND
GND
VEE
FROM U1
PINS 47-58
R4
50.0
R5
50.0
10V
PLATE GND
-15V
C7
10
C12
10
C9
0.1
C11
10
C10
0.1
C27
22PF
U9-B
3 POLE BUTTERWORTH LOWPASS
TP2
10V PTP
R6
1.00K
L1
1000
C13
680PF
C14
680PF
TP3
4.77V PTP
R7
1.00K
TP6
TP7
ANALOG
GND
C34
150PF
R8
374
R9
100
S2
U10
CW
U9-A
S1
U10
TP4
2VPP
C26
150PF
J1 16
INT MOD
TO OUTPUT BOARD,
A8 OR A31
VIA
CABLE TRANS
A17 & A18
FROM U6 PIN 2
FROM U6 PIN 1
LEVEL CONTROL
+15V
C16
0.1
U8
VDD
VREF
LDAC*
CSLSB*
CSMSB*
WR*
RFB
IOUT
AGND
D7
D6
D5
D4
D3
D2
D1
D0
CTRL
DF
DGND
+5.1V
FROM U1 PIN 40
SAB0
FROM U1 PIN 39
SD0-SD7
C15
15PF
U11A
C33
0.1
TP9
@4095
4.77V PTP
C32
0.1
U11B
S4
U10
S3
U10
TP5
8V PTP INTO 600 OHMS
R10
600
C25
150PF
C35
150PF
R11
8.87K
R13
500
GAIN
R12
3.48K
J1 15
MOD OUT
TO FRONT PANEL
VIA
CABLE TRANS A18
PULSE DRIVERS
+15V
C17
0.1
U4
C18
0.1
LOGIC LEVEL DRIVER
S5
Q1
EXT.
PULSE
CR4
R21
51
CR5
R20
10K
INT. PULSE
R23
1.0K
+5.1V
R24
5.11K
C19
0.1
U5
R22
2.05K
R25
1.0K
C20
0.1
1VPTP DRIVER
S6
Q2
R26
10K
CR3
FROM U6 PIN 14
FROM U6 PIN 13
PULSE
FROM CR6 ANODE
6082A-1067
(2 of 2)

PB <7>	PC <7>	MODE <1>	MODE <0>	S1	S2 S6	S3	S4	S5	OPERATION
0	0	0	0	OFF	ON	OFF	ON	ON	PULSE GENERATION
1	1	0	1	ON	OFF	ON	OFF	OFF	NOD OUT AND INT MOD ARE ON
1	1	1	0	ON	OFF	ON	OFF	OFF	MOD OUT AND INT MOD ARE FULL SCALE
1	1	1	1	ON	OFF	ON	OFF	OFF	MOD OUT AND INT MOD ARE ZERO SCALE
0	1	0	1	OFF	ON	ON	OFF	OFF	MOD OUT IS ON
1	0	0	1	ON	OFF	OFF	ON	OFF	INT MOD IS ON
0	1	1	0	OFF	ON	ON	OFF	OFF	MOD OUT IS ON

S_N REFERS TO SWITCHES ON THE PWB

WAVEFORM SELECTION TABLE:

PB<6>	PB<5>	PB<4>	WAVEFORM SELECTED:
1	0	0	SINE WAVE
1	0	1	TRIANGULAR WAVE
1	1	0	SQUARE WAVE
1	1	1	GAUSSIAN NOISE
0	0	0	SAWTOOTH WAVE
0	0	1	4 STEP STAIRCASE
0	1	0	OPTION WAVE
0	1	1	OPTION WAVE

Figure 10-6. A6 Mod Oscillator PCA (cont)

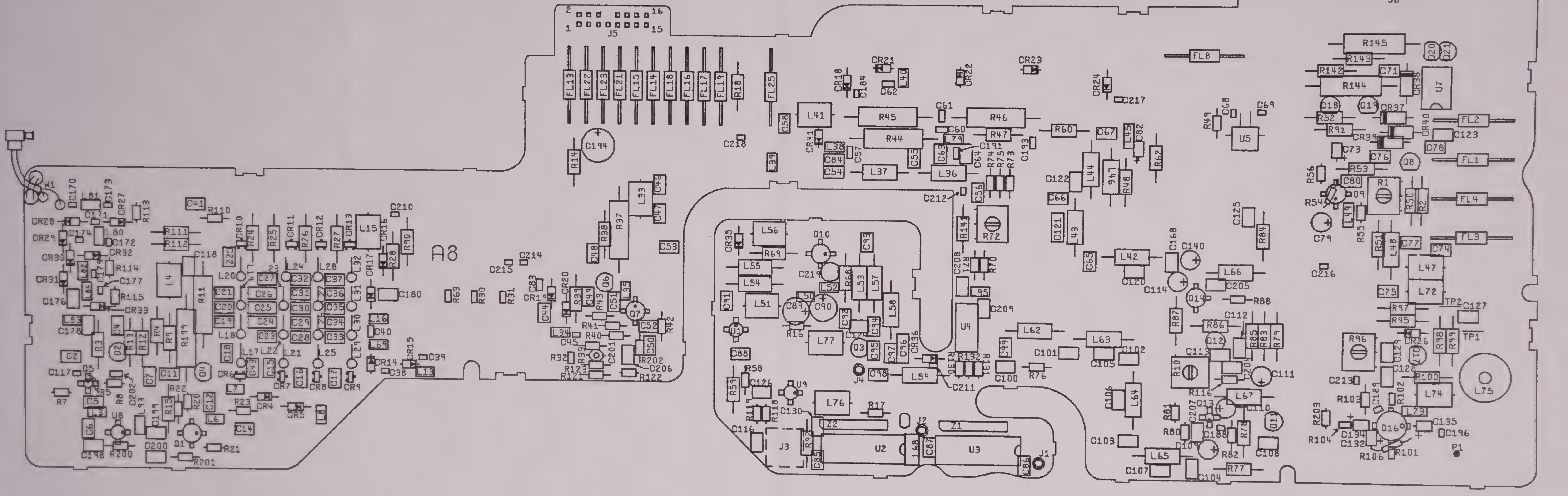
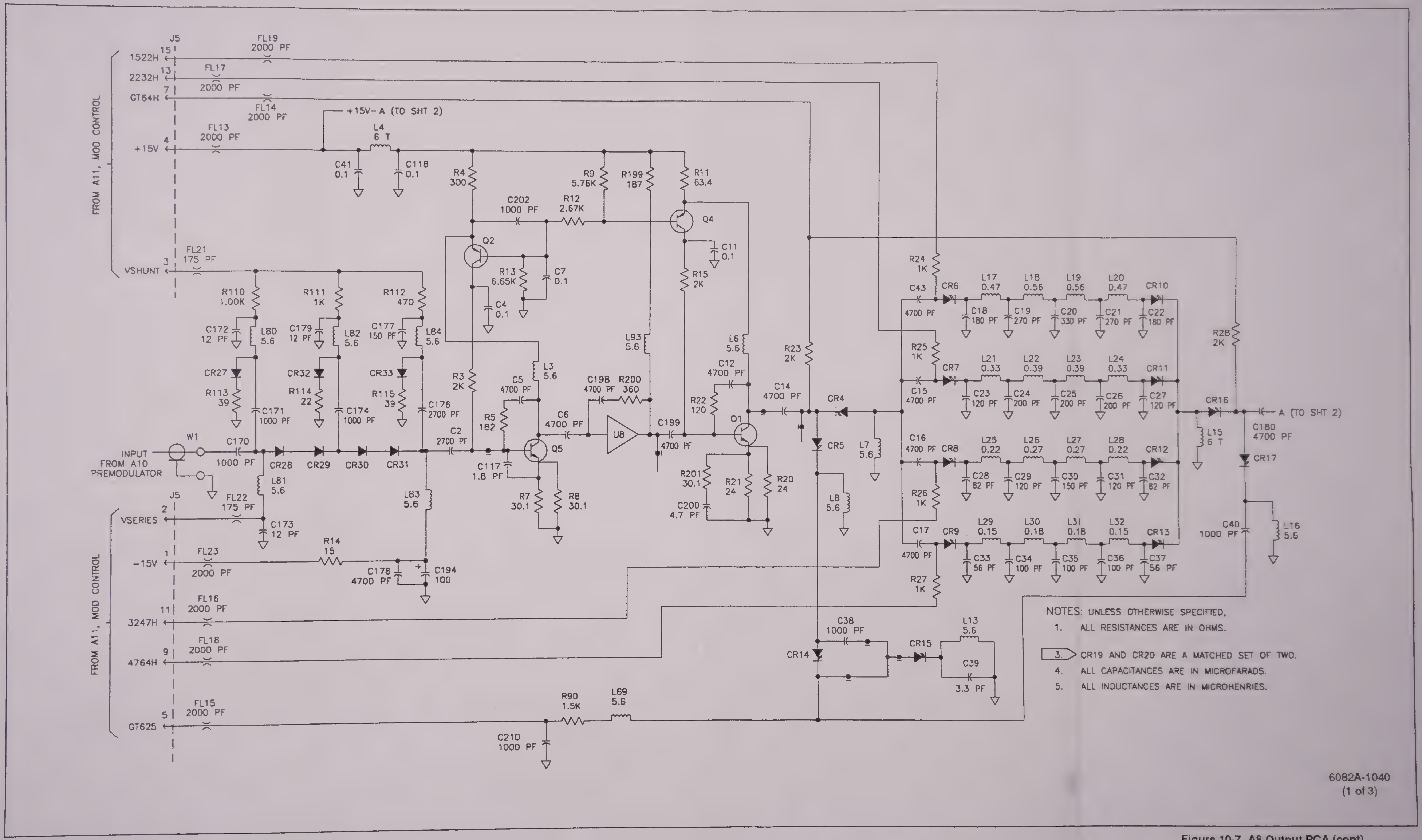

A8
J5
J6
W1
FL13
FL22
FL23
FL21
FL15
FL14
FL18
FL16
FL17
FL19
R18
FL25
FL8
FL2
FL1
FL4
FL3
C194
R14
L33
R37
R38
C48
C53
Q6
Q7
R42
C52
C50
R202
C206
R122
R121
R123
R32
C201
C45
R40
R41
R43
C49
R39
CR20
CR19
C44
C83
C214
C215
R63
R30
R31
L15
R28
R90
C210
C180
CR17
CR16
L32
L31
L30
L29
L28
L26
L24
L23
L22
L21
L20
L18
L17
L25
C37
C36
C35
C34
C33
C32
C31
C30
C29
C28
C27
C26
C25
C24
C23
C22
C21
C20
C19
C18
C17
C16
C15
C13
C14
C12
C11
C7
C6
C5
C4
C2
R27
R26
R25
R24
R11
R12
R13
R9
R4
R3
R199
R111
R112
R110
R113
R114
R115
C41
C118
L4
CR13
CR12
CR11
CR10
CR28
CR29
CR30
CR31
CR32
CR33
CR27
CR4
CR5
CR6
CR7
CR8
CR9
CR14
CR15
C38
C39
L13
L16
C40
L69
L6
L7
L81
L80
L82
L83
L93
C170
C171
C172
C173
C174
C176
C177
C178
C117
C198
C199
C200
C202
R200
R201
R21
R22
R23
R20
R15
R8
R7
Q1
Q2
Q4
Q5
U8
C58
L41
L39
L38
C84
C54
C57
L37
L36
R45
R44
R46
R47
C55
C63
L79
C60
C61
C62
C64
C191
C193
C216
C218
CR18
CR21
CR22
CR23
CR24
CR41
C184
L40
C217
R60
C67
C82
L45
R62
L44
L46
R48
C122
C66
C121
L43
R74
R75
R73
C56
C212
R143
R72
C208
R71
R70
CR35
L56
R69
L55
L54
L51
Q10
C93
C219
C89
C90
C50
L52
R68
L53
L57
L58
C92
C94
C95
C97
C96
CR36
U4
C209
C95
R16
L77
C124
Q3
C91
U1
C88
R58
R59
C126
U9
R119
R118
C130
C116
L76
R17
J4
C98
L59
R130
R131
R132
C211
C99
C100
L62
R76
C101
L63
C105
C102
J3
R92
C85
U2
L68
C87
U3
C86
Z1
Z2
J2
J1
C63
L42
C120
C168
C140
C114
L66
C205
Q14
R88
C112
R87
R86
Q12
R85
R83
R79
C113
R10
C204
C111
R116
L67
C110
Q13
C207
R81
R80
C188
C109
R78
Q11
R82
C108
C106
L64
C103
L65
C107
C104
R77
R49
C68
C69
U5
C125
R84
R145
R143
R142
R144
C71
CR38
U7
Q20
Q21
Q18
Q19
CR37
R52
R91
CR39
CR40
C123
C73
C76
C78
Q8
R53
R56
C80
R1
R54
Q9
R50
R2
C79
C49
R55
R51
L48
C77
C74
L47
C75
L72
R97
R95
TP2
C127
TP1
R96
CR26
C129
Q17
R98
R99
C128
C213
R100
R103
C189
R102
L74
L75
L73
R203
C134
C132
R104
Q16
C135
C196
R106
R101
P1
2
16
1
15
10
9
6082A-1640

Figure 10-7. A8 Output PCA


FROM A11, MOD CONTROL
J5
15
1522H
FL19
2000 PF
13
2232H
FL17
2000 PF
7
GT64H
FL14
2000 PF
+15V-A (TO SHT 2)
4
+15V
FL13
2000 PF
L4
6 T
C41
0.1
C118
0.1
R4
300
R9
5.76K
R199
187
R11
63.4
C202
1000 PF
R12
2.67K
Q4
Q2
C11
0.1
3
VSHUNT
FL21
175 PF
R13
6.65K
C7
0.1
R15
2K
C4
0.1
R110
1.00K
R111
1K
R112
470
C172
12 PF
L80
5.6
C179
12 PF
L82
5.6
C177
150 PF
L84
5.6
L93
5.6
L6
5.6
CR27
CR32
CR33
R113
39
R114
22
R115
39
C171
1000 PF
C174
1000 PF
C176
2700 PF
R3
2K
L3
5.6
C5
4700 PF
C198
4700 PF
R200
360
C12
4700 PF
R22
120
C14
4700 PF
R23
2K
CR4
R5
182
C6
4700 PF
U8
C199
4700 PF
Q1
W1
INPUT FROM A10 PREMODULATOR
C170
1000 PF
CR28
CR29
CR30
CR31
C2
2700 PF
C117
1.8 PF
Q5
R201
30.1
C200
4.7 PF
R21
24
R20
24
CR5
L7
5.6
L8
5.6
L81
5.6
L83
5.6
R7
30.1
R8
30.1
J5
2
VSERIES
FL22
175 PF
C173
12 PF
1
-15V
FL23
2000 PF
R14
15
C178
4700 PF
C194
100
11
3247H
FL16
2000 PF
9
4764H
FL18
2000 PF
5
GT625
FL15
2000 PF
R90
1.5K
L69
5.6
C210
1000 PF
C38
1000 PF
CR14
CR15
L13
5.6
C39
3.3 PF
R24
1K
C43
4700 PF
CR6
L17
0.47
L18
0.56
L19
0.56
L20
0.47
CR10
C18
180 PF
C19
270 PF
C20
330 PF
C21
270 PF
C22
180 PF
R25
1K
CR7
L21
0.33
L22
0.39
L23
0.39
L24
0.33
CR11
C15
4700 PF
C23
120 PF
C24
200 PF
C25
200 PF
C26
200 PF
C27
120 PF
C16
4700 PF
CR8
L25
0.22
L26
0.27
L27
0.27
L28
0.22
CR12
R26
1K
C28
82 PF
C29
120 PF
C30
150 PF
C31
120 PF
C32
82 PF
C17
4700 PF
CR9
L29
0.15
L30
0.18
L31
0.18
L32
0.15
CR13
C33
56 PF
C34
100 PF
C35
100 PF
C36
100 PF
C37
56 PF
R27
1K
R28
2K
CR16
A (TO SHT 2)
C180
4700 PF
L15
6 T
CR17
C40
1000 PF
L16
5.6

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES ARE IN OHMS.

3. CR19 AND CR20 ARE A MATCHED SET OF TWO.

4. ALL CAPACITANCES ARE IN MICROFARADS.

5. ALL INDUCTANCES ARE IN MICROHENRIES.

6082A-1040
(1 of 3)

Figure 10-7. A8 Output PCA (cont)

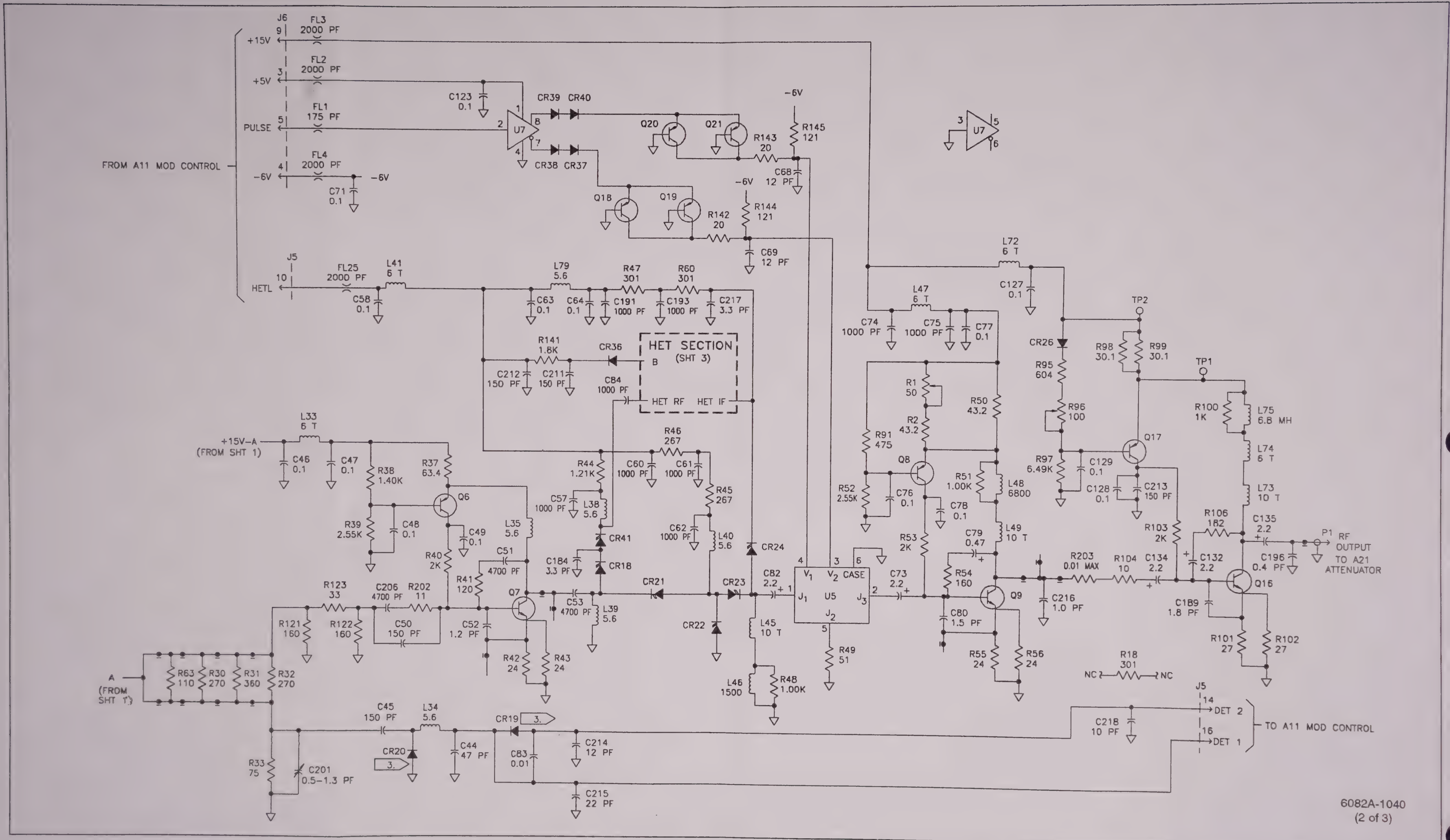

J6
FL3 2000 PF
+15V 9
FL2 2000 PF
+5V 3
FL1 175 PF
PULSE 5
FL4 2000 PF
-6V 4
FROM A11 MOD CONTROL
C71 0.1
-6V
C123 0.1
U7
CR39 CR40
CR38 CR37
Q20 Q21
R143 20
-6V
R145 121
C68 12 PF
Q18 Q19
R142 20
-6V
R144 121
C69 12 PF
U7
J5
HETL 10
FL25 2000 PF
C58 0.1
L41 6 T
L79 5.6
R47 301
R60 301
C63 0.1
C64 0.1
C191 1000 PF
C193 1000 PF
C217 3.3 PF
R141 1.8K
CR36
C212 150 PF
C211 150 PF
C84 1000 PF
HET SECTION (SHT 3)
B
HET RF
HET IF
L72 6 T
C127 0.1
L47 6 T
C74 1000 PF
C75 1000 PF
C77 0.1
TP2
CR26
R95 604
R98 30.1
R99 30.1
TP1
R1 50
R2 43.2
R50 43.2
R91 475
R96 100
R100 1K
L75 6.8 MH
Q17
L74 6 T
Q8
R97 6.49K
C129 0.1
R51 1.00K
L48 6800
C128 0.1
C213 150 PF
L73 10 T
R52 2.55K
C76 0.1
C78 0.1
R106 182
C135 2.2
R103 2K
L33 6 T
+15V-A (FROM SHT 1)
C46 0.1
C47 0.1
R38 1.40K
R37 63.4
Q6
R39 2.55K
C48 0.1
C49 0.1
R40 2K
R44 1.21K
R46 267
C60 1000 PF
C61 1000 PF
R45 267
C57 1000 PF
L38 5.6
L35 5.6
C62 1000 PF
L40 5.6
CR41
CR24
C184 3.3 PF
CR18
C51 4700 PF
R41 120
Q7
R123 33
C206 4700 PF
R202 11
C50 150 PF
C52 1.2 PF
C53 4700 PF
L39 5.6
CR21
CR23
CR22
C82 2.2
V1 V2 CASE
J1 U5 J3
J2
4 3 6 1 2 5
C73 2.2
R53 2K
C79 0.47
L49 10 T
R54 160
Q9
C80 1.5 PF
R203 0.01 MAX
R104 10
C134 2.2
C132 2.2
C196 0.4 PF
P1 RF OUTPUT TO A21 ATTENUATOR
Q16
C216 1.0 PF
C189 1.8 PF
R101 27
R102 27
R121 160
R122 160
R42 24
R43 24
L45 10 T
R49 51
R55 24
R56 24
R18 301
NC NC
A (FROM SHT 1)
R63 110
R30 270
R31 360
R32 270
L46 1500
R48 1.00K
J5
14 DET 2
16 DET 1
TO A11 MOD CONTROL
C218 10 PF
C45 150 PF
L34 5.6
CR19 3.
CR20 3.
C44 47 PF
C83 0.01
C214 12 PF
C215 22 PF
R33 75
C201 0.5-1.3 PF
6082A-1040 (2 of 3)

Figure 10-7. A8 Output PCA (cont)

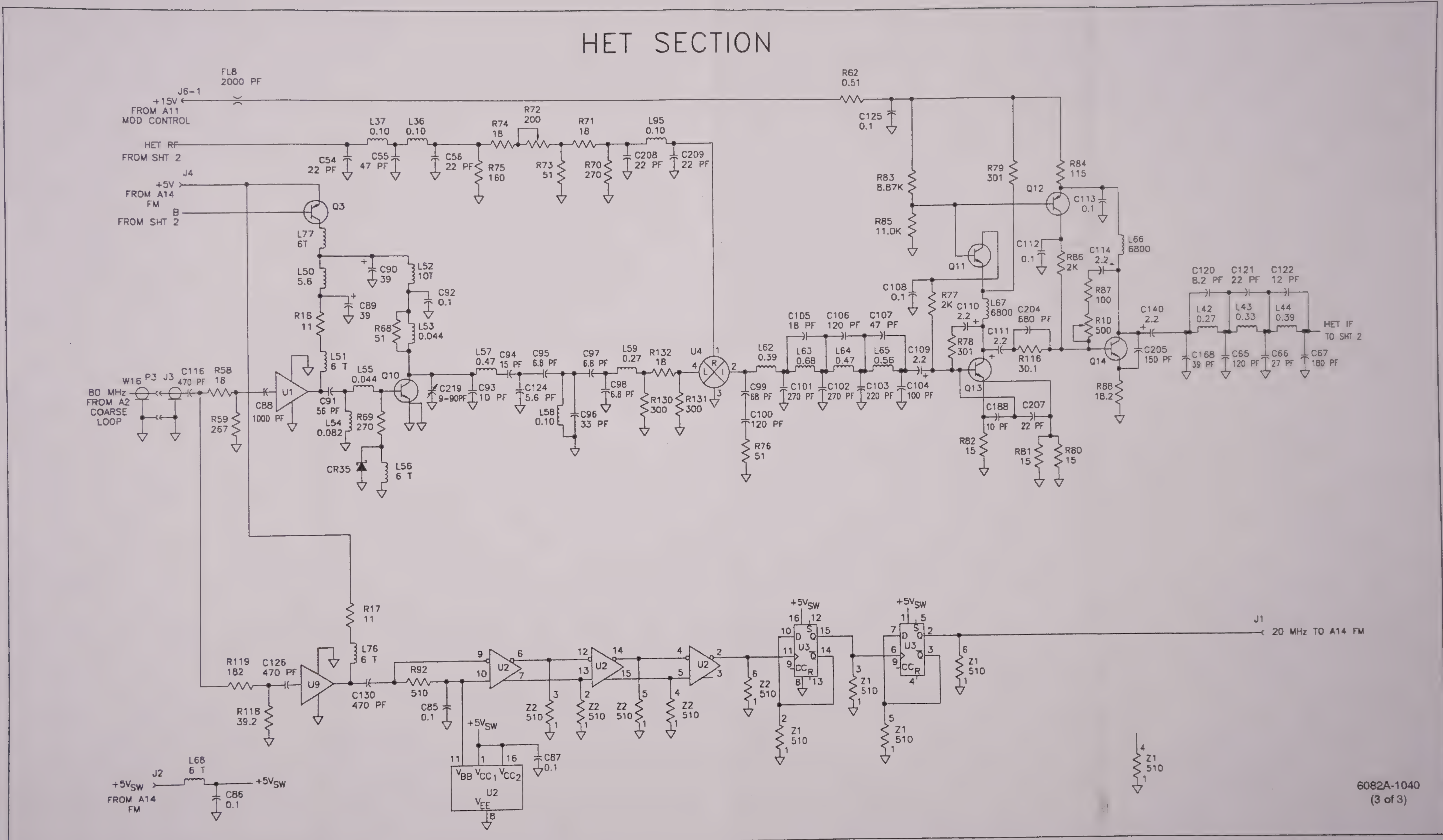
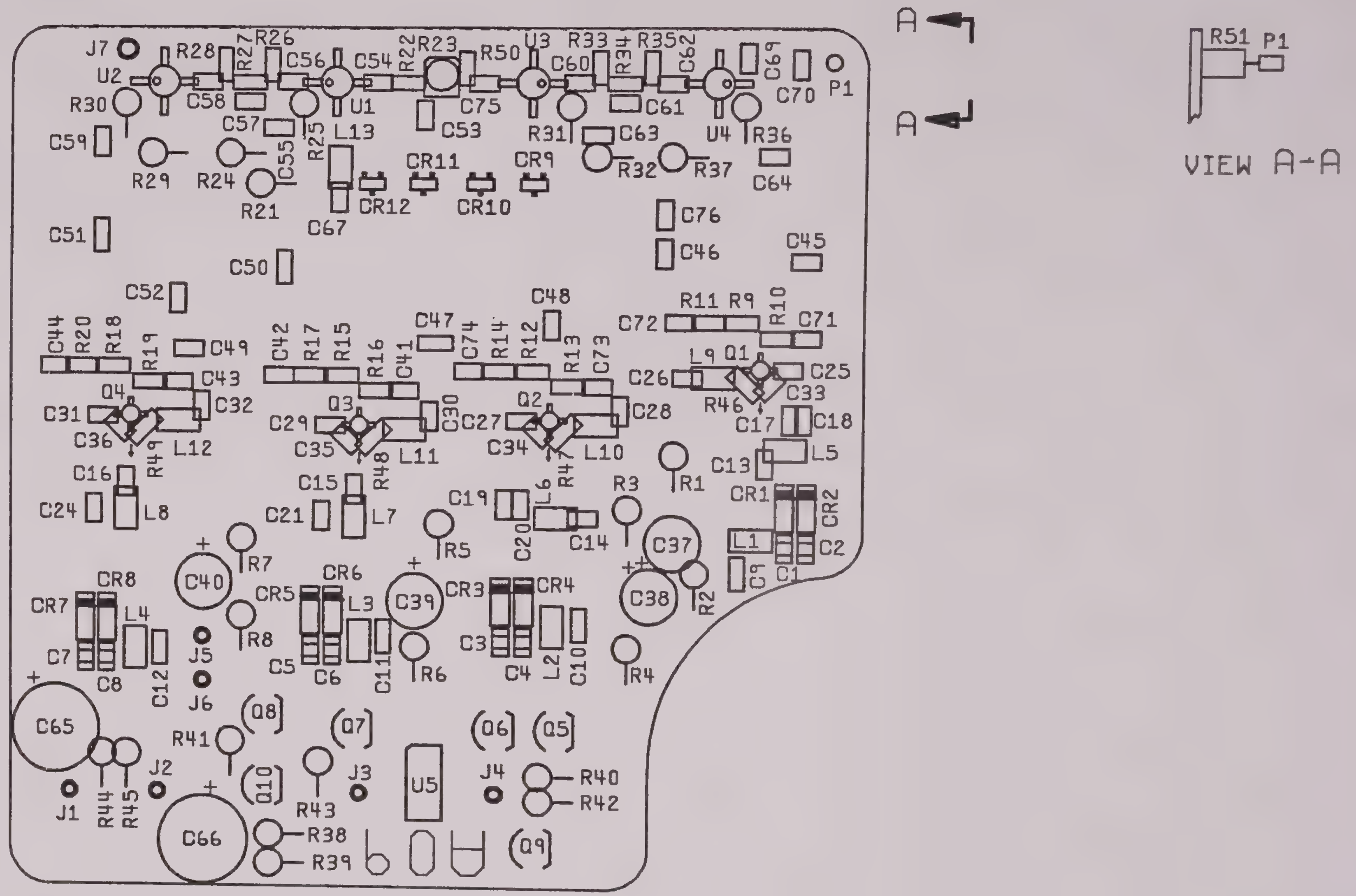
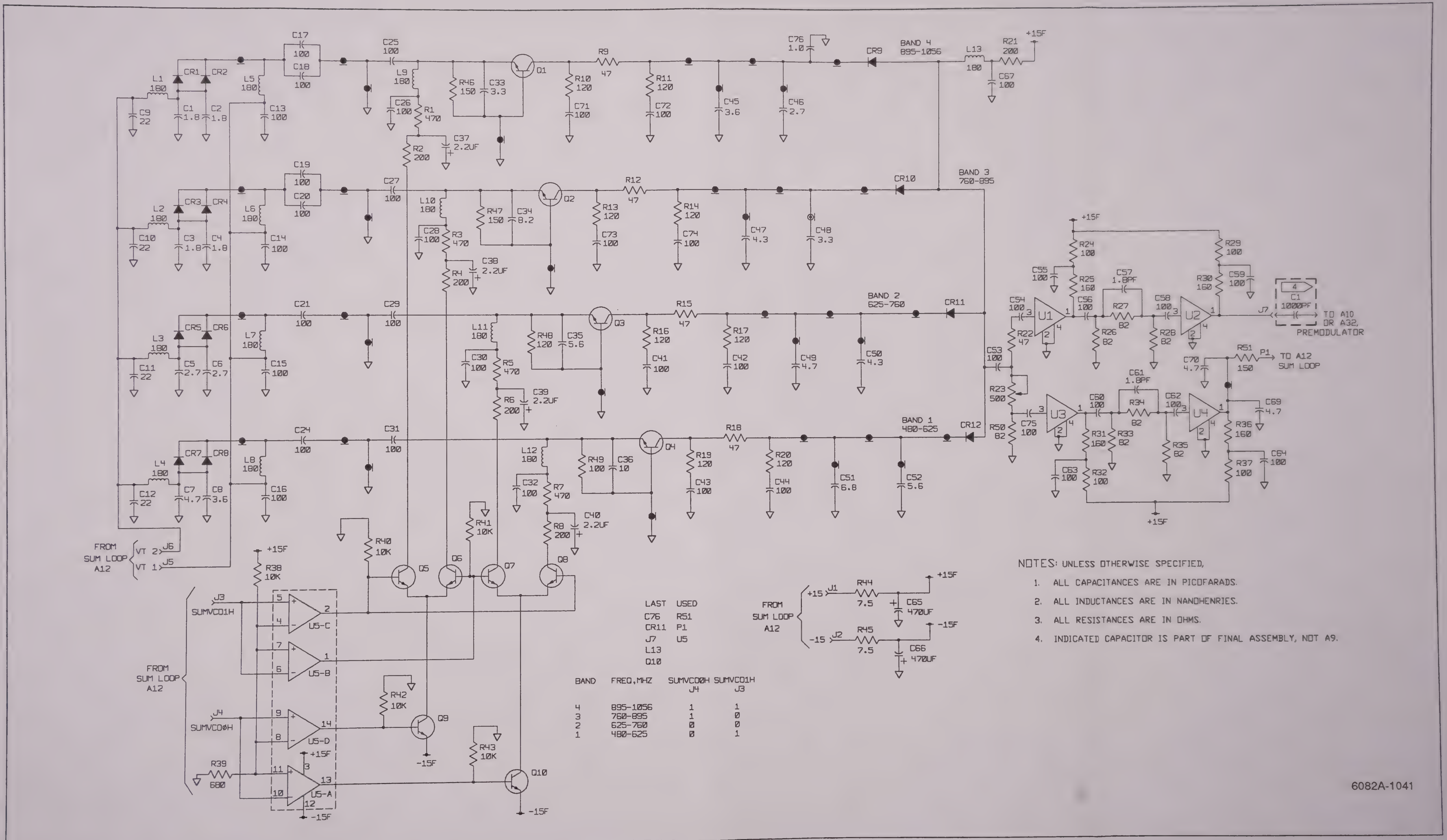

HET SECTION
FL8
2000 PF
J6-1
+15V
FROM A11
MOD CONTROL
HET RF
FROM SHT 2
J4
+5V
FROM A14
FM
B
FROM SHT 2
L37
0.10
L36
0.10
R74
18
R72
200
R71
18
L95
0.10
C54
22 PF
C55
47 PF
C56
22 PF
R75
160
R73
51
R70
270
C208
22 PF
C209
22 PF
R62
0.51
C125
0.1
Q3
L77
6T
L50
5.6
C90
39
L52
10T
C92
0.1
C89
39
R16
11
R68
51
L53
0.044
L51
6 T
W16
P3
J3
C116
470 PF
R58
18
80 MHz
FROM A2
COARSE
LOOP
R59
267
C88
1000 PF
U1
C91
56 PF
L55
0.044
L54
0.082
R69
270
Q10
C219
9-90PF
C93
10 PF
CR35
L56
6 T
L57
0.47
C94
15 PF
C95
6.8 PF
C124
5.6 PF
L58
0.10
C96
33 PF
C97
6.8 PF
L59
0.27
C98
6.8 PF
R132
18
R130
300
R131
300
U4
R
L
I
L62
0.39
C99
68 PF
C100
120 PF
R76
51
C105
18 PF
C106
120 PF
C107
47 PF
L63
0.68
L64
0.47
L65
0.56
C101
270 PF
C102
270 PF
C103
220 PF
C104
100 PF
C109
2.2
R83
8.87K
R85
11.0K
Q11
C108
0.1
R77
2K
R79
301
R84
115
Q12
C113
0.1
C112
0.1
R86
2K
C114
2.2
L66
6800
C110
2.2
L67
6800
C204
680 PF
R87
100
R10
500
R78
301
C111
2.2
R116
30.1
Q13
Q14
C188
10 PF
C207
22 PF
R82
15
R81
15
R80
15
R88
18.2
C140
2.2
C205
150 PF
C120
8.2 PF
C121
22 PF
C122
12 PF
L42
0.27
L43
0.33
L44
0.39
C168
39 PF
C65
120 PF
C66
27 PF
C67
180 PF
HET IF
TO SHT 2
R17
11
L76
6 T
R119
182
C126
470 PF
U9
R118
39.2
C130
470 PF
R92
510
C85
0.1
U2
Z2
510
+5V_SW
U3
D
S
Q
CC
R
J1
20 MHz TO A14 FM
Z1
510
V_BB
V_CC1
V_CC2
V_EE
C87
0.1
J2
L68
6 T
FROM A14
FM
C86
0.1
6082A-1040
(3 of 3)

Figure 10-7. A8 Output PCA (cont)


A
A
VIEW A-A
R51
P1
J7
U2
R28
R27
R26
C56
C54
R22
R23
R50
U3
R33
R34
R35
C62
C69
C70
P1
R30
C58
U1
C75
C60
C61
U4
R36
C59
C57
R25
L13
C53
R31
C63
R29
R24
C55
CR11
CR9
R32
R37
C64
R21
CR12
CR10
C67
C76
C51
C50
C46
C45
C52
C48
C47
R11
R9
R10
C72
C71
C44
R20
R18
R19
C49
C42
R17
R15
R16
C41
C74
R14
R12
R13
C73
L9
Q1
C25
C43
C26
C33
Q4
C32
Q3
C30
Q2
C28
R46
C31
C29
C27
C17
C18
C36
R49
L12
C35
R48
L11
C34
R47
L10
L5
C16
C15
C13
R1
C19
L6
R3
CR1
CR2
C24
L8
C21
L7
R5
C20
C14
C37
L1
C2
R7
CR6
C9
C1
CR8
C40
CR5
C39
CR3
CR4
C38
R2
CR7
L4
L3
R8
J5
C7
C5
C6
C11
R6
C3
C4
L2
C10
R4
C8
C12
J6
C65
Q8
Q7
Q6
Q5
R41
J2
Q10
J3
U5
J4
R40
R42
J1
R44
R45
C66
R43
R38
R39
Q9

6082A-1641

Figure 10-8. A9 Sum Loop VCO PCA


BAND 4
895-1056
BAND 3
760-895
BAND 2
625-760
BAND 1
480-625
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
U1
U2
U3
U4
U5-A
U5-B
U5-C
U5-D
CR9
CR10
CR11
CR12
L13
180
R21
200
+15F
-15F
J7
C1
1000PF
TO A10
OR A32,
PREMODULATOR
R51
150
P1
TO A12
SUM LOOP
FROM
SUM LOOP
A12
VT 2
J6
VT 1
J5
J3
SUMVCO1H
J4
SUMVCO0H
R39
680
+15
J1
R44
7.5
C65
470UF
-15
J2
R45
7.5
C66
470UF

NOTES: UNLESS OTHERWISE SPECIFIED,

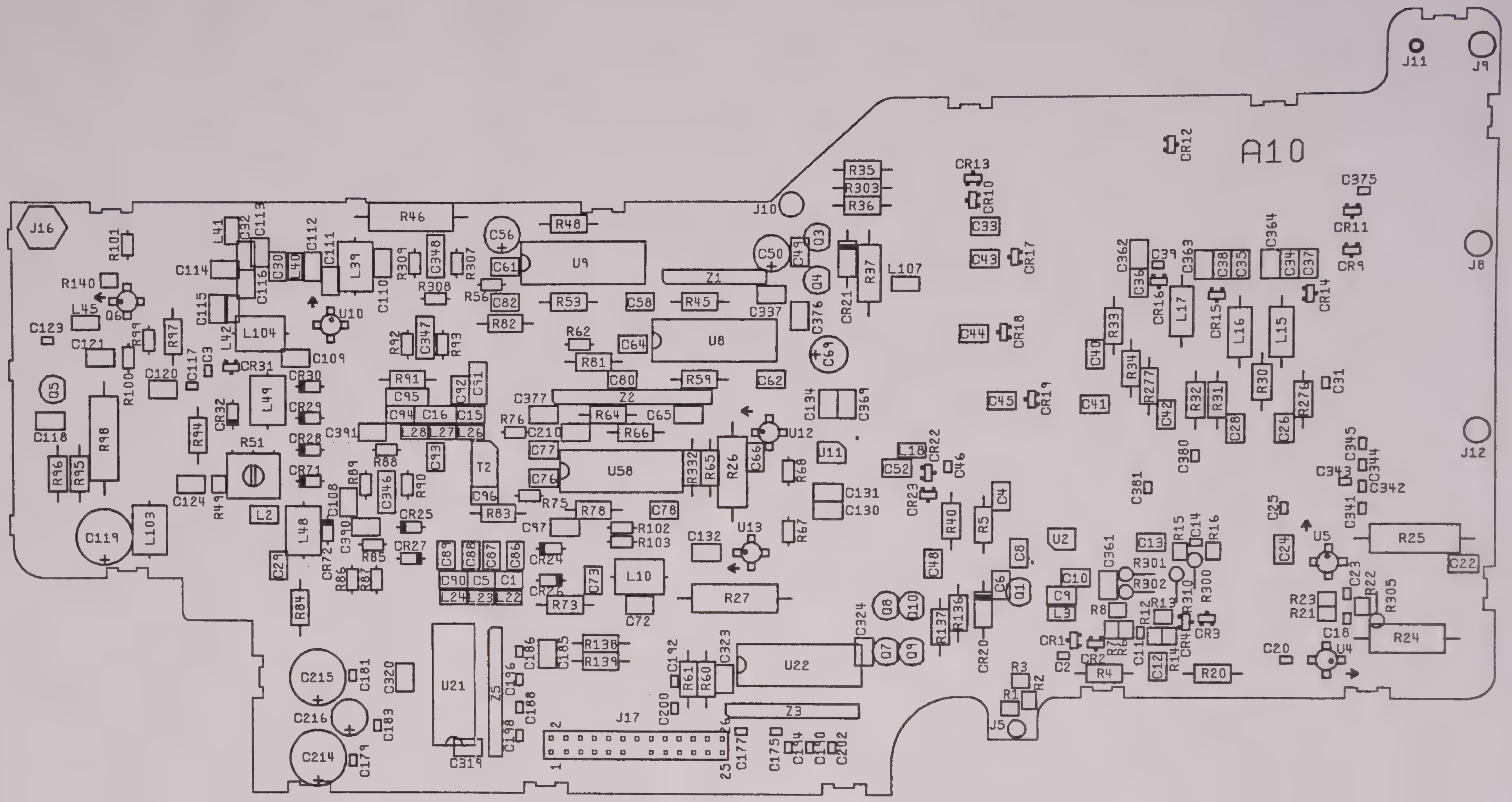
1. ALL CAPACITANCES ARE IN PICOFARADS.
2. ALL INDUCTANCES ARE IN NANOHENRIES.
3. ALL RESISTANCES ARE IN OHMS.
4. INDICATED CAPACITOR IS PART OF FINAL ASSEMBLY, NOT A9.

LAST	USED
C76	R51
CR11	P1
J7	U5
L13	
Q10	

BAND	FREQ,MHZ	SUMVCO0H J4	SUMVCO1H J3
4	895-1056	1	1
3	760-895	1	0
2	625-760	0	0
1	480-625	0	1

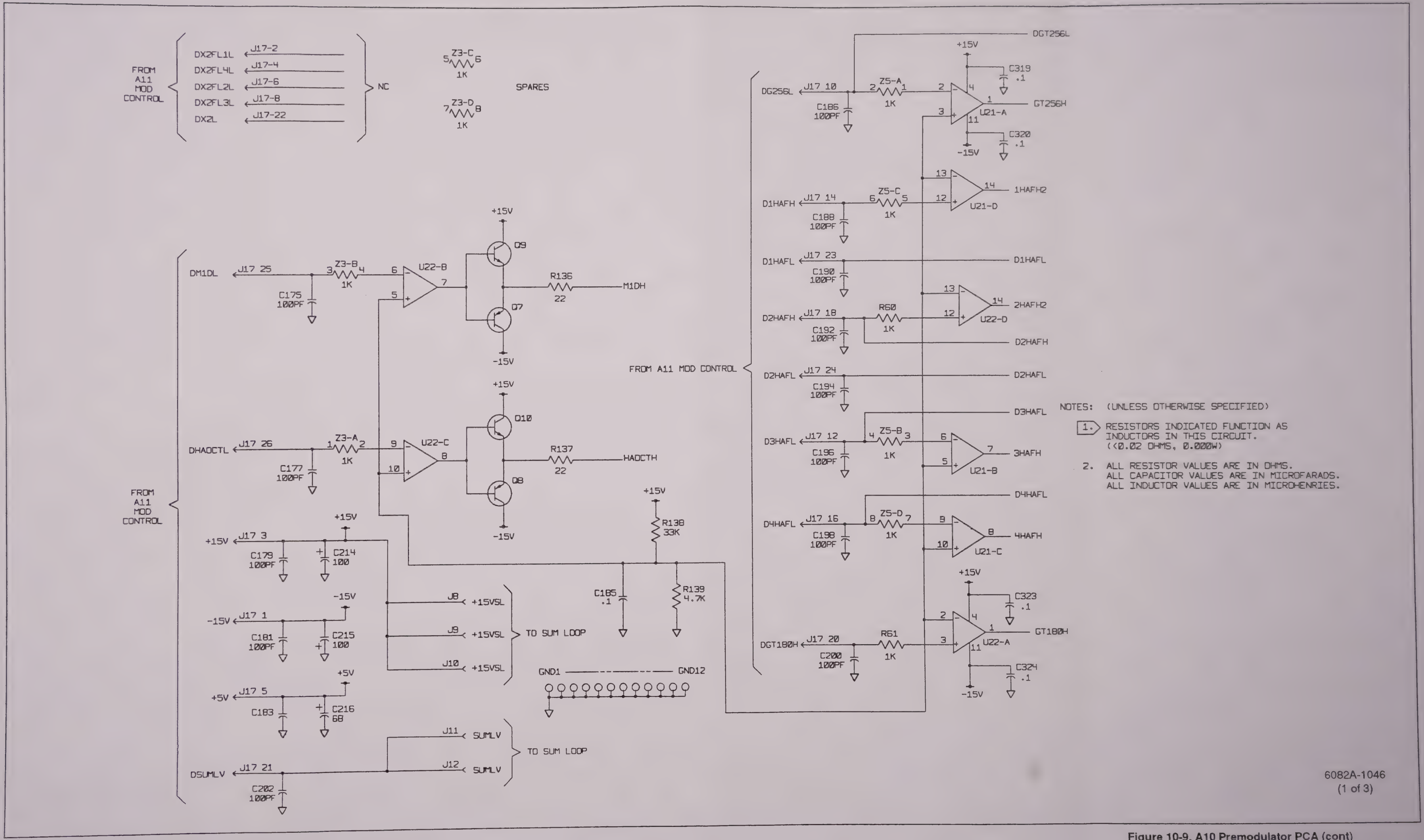
6082A-1041

Figure 10-8. A9 Sum Loop VCO PCA (cont)


A10
J11
J9
J8
J12
J10
J16
J5
J17
1
2
25
26
CR12
C375
CR11
CR9
R35
R303
R36
CR13
CR10
C33
C43
CR17
L107
R37
CR21
C376
Q4
Q3
C49
C50
C337
R46
R48
C56
C61
U9
Z1
R45
C58
R53
C82
R56
R308
R307
C348
R309
C110
L39
C111
C112
L40
C30
C116
C113
C32
L41
C114
R101
R140
L45
Q6
C123
C121
R99
R97
C115
L42
L104
U10
C109
R92
C347
R93
R82
R62
C64
U8
C69
R81
C80
R59
C62
C134
C369
C44
CR18
C45
CR19
C41
C40
R33
R34
R277
C42
R32
R31
C28
R30
R276
C26
C31
L17
CR16
C39
C363
C36
C362
C38
C35
C364
C34
C37
CR14
L16
L15
CR15
Q5
C118
R98
R96
R95
R100
C120
C117
C03
CR31
CR30
L49
CR29
CR32
R94
R51
CR28
C391
R91
C95
C94
C16
C15
C92
C91
L28
L27
L26
C377
Z2
R76
C210
R64
C65
R66
U12
C66
R26
U11
L18
CR22
C52
C46
C131
C130
CR23
C4
R40
R5
C77
C76
U58
R332
R65
R68
R67
C78
R78
R102
R103
C132
U13
C97
R75
R83
C96
T2
C93
R88
R89
R90
C346
CR25
CR71
C124
R49
L2
L48
C108
C390
CR72
R85
R86
R87
CR27
C89
C88
C87
C86
CR24
C90
C5
C1
L24
L23
L22
CR26
R73
C73
L10
C72
R27
C29
R84
C119
L103
C215
C216
C214
C181
C183
C179
C320
U21
C319
Z5
C186
C185
C196
C188
C198
R138
R139
C192
R61
R60
C323
C200
C324
U22
Z3
C177
C175
C174
C170
C202
Q8
Q10
Q7
Q9
R137
R136
CR20
C6
Q1
C48
C8
U2
C10
C9
L3
C361
R8
C13
R15
C14
R16
R301
R302
R300
R310
R13
R12
R7
C11
CR1
CR2
C2
R14
CR4
CR3
C12
R4
R20
R3
R1
R2
C380
C381
C25
U5
C24
C343
C345
C344
C342
C341
R25
C22
C23
R22
R305
R23
R21
C18
C20
U4
R24

6082A-1646

Figure 10-9. A10 Premodulator PCA

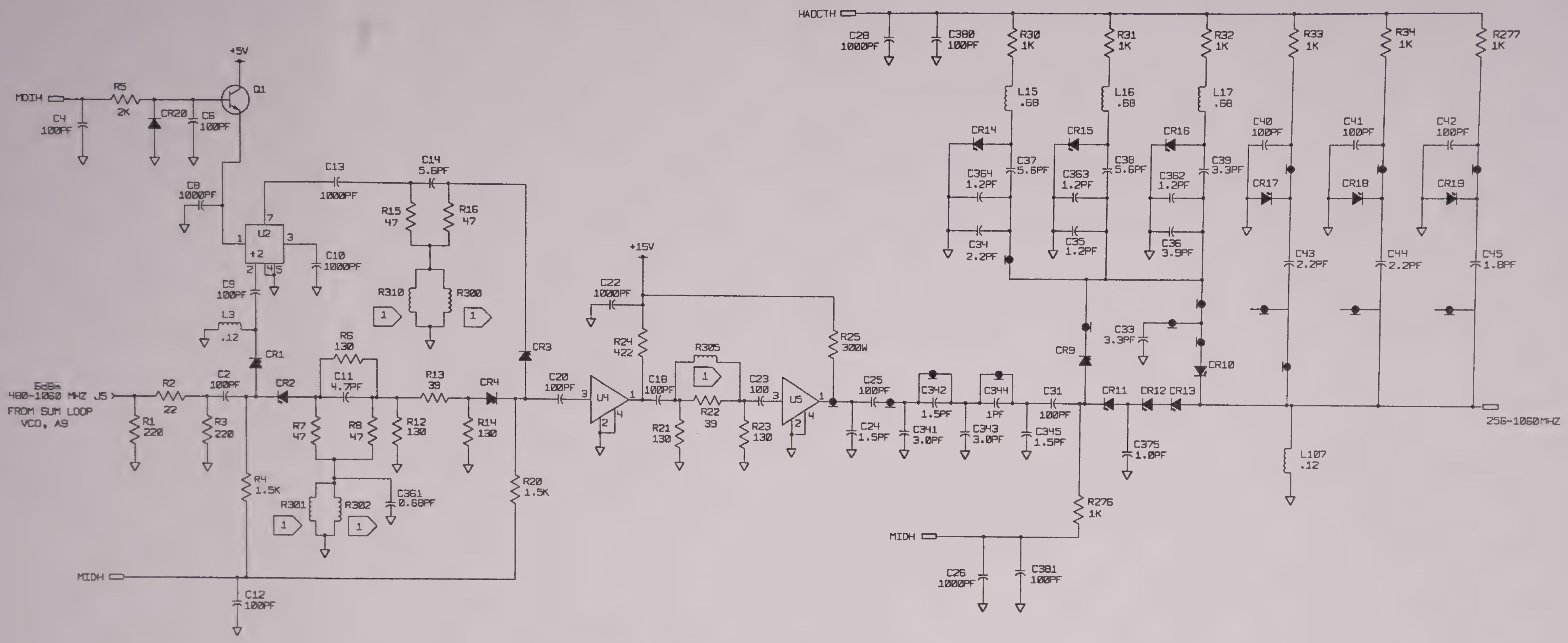

FROM A11 MOD CONTROL
DX2FL1L J17-2
DX2FL4L J17-4
DX2FL2L J17-6
DX2FL3L J17-8
DX2L J17-22
NC
Z3-C 5 6 1K
Z3-D 7 8 1K
SPARES
DM1DL J17 25
C175 100PF
Z3-B 3 4 1K
U22-B 6 5 7
+15V
Q9
Q7
-15V
R136 22
M1DH
+15V
Q10
Q8
-15V
DHAOCTL J17 26
C177 100PF
Z3-A 1 2 1K
U22-C 9 10 8
R137 22
HADCTH
FROM A11 MOD CONTROL
+15V J17 3
C179 100PF
C214 100
+15V
-15V J17 1
C181 100PF
C215 100
-15V
+5V J17 5
C183
C216 68
+5V
J8 +15VSL
J9 +15VSL
J10 +15VSL
TO SUM LOOP
+15V
R138 33K
C185 .1
R139 4.7K
GND1 GND12
J11 SUMLV
J12 SUMLV
TO SUM LOOP
DSUMLV J17 21
C202 100PF
FROM A11 MOD CONTROL
DGT256L
+15V
C319 .1
DG256L J17 10
C186 100PF
Z5-A 2 1 1K
U21-A 2 3 4 11 1
GT256H
C320 .1
-15V
U21-D 13 12 14
1HAFH2
D1HAFH J17 14
C188 100PF
Z5-C 6 5 1K
D1HAFL J17 23
C190 100PF
D1HAFL
U22-D 13 12 14
2HAFH2
D2HAFH J17 18
C192 100PF
R60 1K
D2HAFH
D2HAFL J17 24
C194 100PF
D2HAFL
D3HAFL
D3HAFL J17 12
C196 100PF
Z5-B 4 3 1K
U21-B 6 5 7
3HAFH
D4HAFL
D4HAFL J17 16
C198 100PF
Z5-D 8 7 1K
U21-C 9 10 8
4HAFH
+15V
C323 .1
DGT180H J17 20
C200 100PF
R61 1K
U22-A 2 3 4 11 1
GT180H
C324 .1
-15V

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS INDICATED FUNCTION AS INDUCTORS IN THIS CIRCUIT. (<0.02 OHMS, 0.000W)
2. ALL RESISTOR VALUES ARE IN OHMS. ALL CAPACITOR VALUES ARE IN MICROFARADS. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

6082A-1046
(1 of 3)

Figure 10-9. A10 Premodulator PCA (cont)


HADCTH
C28
1000PF
C380
100PF
R30
1K
R31
1K
R32
1K
R33
1K
R34
1K
R277
1K
L15
.68
L16
.68
L17
.68
CR14
CR15
CR16
C40
100PF
C41
100PF
C42
100PF
C37
5.6PF
C38
5.6PF
C39
3.3PF
C364
1.2PF
C363
1.2PF
C362
1.2PF
CR17
CR18
CR19
C34
2.2PF
C35
1.2PF
C36
3.9PF
C43
2.2PF
C44
2.2PF
C45
1.8PF
+5V
MDIH
R5
2K
Q1
C4
100PF
CR20
C6
100PF
C8
1000PF
C13
1000PF
C14
5.6PF
R15
47
R16
47
U2
÷2
C10
1000PF
C9
100PF
L3
.12
R310
R300
1
1
+15V
C22
1000PF
R24
422
R25
300W
R305
1
CR1
CR3
CR9
C33
3.3PF
CR10
6dBm
400-1060 MHZ J5
FROM SUM LOOP
VCO, A9
R1
220
R2
22
C2
100PF
R3
220
CR2
R6
130
C11
4.7PF
R7
47
R8
47
R13
39
R12
130
CR4
R14
130
C20
100PF
U4
C18
100PF
R21
130
R22
39
C23
100
R23
130
U5
C25
100PF
C24
1.5PF
C342
1.5PF
C341
3.0PF
C344
1PF
C343
3.0PF
C31
100PF
C345
1.5PF
CR11
CR12
CR13
C375
1.0PF
L107
.12
256-1060MHZ
R4
1.5K
R301
R302
1
1
C361
0.68PF
R20
1.5K
R276
1K
MIDH
C26
1000PF
C381
100PF
MIDH
C12
100PF

FREQ	.01 - 258$^-$	256$^+$ - 350$^-$	350$^+$ - 512$^-$	512$^+$ - 730$^-$	730$^+$ - 1056
MIDTH	+12V	+12V	+12V	-13V	-13V
HADCTH	-13V	+12V	-13V	-13V	+12V

6082A-1046
(2 of 3)

Figure 10-9. A10 Premodulator PCA

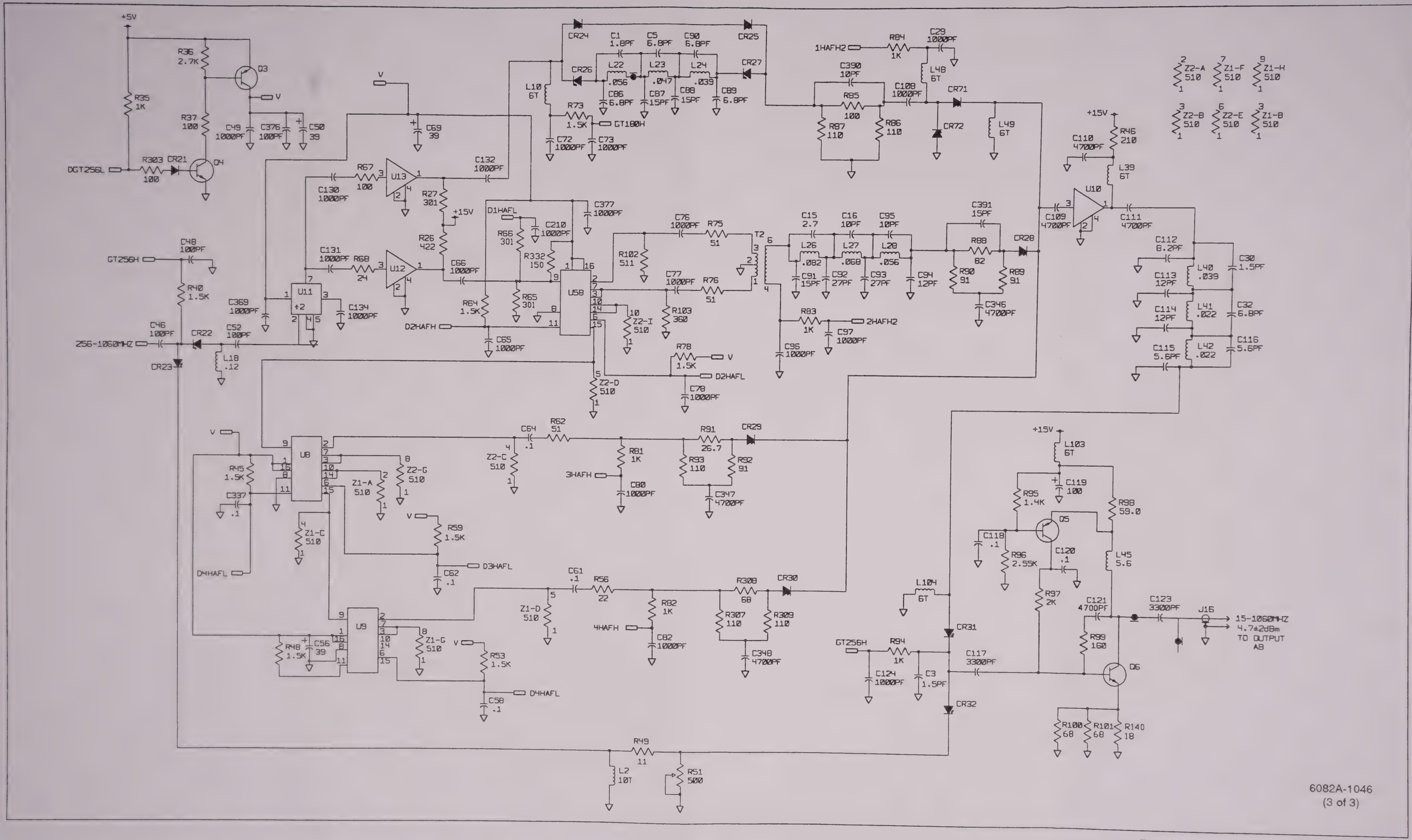

+5V
R36 2.7K
Q3
R35 1K
R37 100
V
C49 1000PF
C376 100PF
C50 39
DGT256L
R303 100
CR21
Q4
V
C69 39
R67 100
U13
C130 1000PF
C132 1000PF
R27 301
+15V
R26 422
C131 1000PF
R68 24
U12
C66 1000PF
GT256H
C48 100PF
R40 1.5K
U11
÷2
C369 1000PF
C134 1000PF
C46 100PF
256-1060MHZ
CR22
C52 100PF
L18 .12
CR23
D1HAFL
C210 1000PF
R66 301
R332 150
C377 1000PF
U58
R64 1.5K
R65 301
D2HAFH
C65 1000PF
CR24
C1 1.8PF
C5 6.8PF
C90 6.8PF
CR25
CR26
L22 .056
L23 .047
L24 .039
CR27
L10 6T
C86 6.8PF
C87 15PF
C88 15PF
C89 6.8PF
R73 1.5K
GT180H
C72 1000PF
C73 1000PF
C76 1000PF
R75 51
T2
R102 511
C77 1000PF
R76 51
R103 360
Z2-I 510
R78 1.5K
D2HAFL
C78 1000PF
Z2-D 510
1HAFH2
R84 1K
C29 1000PF
L48 6T
C390 10PF
R85 100
C108 1000PF
CR71
R87 110
R86 110
CR72
L49 6T
C15 2.7
C16 10PF
C95 10PF
L26 .082
L27 .068
L28 .056
C91 15PF
C92 27PF
C93 27PF
C94 12PF
R83 1K
2HAFH2
C96 1000PF
C97 1000PF
C391 15PF
R88 82
CR28
R90 91
R89 91
C346 4700PF
Z2-A 510
Z1-F 510
Z1-H 510
Z2-B 510
Z2-E 510
Z1-B 510
+15V
R46 210
C110 4700PF
L39 6T
U10
C109 4700PF
C111 4700PF
C112 8.2PF
C30 1.5PF
C113 12PF
L40 .039
C114 12PF
L41 .022
C32 6.8PF
C115 5.6PF
L42 .022
C116 5.6PF
V
U8
R45 1.5K
C337 .1
Z1-C 510
D4HAFL
Z1-A 510
Z2-G 510
C64 .1
R62 51
Z2-C 510
R81 1K
3HAFH
C80 1000PF
R91 26.7
CR29
R93 110
R92 91
C347 4700PF
V
R59 1.5K
D3HAFL
C62 .1
C61 .1
R56 22
Z1-D 510
R82 1K
4HAFH
C82 1000PF
R308 68
CR30
R307 110
R309 110
C348 4700PF
U9
R48 1.5K
C56 39
Z1-G 510
V
R53 1.5K
D4HAFL
C58 .1
R49 11
L2 10T
R51 500
+15V
L103 6T
C119 100
R95 1.4K
Q5
R98 59.0
C118 .1
R96 2.55K
C120 .1
L45 5.6
L104 6T
R97 2K
C121 4700PF
C123 3300PF
J16
15-1060MHZ
4.7±2dBm
TO OUTPUT
A8
CR31
R99 160
GT256H
R94 1K
C117 3300PF
C124 1000PF
C3 1.5PF
Q6
CR32
R100 68
R101 68
R140 18
6082A-1046
(3 of 3)

Figure 10-9. A10 Premodulator PCA (cont)

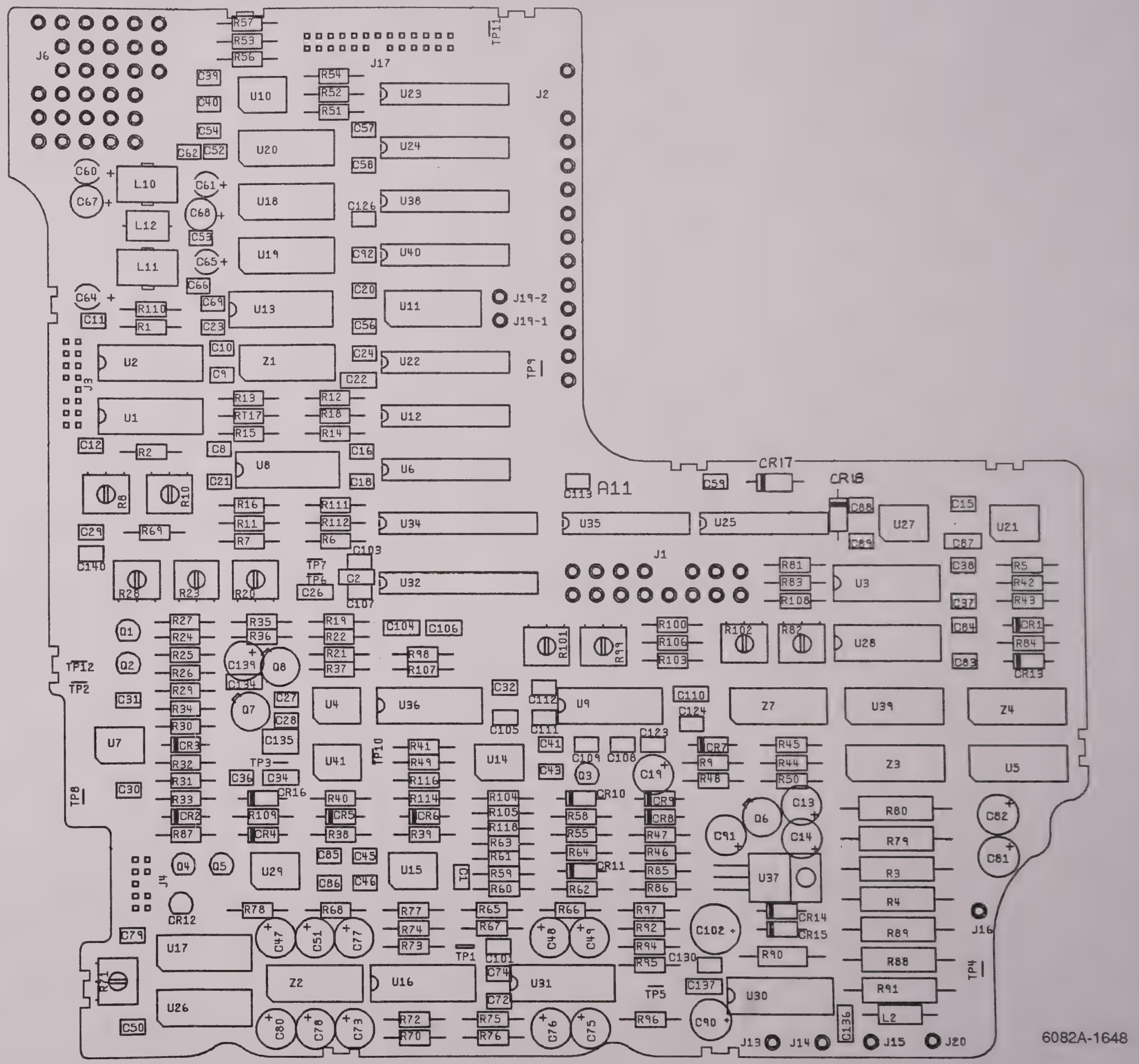
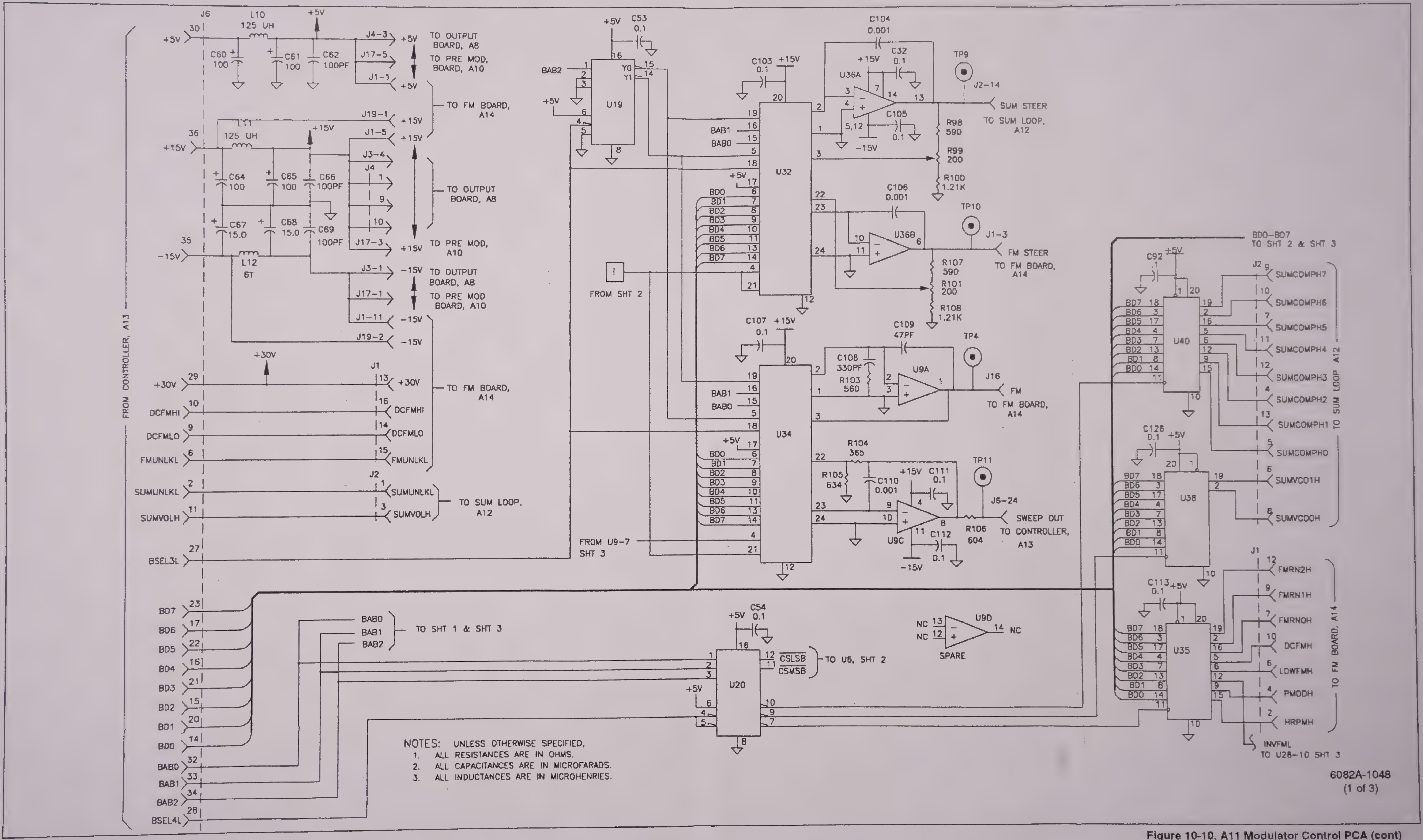

J6
R57
R53
R56
J17
TP11
J2
C39
C40
C54
U10
R54
R52
R51
U23
C57
U24
C58
C62
C52
U20
C60
C67
L10
C61
C68
U18
C126
U38
L12
C53
L11
C65
U19
C92
U40
C66
C64
R110
C69
U13
C20
U11
J19-2
J19-1
C11
R1
C23
C56
C10
U2
Z1
C24
U22
TP9
C9
C22
J3
U1
R13
RT17
R15
R12
R18
R14
U12
C12
R2
C8
C16
U8
U6
C18
R8
R10
C21
R16
R11
R7
R111
R112
R6
C103
U34
A11
C113
U35
U25
CR17
C59
CR18
C88
U27
C15
U21
C29
R69
C140
TP7
TP6
C2
C107
U32
C89
C87
J1
R81
R83
R108
U3
C38
R5
R42
R43
C37
R28
R23
R20
C26
R27
R24
R25
R26
R29
R34
R30
CR3
R32
R31
R33
CR2
R87
Q1
Q2
TP12
TP2
R35
R36
C139
Q8
C134
R19
R22
R21
R37
R98
R107
C104
C106
R101
R99
R100
R106
R103
R102
R82
U28
C84
CR1
R84
CR13
C83
C31
Q7
C27
C28
C135
U4
U36
C32
C112
U9
C110
C124
Z7
U39
Z4
C105
C111
C123
U7
TP3
U41
TP10
R41
R49
R116
U14
C41
C109
C108
CR7
R9
R48
R45
R44
R50
Z3
U5
C30
TP8
C36
C34
CR16
R40
CR5
R38
R109
CR4
R114
CR6
R39
R104
R105
R118
R63
R61
R59
R60
C43
Q3
C19
CR10
R58
R55
R64
CR11
R62
CR9
CR8
R47
R46
R85
R86
Q6
C13
C91
C14
R80
R79
R3
R4
U37
C82
C81
J16
J4
Q4
Q5
U29
C85
C45
C86
C46
U15
C1
CR12
R78
R68
R77
R74
R73
R65
R67
R66
C47
C51
C77
C48
C49
TP1
C101
R97
R92
R94
R95
C130
C102
CR14
CR15
R90
R89
R88
TP4
C79
R21
U17
U26
C50
Z2
U16
C74
U31
C72
TP5
C137
U30
R91
L2
C136
C80
C78
C73
R72
R70
R75
R76
C76
C75
R96
C90
J13
J14
J15
J20
6082A-1648

Figure 10-10. A11 Modulator Control PCA


FROM CONTROLLER, A13
J6
+5V
+15V
-15V
+30V
DCFMHI
DCFMLO
FMUNLKL
SUMUNLKL
SUMVOLH
BSEL3L
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
BAB0
BAB1
BAB2
BSEL4L
L10 125 UH
L11 125 UH
L12 6T
C60 100
C61 100
C62 100PF
C64 100
C65 100
C66 100PF
C67 15.0
C68 15.0
C69 100PF
J4-3
J17-5
J1-1
J19-1
J1-5
J3-4
J17-3
J3-1
J17-1
J1-11
J19-2
TO OUTPUT BOARD, A8
TO PRE MOD, BOARD, A10
TO FM BOARD, A14
TO OUTPUT BOARD, A8
TO PRE MOD, A10
TO OUTPUT BOARD, A8
TO PRE MOD BOARD, A10
TO FM BOARD, A14
TO SUM LOOP, A12
BAB0
BAB1
BAB2
TO SHT 1 & SHT 3
U19
YO
Y1
C53 0.1
U32
U34
U20
C103 0.1
C107 0.1
C54 0.1
CSLSB
CSMSB
TO U6, SHT 2
FROM SHT 2
FROM U9-7 SHT 3
U36A
U36B
U9A
U9C
U9D
SPARE
NC
C104 0.001
C32 0.1
C105 0.1
C106 0.001
C108 330PF
C109 47PF
C110 0.001
C111 0.1
C112 0.1
R98 590
R99 200
R100 1.21K
R107 590
R101 200
R108 1.21K
R103 560
R104 365
R105 634
R106 604
TP9
TP10
TP4
TP11
J2-14
SUM STEER
TO SUM LOOP, A12
J1-3
FM STEER
TO FM BOARD, A14
J16
FM
TO FM BOARD, A14
J6-24
SWEEP OUT
TO CONTROLLER, A13
BD0-BD7
TO SHT 2 & SHT 3
U40
U38
U35
C92 .1
C126 0.1
C113 0.1
SUMCOMPH7
SUMCOMPH6
SUMCOMPH5
SUMCOMPH4
SUMCOMPH3
SUMCOMPH2
SUMCOMPH1
SUMCOMPH0
SUMVCO1H
SUMVCO0H
TO SUM LOOP A12
FMRN2H
FMRN1H
FMRN0H
DCFMH
LOWFMH
PMODH
HRPMH
TO FM BOARD, A14
INVFML
TO U28-10 SHT 3

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES ARE IN OHMS.
2. ALL CAPACITANCES ARE IN MICROFARADS.
3. ALL INDUCTANCES ARE IN MICROHENRIES.

6082A-1048
(1 of 3)

Figure 10-10. A11 Modulator Control PCA (cont)

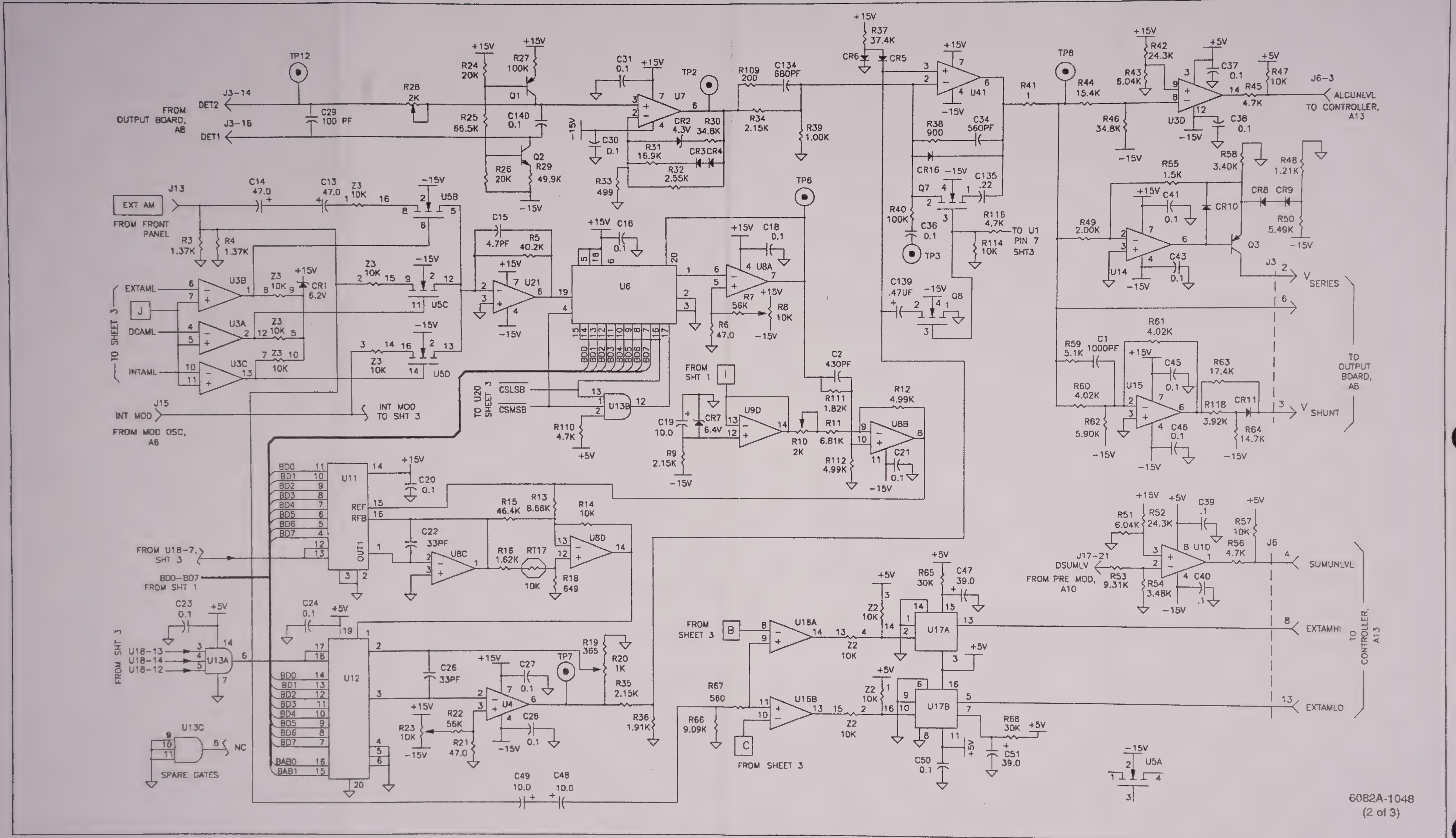

FROM OUTPUT BOARD, A8
J3-14
DET2
J3-16
DET1
TP12
C29 100 PF
R28 2K
Q1
Q2
R24 20K
R27 100K
R25 66.5K
R26 20K
R29 49.9K
C140 0.1
C31 0.1
U7
TP2
CR2 4.3V
R30 34.8K
R31 16.9K
CR3 CR4
R32 2.55K
R33 499
C30 0.1
R109 200
C134 680PF
R34 2.15K
R39 1.00K
R37 37.4K
CR6 CR5
U41
R38 900
C34 560PF
CR16
Q7
C135 .22
R40 100K
C36 0.1
TP3
R116 4.7K
TO U1 PIN 7 SHT3
R114 10K
C139 .47UF
Q8
R41 1
TP8
R44 15.4K
R46 34.8K
R42 24.3K
R43 6.04K
U3D
C37 0.1
C38 0.1
R45 4.7K
R47 10K
J6-3
ALCUNLVL TO CONTROLLER, A13
R55 1.5K
R58 3.40K
R48 1.21K
CR8 CR9
CR10
R50 5.49K
R49 2.00K
C41 0.1
U14
C43 0.1
Q3
J3
V SERIES
R61 4.02K
R59 5.1K
C1 1000PF
C45 0.1
U15
R60 4.02K
R62 5.90K
C46 0.1
R63 17.4K
R118 3.92K
CR11
R64 14.7K
V SHUNT
TO OUTPUT BOARD, A8
J13
EXT AM
FROM FRONT PANEL
C14 47.0
C13 47.0
Z3 10K
U5B
R3 1.37K
R4 1.37K
TO SHEET 3
EXTAML
U3B
CR1 6.2V
U5C
DCAML
U3A
INTAML
U3C
U5D
J15
INT MOD
FROM MOD OSC, A6
INT MOD TO SHT 3
C15 4.7PF
R5 40.2K
U21
C16 0.1
U6
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7
U8A
C18 0.1
R7 56K
R8 10K
R6 47.0
TP6
TO U20 SHEET 3
CSLSB
CSMSB
U13B
R110 4.7K
FROM SHT 1
U9D
C19 10.0
CR7 6.4V
R9 2.15K
R10 2K
R11 6.81K
C2 430PF
R111 1.82K
R12 4.99K
U8B
R112 4.99K
C21 0.1
U11
C20 0.1
REF
RFB
OUT1
R15 46.4K
R13 8.66K
R14 10K
C22 33PF
U8C
R16 1.62K
RT17 10K
U8D
R18 649
FROM U18-7, SHT 3
BD0-BD7 FROM SHT 1
C23 0.1
FROM SHT 3
U18-13
U18-14
U18-12
U13A
U13C
NC
SPARE GATES
C24 0.1
U12
BAB0
BAB1
C26 33PF
U4
C27 0.1
TP7
R19 365
R20 1K
R35 2.15K
R36 1.91K
R22 56K
R23 10K
R21 47.0
C28 0.1
C49 10.0
C48 10.0
FROM SHEET 3
U16A
U16B
R67 560
R66 9.09K
FROM SHEET 3
Z2 10K
U17A
U17B
R65 30K
C47 39.0
C50 0.1
R68 30K
C51 39.0
EXTAMHI
EXTAMLO
TO CONTROLLER, A13
R51 6.04K
R52 24.3K
C39 .1
U10
R57 10K
R56 4.7K
J5
SUMUNLVL
J17-21
DSUMLV
FROM PRE MOD, A10
R53 9.31K
R54 3.48K
C40 .1
U5A
+15V
-15V
+5V
6082A-1048 (2 of 3)

Figure 10-10. A11 Modulator Control PCA (cont)

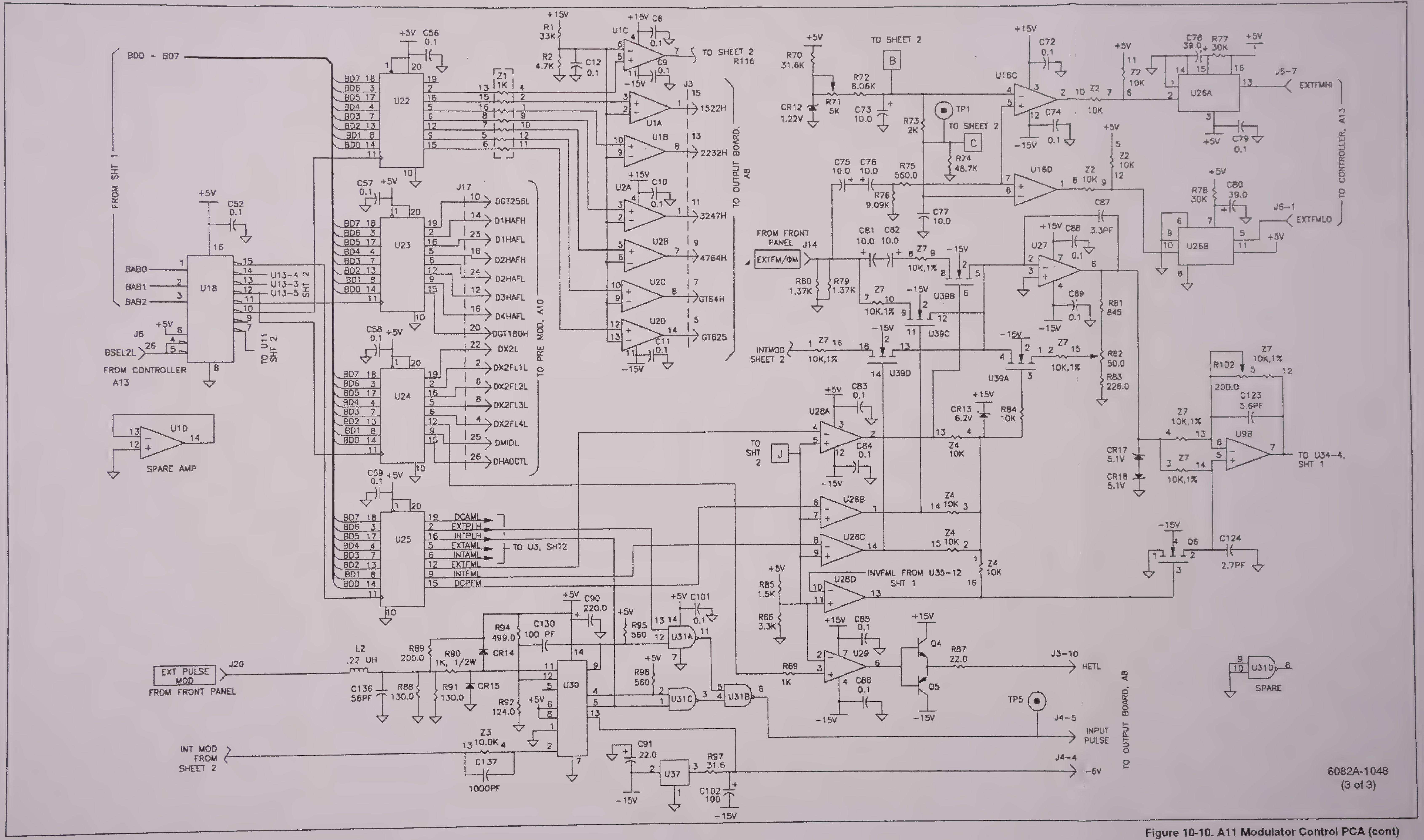
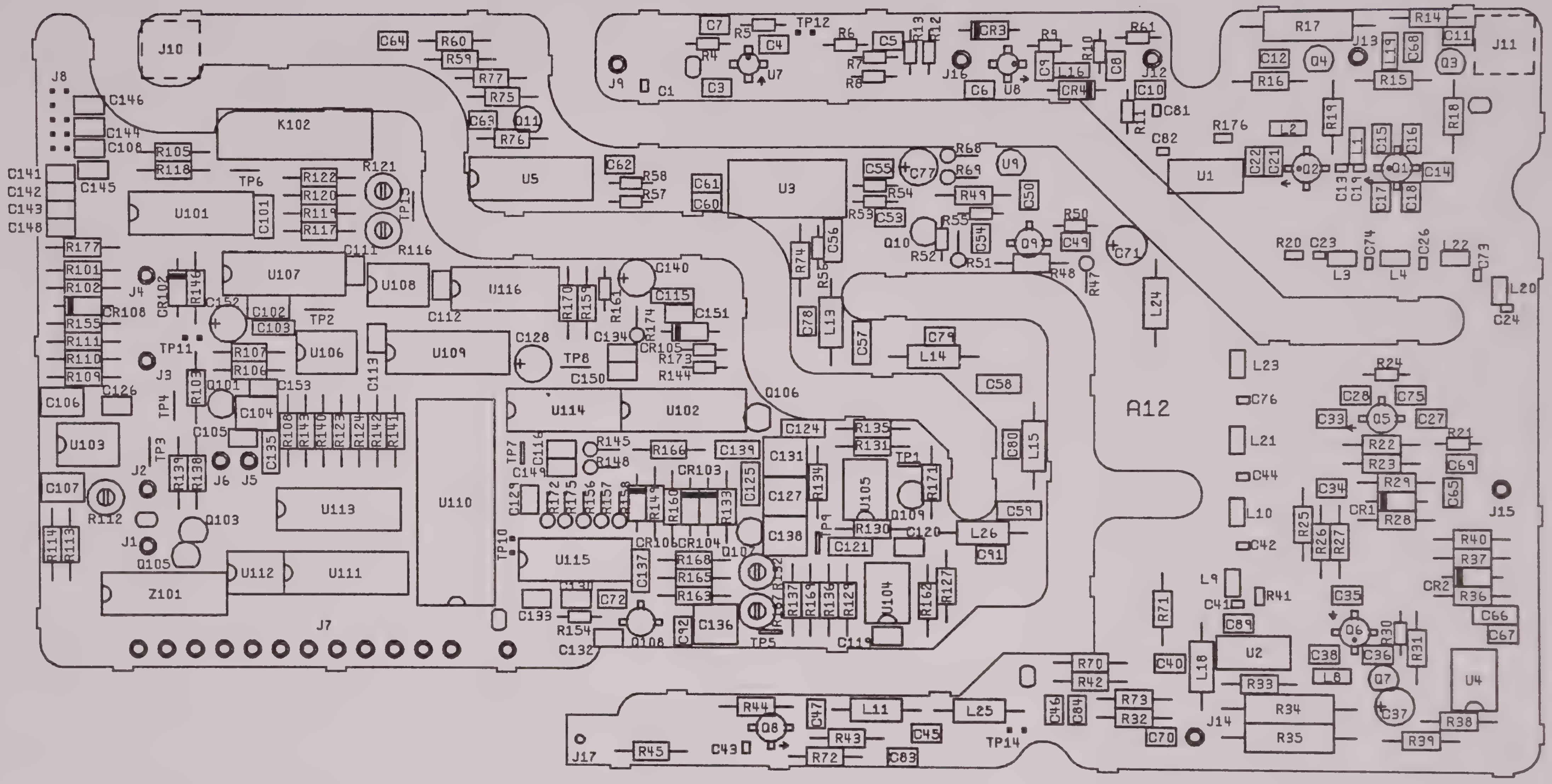
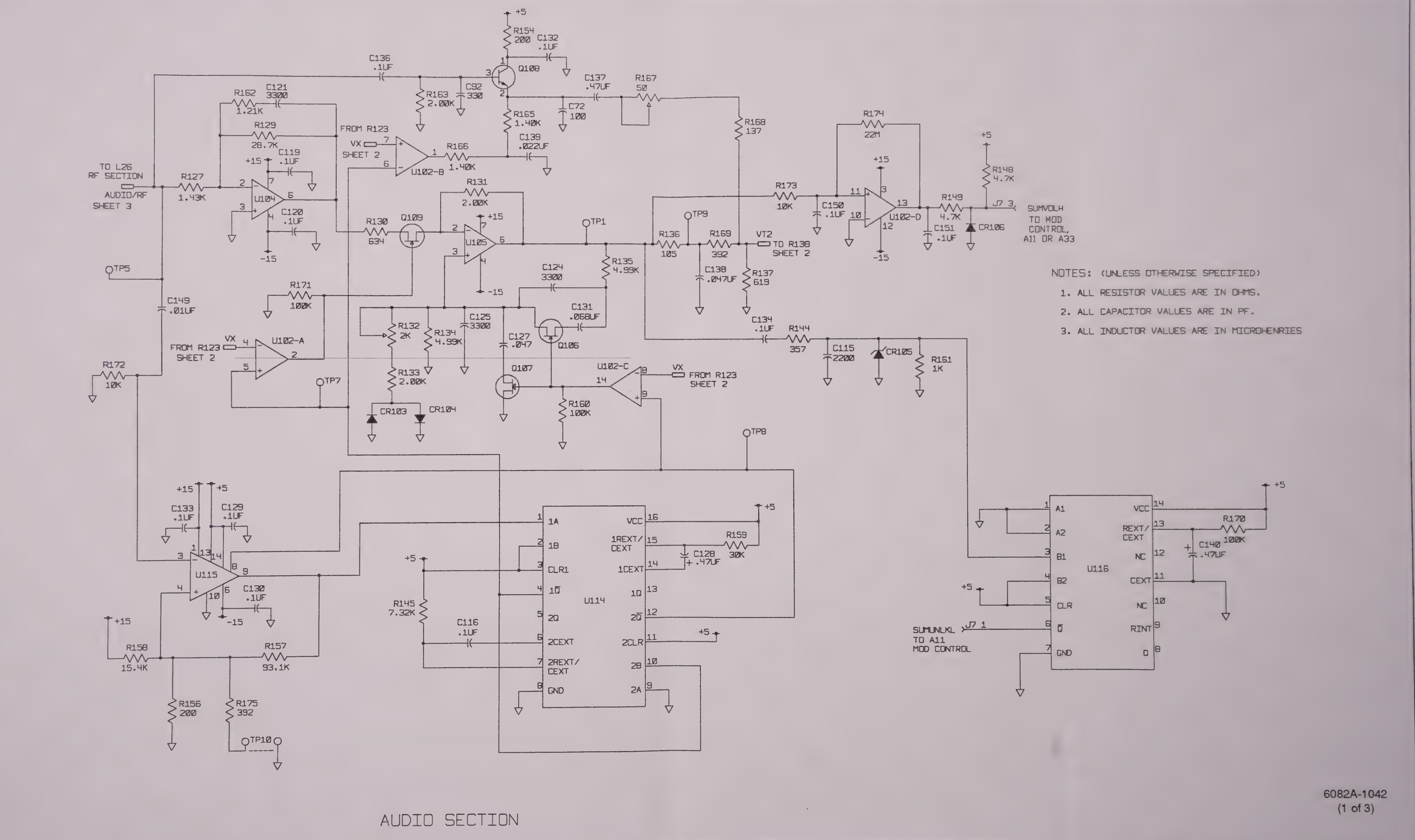

BD0 - BD7
FROM SHT 1
U22
U23
U24
U25
U18
BAB0
BAB1
BAB2
BSEL2L
J6
FROM CONTROLLER A13
U13-4
U13-3
U13-5
SHT 2
TO U11 SHT 2
U1D
SPARE AMP
Z1 1K
J17
DGT256L
D1HAFH
D1HAFL
D2HAFH
D2HAFL
D3HAFL
D4HAFL
DGT180H
DX2L
DX2FL1L
DX2FL2L
DX2FL3L
DX2FL4L
DMIDL
DHADCTL
TO PRE MOD, A10
DCAML
EXTPLH
INTPLH
EXTAML
INTAML
EXTFML
INTFML
DCPFM
TO U3, SHT2
U1C
U1A
U1B
U2A
U2B
U2C
U2D
TO SHEET 2 R116
J3
1522H
2232H
3247H
4764H
GT64H
GT625
TO OUTPUT BOARD, A8
R1 33K
R2 4.7K
C12 0.1
C8
C9 0.1
C10 0.1
C11 0.1
C56 0.1
C57 0.1
C58 0.1
C59 0.1
C52 0.1
+5V
+15V
-15V
TO SHEET 2
B
C
J
TP1
R70 31.6K
R71 5K
R72 8.06K
CR12 1.22V
C73 10.0
R73 2K
R74 48.7K
C75 10.0
C76 10.0
R75 560.0
R76 9.09K
C77 10.0
U16C
U16D
C72 0.1
C74 0.1
Z2 10K
U26A
U26B
C78 39.0
R77 30K
C79 0.1
R78 30K
C80 39.0
J6-7
EXTFMHI
J6-1
EXTFMLO
TO CONTROLLER, A13
FROM FRONT PANEL
J14
EXTFM/ΦM
R80 1.37K
R79 1.37K
C81 10.0
C82 10.0
Z7 10K,1%
U27
C88
C87 3.3PF
C89 0.1
R81 845
R82 50.0
R83 226.0
U39A
U39B
U39C
U39D
INTMOD SHEET 2
CR13 6.2V
R84 10K
U28A
U28B
U28C
U28D
C83 0.1
C84 0.1
TO SHT 2
Z4 10K
INVFML FROM U35-12 SHT 1
R85 1.5K
R86 3.3K
CR17 5.1V
CR18 5.1V
R102 200.0
C123 5.6PF
U9B
TO U34-4, SHT 1
Q6
C124 2.7PF
EXT PULSE MOD FROM FRONT PANEL
J20
L2 .22 UH
C136 56PF
R88 130.0
R89 205.0
R90 1K, 1/2W
R91 130.0
CR14
CR15
R94 499.0
C130 100 PF
C90 220.0
R92 124.0
U30
R95 560
R96 560
U31A
U31B
U31C
C101 0.1
U29
C85 0.1
C86 0.1
R69 1K
Q4
Q5
R87 22.0
J3-10
HETL
TP5
J4-5
INPUT PULSE
J4-4
-6V
TO OUTPUT BOARD, A8
U31D
SPARE
INT MOD FROM SHEET 2
Z3 10.0K
C137 1000PF
C91 22.0
U37
R97 31.6
C102 100
6082A-1048
(3 of 3)

Figure 10-10. A11 Modulator Control PCA (cont)


J10
C64
R60
R59
R77
R75
C63
Q11
R76
J8
C146
C144
C108
C145
R105
R118
K102
TP6
C141
C142
C143
C148
U101
C101
R122
R120
R119
R117
R121
TP13
R116
U5
C62
R58
R57
C61
C60
U3
C55
C77
R68
R69
U9
R54
R49
C50
R53
C53
R55
C54
Q10
R52
R51
Q9
C49
R50
R48
R47
C71
C7
R5
R4
C4
U7
TP12
R6
R7
R8
C5
R13
R12
CR3
J16
R9
Q8
C6
L16
R10
C8
R61
J12
C9
CR4
C10
R11
C81
C82
J9
C1
C3
R17
R14
C11
J11
C12
Q4
J13
L19
C68
Q3
R16
R15
R19
R18
R176
L2
U1
C22
C21
Q2
C13
C19
L1
C15
C16
Q1
C17
C18
C14
R20
C23
L3
C74
L4
C26
L22
C73
L20
C24
R177
R101
R102
CR108
R155
R111
R110
R109
J4
CR102
R146
U107
C111
U108
U116
C140
C152
C102
C103
TP2
C112
R170
R159
R161
C115
C151
R174
C134
CR105
R173
R144
R74
R56
C56
L13
C78
C57
C79
L14
C58
Q106
L24
TP11
R107
R106
U106
U109
C128
TP8
C150
J3
R103
Q101
C153
C113
C106
C126
TP4
C104
C105
U103
TP3
R108
R143
R140
R123
R124
R142
R141
C135
U114
U102
U110
C124
R135
R131
TP1
C80
L15
A12
L23
C76
R24
C28
C75
C33
Q5
C27
L21
R22
R21
R23
C69
C44
C107
J2
R139
R138
J6
J5
R112
Q103
J1
R114
R113
Q105
U113
TP7
C116
C149
R145
R148
R166
C139
C131
CR103
C125
C127
R134
U105
R171
Q109
C120
L26
C59
C91
R130
C136
C121
R172
R175
R156
R157
R158
R149
R160
R133
C129
CR106
CR104
Q107
TP10
U115
C137
R168
R165
R163
R132
R137
R169
R136
R129
U104
R162
R127
C119
TP5
C133
R154
C72
Q108
C132
C136
U112
U111
Z101
J7
L10
C42
C34
R29
CR1
R28
C65
J15
R25
R26
R27
R40
R37
CR2
R36
L9
C41
R41
C35
R71
C89
Q6
R30
R31
C66
C67
U2
C38
C36
L18
C40
L8
Q7
U4
R70
R42
R33
R73
R32
R34
C37
J14
R35
C70
R39
R38
R44
C47
L11
L25
C46
C84
Q8
R43
C45
J17
R45
C43
R72
C83
TP14

6082A-1642

Figure 10-11. A12 Sum Loop PCA


+5
R154 200
C132 .1UF
C136 .1UF
Q108
R162 1.21K
C121 3300
R163 2.00K
C92 330
C137 .47UF
R167 50
R129 28.7K
R165 1.40K
C72 100
R168 137
FROM R123
VX
SHEET 2
U102-B
R166 1.40K
C139 .022UF
R174 22M
+15
C119 .1UF
TO L26
RF SECTION
AUDIO/RF
SHEET 3
R127 1.43K
U104
C120 .1UF
-15
R131 2.00K
R130 634
Q109
U105
TP1
TP9
R173 10K
C150 .1UF
U102-D
R149 4.7K
R148 4.7K
J7 3
SUMVOLH
TO MOD
CONTROL,
A11 OR A33
C151 .1UF
CR106
R136 105
R169 392
VT2
TO R138
SHEET 2
C138 .047UF
R137 619
TP5
R171 100K
R135 4.99K
C124 3300
C149 .01UF
R132 2K
R134 4.99K
C125 3300
C131 .068UF
C127 .047
Q106
C134 .1UF
R144 357
C115 2200
CR105
R161 1K
FROM R123
SHEET 2
U102-A
R172 10K
TP7
R133 2.00K
Q107
U102-C
R160 100K
CR103
CR104
TP8
+15
+5
C133 .1UF
C129 .1UF
U115
C130 .1UF
-15
R158 15.4K
R157 93.1K
R156 200
R175 392
TP10
R145 7.32K
C116 .1UF
U114
1A
1B
CLR1
1Q̄
2Q
2CEXT
2REXT/CEXT
GND
VCC
1REXT/CEXT
1CEXT
1Q
2Q̄
2CLR
2B
2A
R159 30K
C128 .47UF
U116
A1
A2
B1
B2
CLR
Q̄
GND
VCC
REXT/CEXT
NC
CEXT
NC
RINT
Q
R170 100K
C140 .47UF
SUMUNLKL
J7 1
TO A11
MOD CONTROL

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL CAPACITOR VALUES ARE IN PF.
3. ALL INDUCTOR VALUES ARE IN MICROHENRIES

AUDIO SECTION

6082A-1042
(1 of 3)

Figure 10-11. A12 Sum Loop PCA (cont)

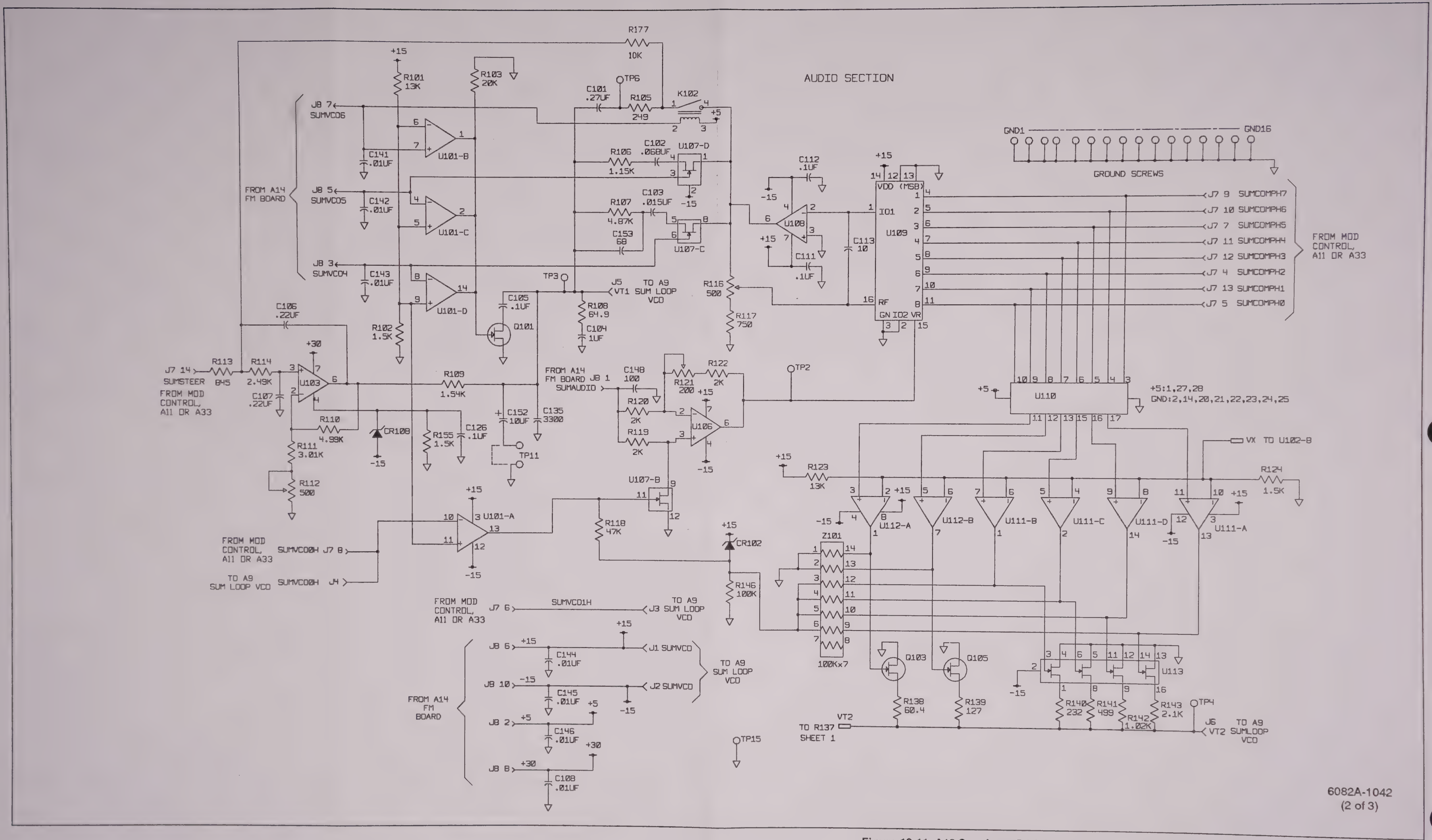

AUDIO SECTION
R177
10K
+15
R101
13K
R103
20K
TP6
C101
.27UF
R105
249
K102
+5
J8 7
SUMVC06
U101-B
C141
.01UF
R106
1.15K
C102
.068UF
U107-D
-15
FROM A14
FM BOARD
J8 5
SUMVC05
C142
.01UF
U101-C
R107
4.87K
C103
.015UF
C153
68
U107-C
J8 3
SUMVC04
C143
.01UF
U101-D
TP3
J5
VT1
TO A9
SUM LOOP
VCO
C105
.1UF
R108
64.9
C104
1UF
Q101
R102
1.5K
C106
.22UF
+30
J7 14
SUMSTEER
R113
845
R114
2.49K
U103
C107
.22UF
FROM MOD
CONTROL,
A11 OR A33
R109
1.54K
C152
10UF
C135
3300
R110
4.99K
CR100
R155
1.5K
C126
.1UF
TP11
R111
3.01K
R112
500
FROM A14
FM BOARD J8 1
SUMAUDIO
C148
100
R121
200
R122
2K
R120
2K
R119
2K
U106
U107-B
R118
47K
U101-A
FROM MOD
CONTROL,
A11 OR A33
SUMVC00H J7 8
TO A9
SUM LOOP VCO
SUMVC00H J4
FROM MOD
CONTROL,
A11 OR A33
J7 6
SUMVC01H
TO A9
J3 SUM LOOP
VCO
J8 6
C144
.01UF
J1 SUMVCO
J8 10
C145
.01UF
J2 SUMVCO
TO A9
SUM LOOP
VCO
FROM A14
FM
BOARD
J8 2
C146
.01UF
J8 8
C108
.01UF
C112
.1UF
U108
C111
.1UF
C113
10
R116
500
R117
750
TP2
CR102
R146
100K
TP15
U109
VDD (MSB)
IO1
RF
GN IO2 VR
GND1
GND16
GROUND SCREWS
J7 9 SUMCOMPH7
J7 10 SUMCOMPH6
J7 7 SUMCOMPH5
J7 11 SUMCOMPH4
J7 12 SUMCOMPH3
J7 4 SUMCOMPH2
J7 13 SUMCOMPH1
J7 5 SUMCOMPH0
FROM MOD
CONTROL,
A11 OR A33
U110
+5:1,27,28
GND:2,14,20,21,22,23,24,25
VX TO U102-B
R123
13K
R124
1.5K
U112-A
U112-B
U111-B
U111-C
U111-D
U111-A
Z101
100Kx7
Q103
Q105
R138
60.4
R139
127
U113
R140
232
R141
499
R142
1.02K
R143
2.1K
TP4
TO R137
SHEET 1
VT2
J6
VT2
TO A9
SUMLOOP
VCO
6082A-1042
(2 of 3)

Figure 10-11. A12 Sum Loop PCA (cont)

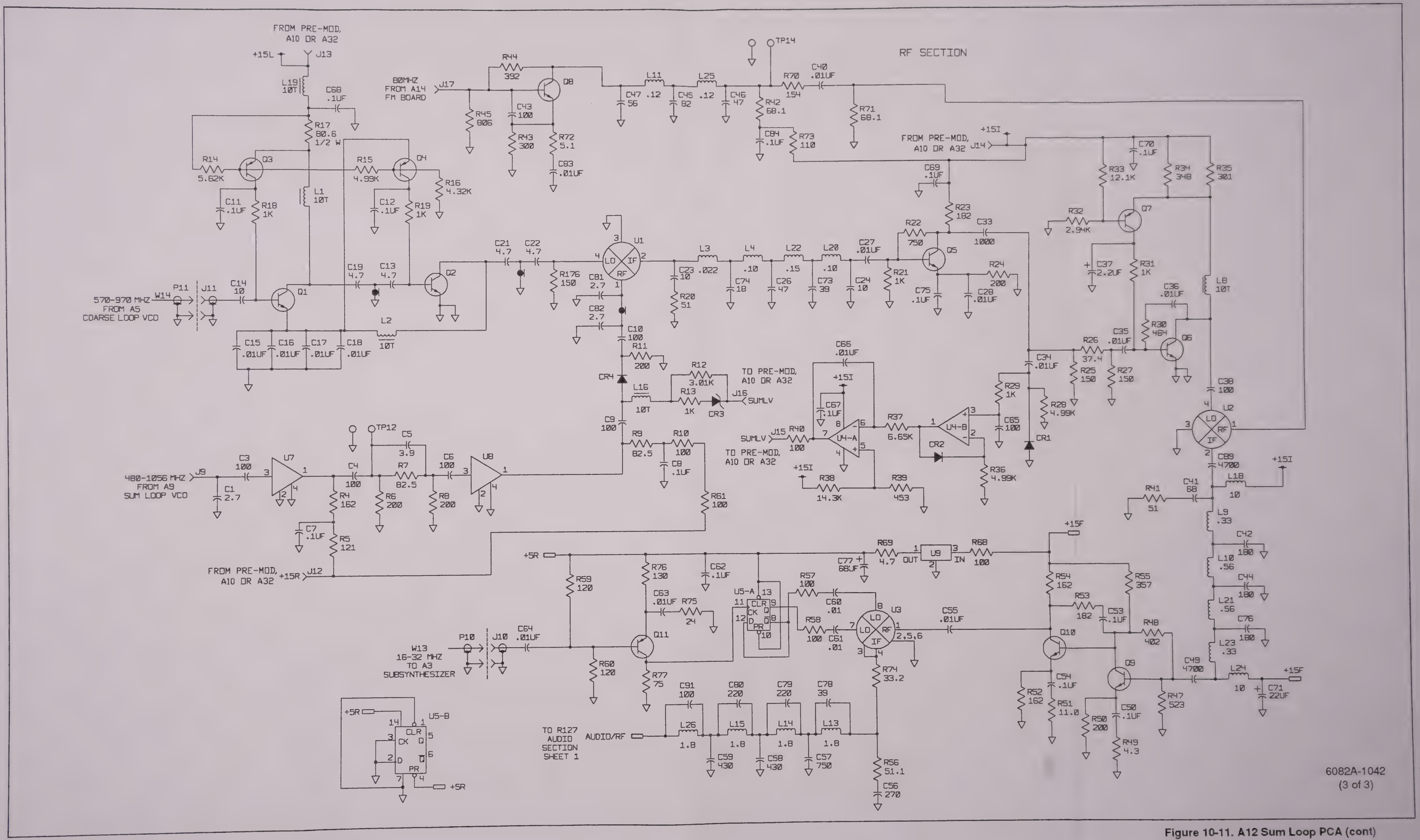

RF SECTION
FROM PRE-MOD, A10 OR A32
+15L
J13
L19 10T
C68 .1UF
R17 80.6 1/2 W
R14 5.62K
Q3
R15 4.99K
Q4
R16 4.32K
C11 .1UF
R18 1K
L1 10T
C12 .1UF
R19 1K
80MHZ FROM A14 FM BOARD
J17
R44 392
Q8
R45 806
C43 100
R43 300
R72 5.1
C83 .01UF
L11
L25
C47 56
.12
C45 82
.12
C46 47
TP14
R70 154
C40 .01UF
R42 68.1
C84 .1UF
R73 110
R71 68.1
FROM PRE-MOD, A10 OR A32
J14
+15I
C70 .1UF
R33 12.1K
R34 348
R35 301
C69 .1UF
R23 182
R32 2.94K
Q7
C33 1000
R22 750
Q5
C37 2.2UF
R31 1K
L8 10T
C21 4.7
C22 4.7
U1
LO IF RF
R176 150
C81 2.7
C82 2.7
L3 .022
L4 .10
L22 .15
L20 .10
C27 .01UF
R21 1K
R24 200
C23 10
C74 18
C26 47
C73 39
C24 10
C75 .1UF
C28 .01UF
R20 51
C36 .01UF
R30 464
Q6
570-970 MHZ FROM A5 COARSE LOOP VCO
P11
W14
J11
C14 10
Q1
C19 4.7
C13 4.7
Q2
L2 10T
C15 .01UF
C16 .01UF
C17 .01UF
C18 .01UF
C10 100
R11 200
CR4
L16 10T
R12 3.01K
R13 1K
CR3
TO PRE-MOD, A10 OR A32
J16
SUMLV
C9 100
R9 82.5
R10 100
C8 .1UF
R61 100
C66 .01UF
+15I
C67 .1UF
U4-A
SUMLV
J15
R40 100
TO PRE-MOD, A10 OR A32
R37 6.65K
U4-B
CR2
R36 4.99K
+15I
R38 14.3K
R39 453
R26 37.4
C35 .01UF
C34 .01UF
R25 150
R27 150
R29 1K
R28 4.99K
C65 100
CR1
C38 100
U2
LO RF IF
C89 4700
+15I
L18 10
R41 51
C41 68
L9 .33
C42 180
L10 .56
C44 180
L21 .56
C76 180
L23 .33
L24 10
C71 22UF
+15F
C49 4700
TP12
C5 3.9
U7
U8
480-1056 MHZ FROM A9 SUM LOOP VCO
J9
C3 100
C1 2.7
C4 100
R7 82.5
C6 100
R4 162
R6 200
R8 200
C7 .1UF
R5 121
FROM PRE-MOD, A10 OR A32
+15R
J12
+5R
R59 120
R76 130
C62 .1UF
C77 68UF
R69 4.7
U9
OUT IN
R68 100
+15F
R54 162
R55 357
R53 182
C53 .1UF
R48 402
Q10
Q9
C63 .01UF
R75 24
U5-A
CLR CK D PR Q
R57 100
C60 .01
R58 100
C61 .01
U3
LO RF IF
C55 .01UF
W13 16-32 MHZ TO A3 SUBSYNTHESIZER
P10
J10
C64 .01UF
Q11
R60 120
R77 75
R74 33.2
C54 .1UF
R52 162
R51 11.0
R50 200
C50 .1UF
R49 4.3
R47 523
+5R
U5-B
CLR CK D PR Q
+5R
TO R127 AUDIO SECTION SHEET 1
AUDIO/RF
C91 100
C80 220
C79 220
C78 39
L26 1.8
L15 1.8
L14 1.8
L13 1.8
C59 430
C58 430
C57 750
R56 51.1
C56 270
6082A-1042 (3 of 3)

Figure 10-11. A12 Sum Loop PCA (cont)

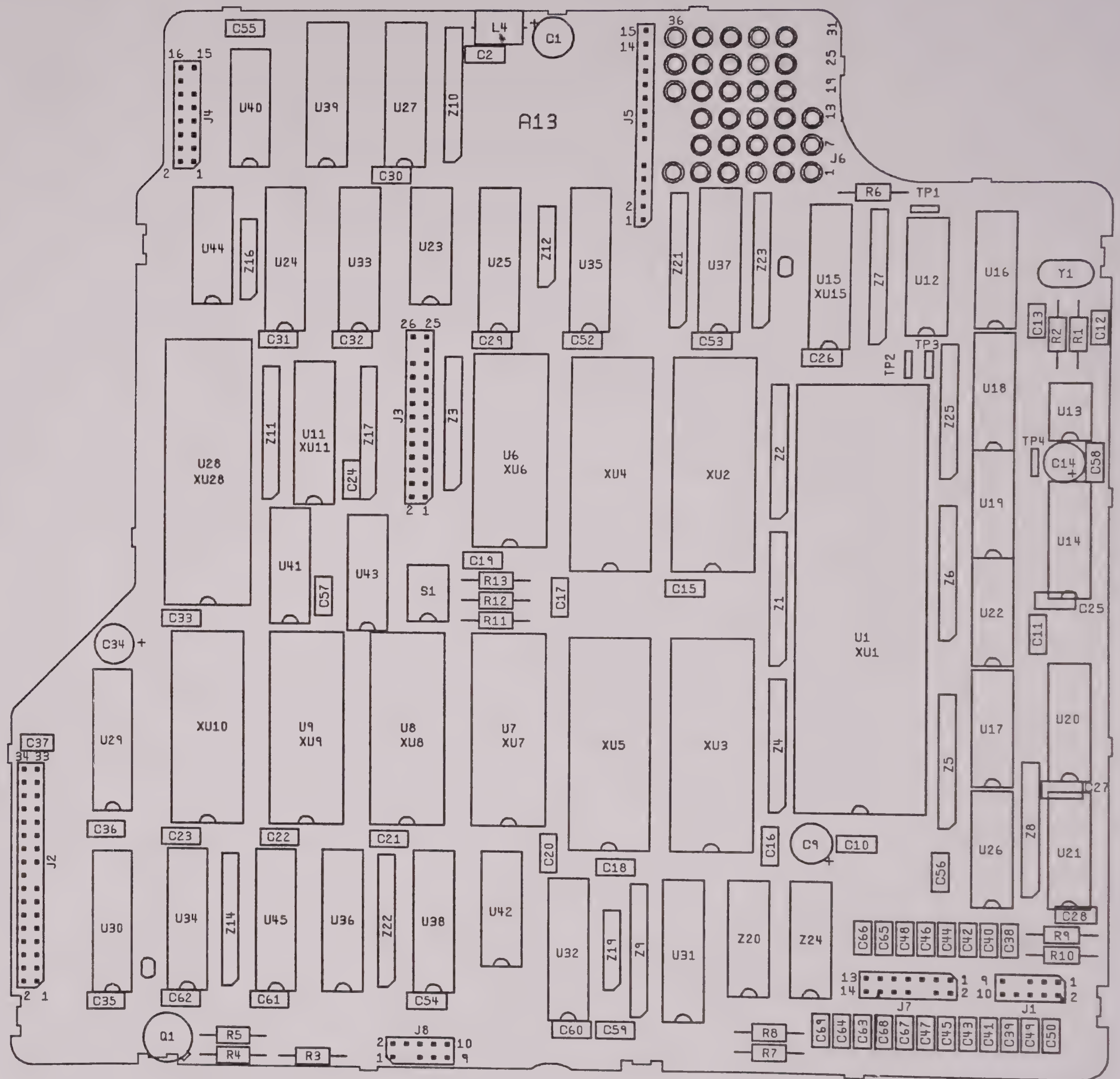
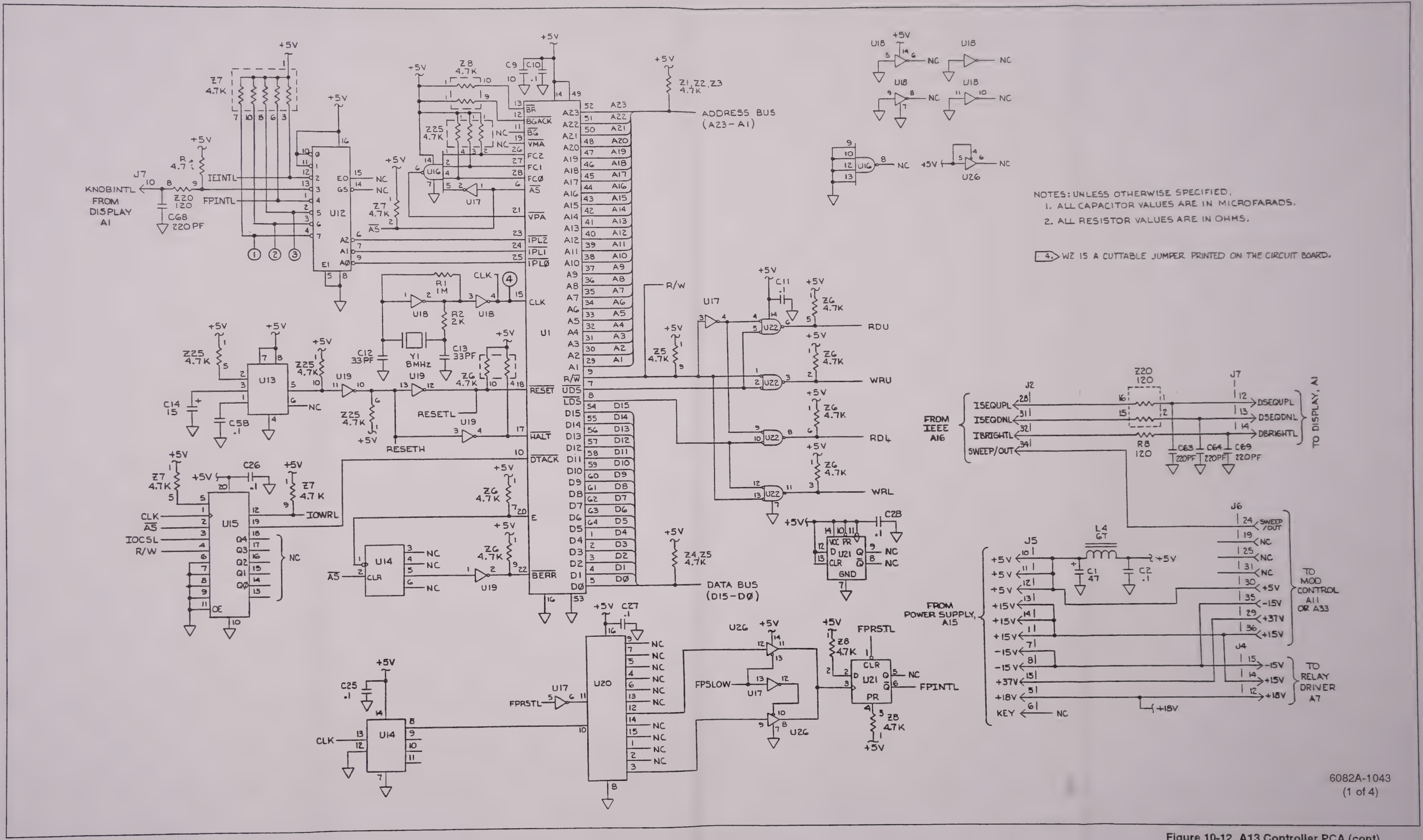

A13
C55
16 15
J4
2 1
U40
U39
U27
C30
Z10
L4
C2
C1
15
14
J5
2
1
36
31
25
19
13
7
1
J6
R6
TP1
U44
Z16
U24
U33
U23
U25
Z12
U35
Z21
U37
Z23
U15
XU15
Z7
U12
U16
Y1
C31
C32
C29
C52
C53
C26
TP3
TP2
C13
R2
R1
C12
26 25
J3
2 1
U28
XU28
Z11
U11
XU11
Z17
C24
Z3
U6
XU6
XU4
XU2
Z2
U1
XU1
Z25
U18
U13
TP4
C14
C58
U19
U14
Z6
U41
C57
U43
S1
C19
R13
R12
R11
C17
C15
Z1
U22
C25
C11
C33
C34
C37
34 33
J2
2 1
U29
XU10
U9
XU9
U8
XU8
U7
XU7
XU5
XU3
Z4
Z5
U17
U20
C27
Z8
C36
C23
C22
C21
C20
C18
C16
C9
C10
C56
U26
U21
C28
U30
U34
Z14
U45
U36
Z22
U38
U42
U32
Z19
Z9
U31
Z20
Z24
C66
C65
C48
C46
C44
C42
C40
C38
R9
R10
13
14
J7
1 9
2 10
J1
1
2
C35
C62
C61
C54
C60
C59
Q1
R5
R4
R3
J8
2
1
10
9
R8
R7
C69
C64
C63
C68
C67
C47
C45
C43
C41
C39
C49
C50
6082A-1643

Figure 10-12. A13 Controller PCA


KNOBINTL
FROM DISPLAY A1
J7
FPINTL
IEINTL
C68 220 PF
Z20 120
U12
EO
GS
A2
A1
A0
NC
U16
U17
U18
U19
U13
U14
U15
U20
U21
U22
U26
U1
Z7 4.7K
Z8 4.7K
Z25 4.7K
Z6 4.7K
Z5 4.7K
Z1,Z2,Z3 4.7K
Z4,Z5 4.7K
R1 1M
R2 2K
Y1 8MHz
C12 33PF
C13 33PF
C14 15
C58 .1
C9
C10
C11 .1
C25 .1
C26 .1
C27 .1
C28 .1
+5V
CLK
BR
BGACK
BG
VMA
FC2
FC1
FC0
AS
VPA
IPL2
IPL1
IPL0
RESET
HALT
DTACK
E
BERR
R/W
UDS
LDS
RESETL
RESETH
ADDRESS BUS (A23–A1)
DATA BUS (D15–D0)
IOWRL
IOCSL
RDU
WRU
RDL
WRL
FPRSTL
FPSLOW
FPINTL
CLR
PR
GND
J2
J4
J5
J6
ISEQUPL
ISEQDNL
IBRIGHTL
SWEEP/OUT
DSEQUPL
DSEQDNL
DBRIGHTL
FROM IEEE A16
TO DISPLAY, A1
R8 120
C63 220PF
C64 220PF
C69 220PF
L4 6T
C1 47
C2 .1
FROM POWER SUPPLY, A15
TO MOD CONTROL A11 OR A33
TO RELAY DRIVER A7
+15V
-15V
+37V
+18V
KEY
SWEEP /OUT

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.

④ WZ IS A CUTTABLE JUMPER PRINTED ON THE CIRCUIT BOARD.

6082A-1043
(1 of 4)

Figure 10-12. A13 Controller PCA (cont)

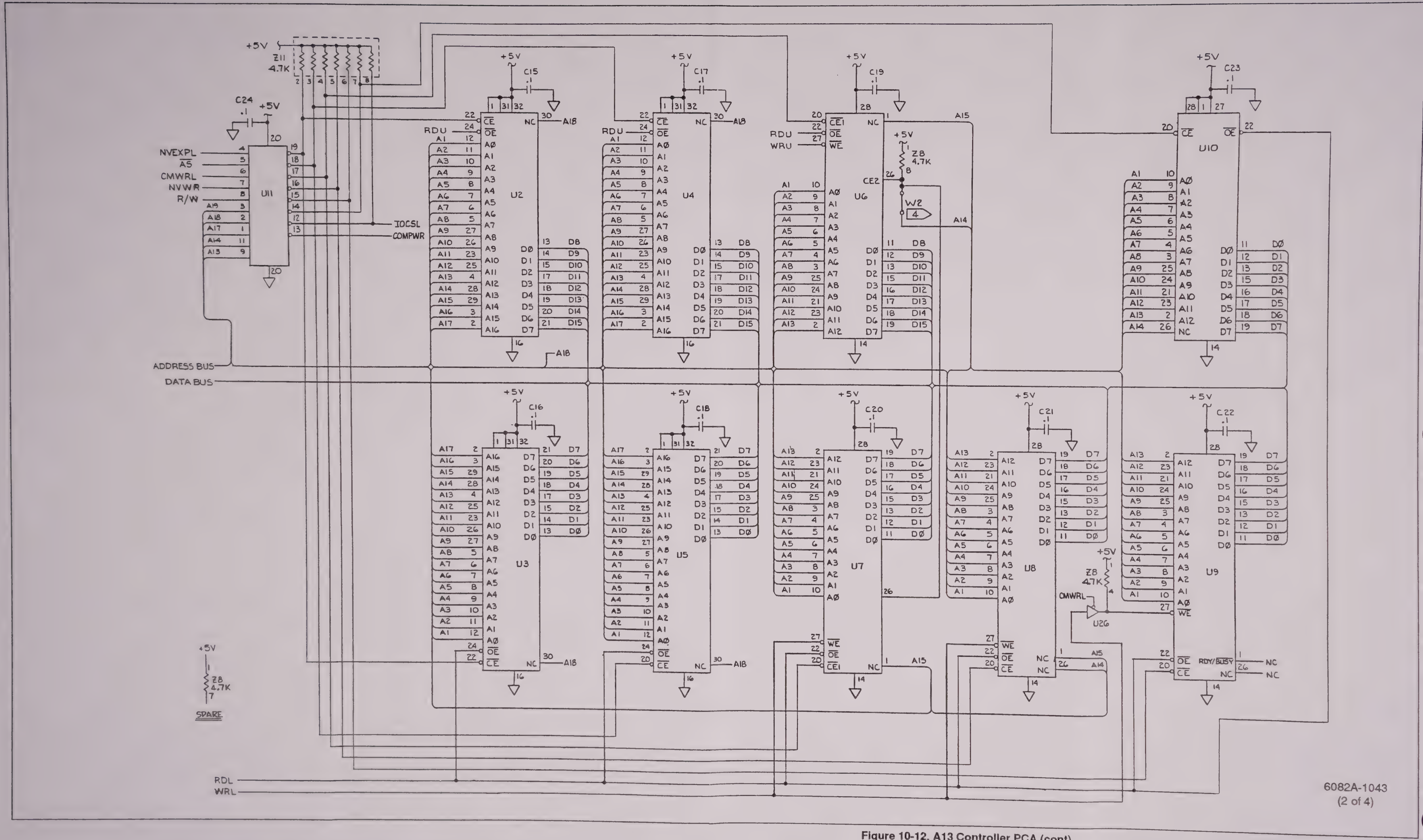

+5V
Z11 4.7K
C24 .1
NVEXPL
A5
CMWRL
NVWR
R/W
U11
IOCSL
COMPWR
U2
U3
U4
U5
U6
U7
U8
U9
U10
U26
C15
C16
C17
C18
C19
C20
C21
C22
C23
Z8 4.7K
W2
RDU
WRU
A18
A15
A14
CE2
ADDRESS BUS
DATA BUS
CMWRL
NC
SPARE
RDL
WRL
6082A-1043
(2 of 4)

Figure 10-12. A13 Controller PCA (cont)

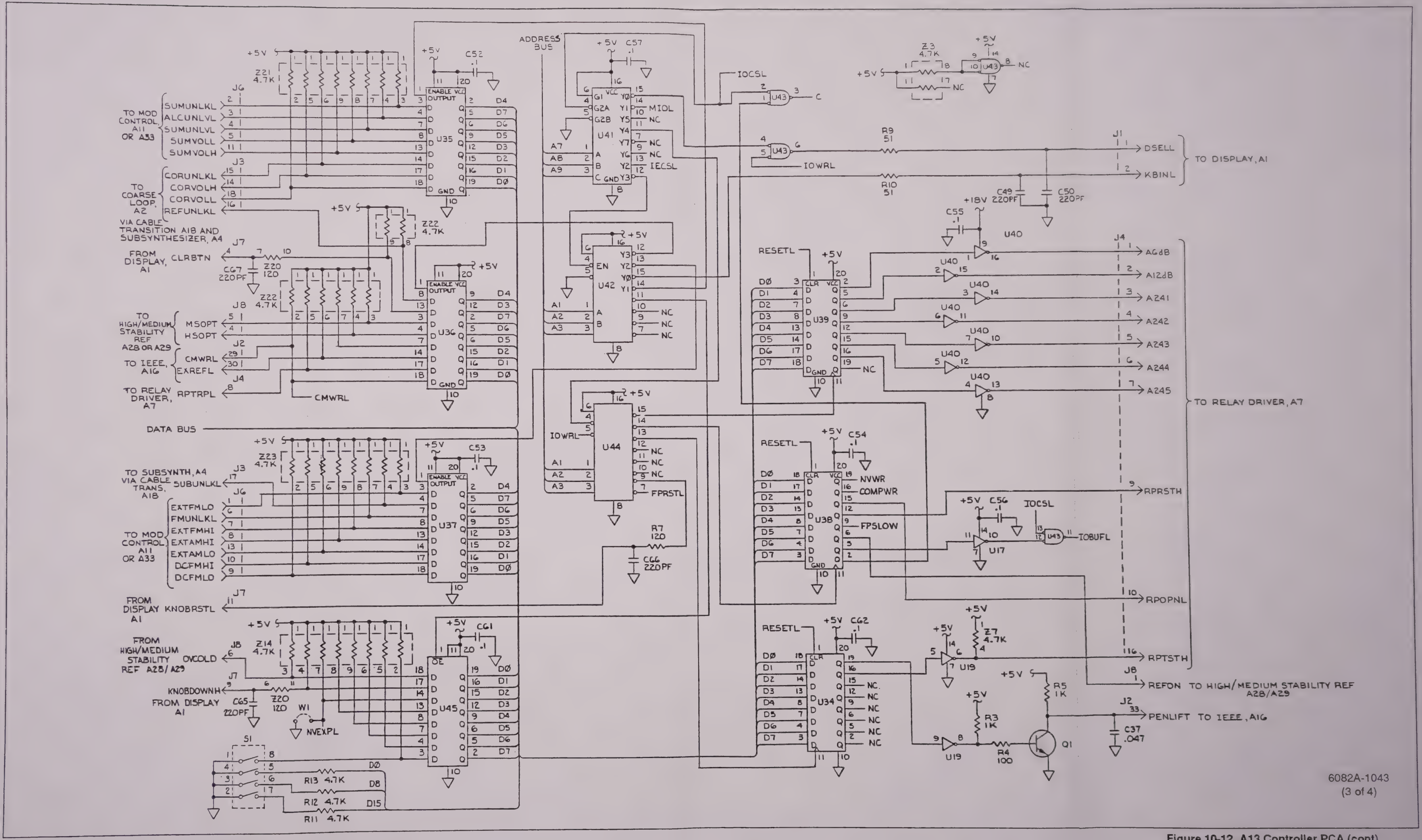

TO MOD CONTROL, A11 OR A33
SUMUNLKL
ALCUNLVL
SUMUNLVL
SUMVOLL
SUMVOLH
TO COARSE LOOP, A2
CORUNLKL
CORVOLH
CORVOLL
REFUNLKL
VIA CABLE TRANSITION A18 AND SUBSYNTHESIZER, A4
FROM DISPLAY, A1
CLRBTN
TO HIGH/MEDIUM STABILITY REF A28 OR A29
MSOPT
HSOPT
TO IEEE, A16
CMWRL
EXREFL
TO RELAY DRIVER, A7
RPTRPL
DATA BUS
TO SUBSYNTH, A4 VIA CABLE TRANS, A18
SUBUNLKL
EXTFMLO
FMUNLKL
EXTFMHI
EXTAMHI
EXTAMLO
DCFMHI
DCFMLO
FROM DISPLAY A1
KNOBRSTL
FROM HIGH/MEDIUM STABILITY REF A28/A29
OVCOLD
KNOBDOWNH
FROM DISPLAY A1
NVEXPL
W1
S1
R13 4.7K
R12 4.7K
R11 4.7K
Z21 4.7K
Z22 4.7K
Z23 4.7K
Z14 4.7K
Z20 120
C67 220PF
C65 220PF
U35
U36
U37
U45
C52
C53
C61
ADDRESS BUS
U41
U42
U44
C57
IOWRL
IOCSL
MIOL
IECSL
FPRSTL
R7 120
C66 220PF
U43
Z3 4.7K
R9 51
R10 51
C49 220PF
C50 220PF
C55
+18V
DSELL
KBINL
TO DISPLAY, A1
U39
U40
RESETL
A6dB
A12dB
A241
A242
A243
A244
A245
TO RELAY DRIVER, A7
U38
C54
NVWR
COMPWR
FPSLOW
C56
U17
IOBUFL
RPRSTH
RPOPNL
U34
C62
U19
Z7 4.7K
RPTSTH
REFON TO HIGH/MEDIUM STABILITY REF A28/A29
R5 1K
R3 1K
R4 100
Q1
C37 .047
PENLIFT TO IEEE, A16
+5V
NC
6082A-1043
(3 of 4)

Figure 10-12. A13 Controller PCA (cont)

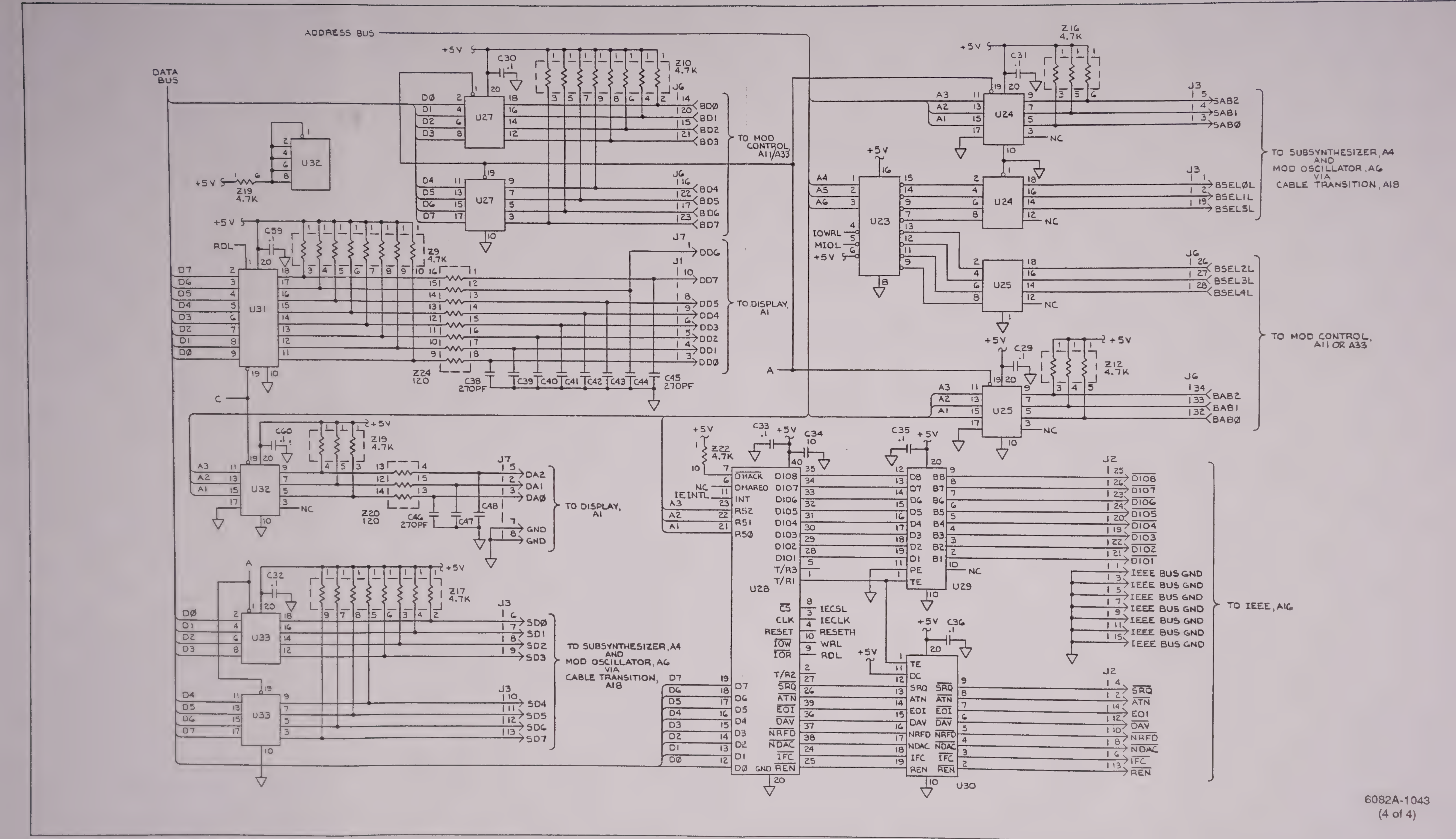

ADDRESS BUS
DATA BUS
+5V
C30 .1
Z10 4.7K
J6
U27
D0 D1 D2 D3 D4 D5 D6 D7
BD0 BD1 BD2 BD3
BD4 BD5 BD6 BD7
TO MOD CONTROL A11/A33
U32
Z19 4.7K
C59 .1
RDL
Z9 4.7K
U31
Z24 120
C38 270PF
C39 C40 C41 C42 C43 C44
C45 270PF
J7
J1
DD6 DD7 DD5 DD4 DD3 DD2 DD1 DD0
TO DISPLAY, A1
A
C
C60
Z19 4.7K
A3 A2 A1
Z20 120
C46 270PF
C47 C48
DA2 DA1 DA0
GND GND
NC
TO DISPLAY, A1
C32 .1
Z17 4.7K
U33
J3
SD0 SD1 SD2 SD3
SD4 SD5 SD6 SD7
TO SUBSYNTHESIZER, A4 AND MOD OSCILLATOR, A6 VIA CABLE TRANSITION, A18
Z16 4.7K
C31 .1
U24
SAB2 SAB1 SAB0
A4 A5 A6
IOWRL
MIOL
U23
BSEL0L BSEL1L BSEL5L
TO SUBSYNTHESIZER, A4 AND MOD OSCILLATOR, A6 VIA CABLE TRANSITION, A18
U25
BSEL2L BSEL3L BSEL4L
C29 .1
Z12 4.7K
BAB2 BAB1 BAB0
TO MOD CONTROL, A11 OR A33
Z22 4.7K
C33 .1
C34 10
C35 .1
DMACK DMAREQ INT RS2 RS1 RS0
IEINTL
DIO8 DIO7 DIO6 DIO5 DIO4 DIO3 DIO2 DIO1
T/R3 T/R1
U28
CS CLK RESET IOW IOR
IECSL IECLK RESETH WRL RDL
T/R2 SRQ ATN EOI DAV NRFD NDAC IFC REN
GND
U29
D8 D7 D6 D5 D4 D3 D2 D1 PE TE
B8 B7 B6 B5 B4 B3 B2 B1
J2
IEEE BUS GND
TO IEEE, A16
C36 .1
U30
TE DC SRQ ATN EOI DAV NRFD NDAC IFC REN
6082A-1043
(4 of 4)

Figure 10-12. A13 Controller PCA (cont)

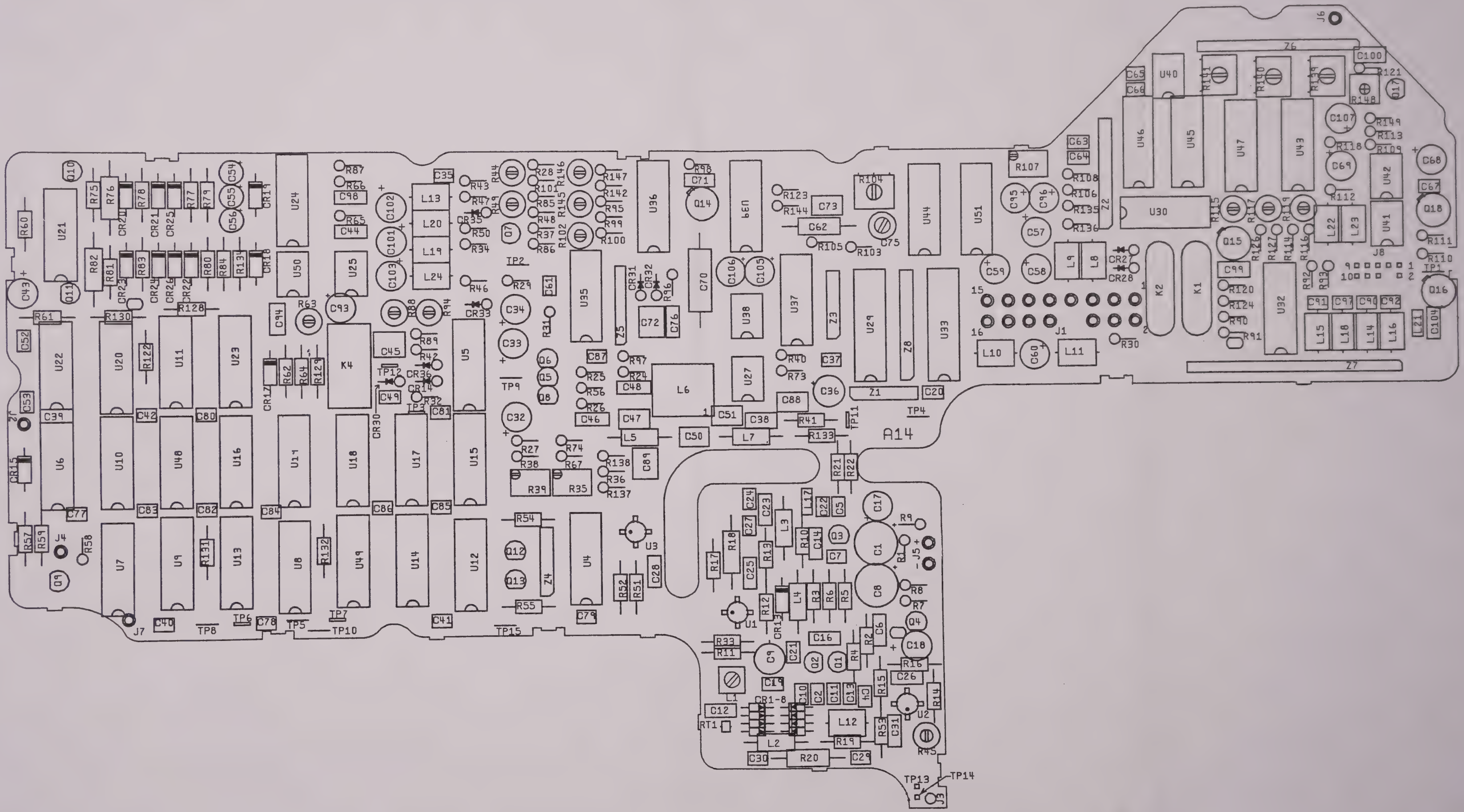
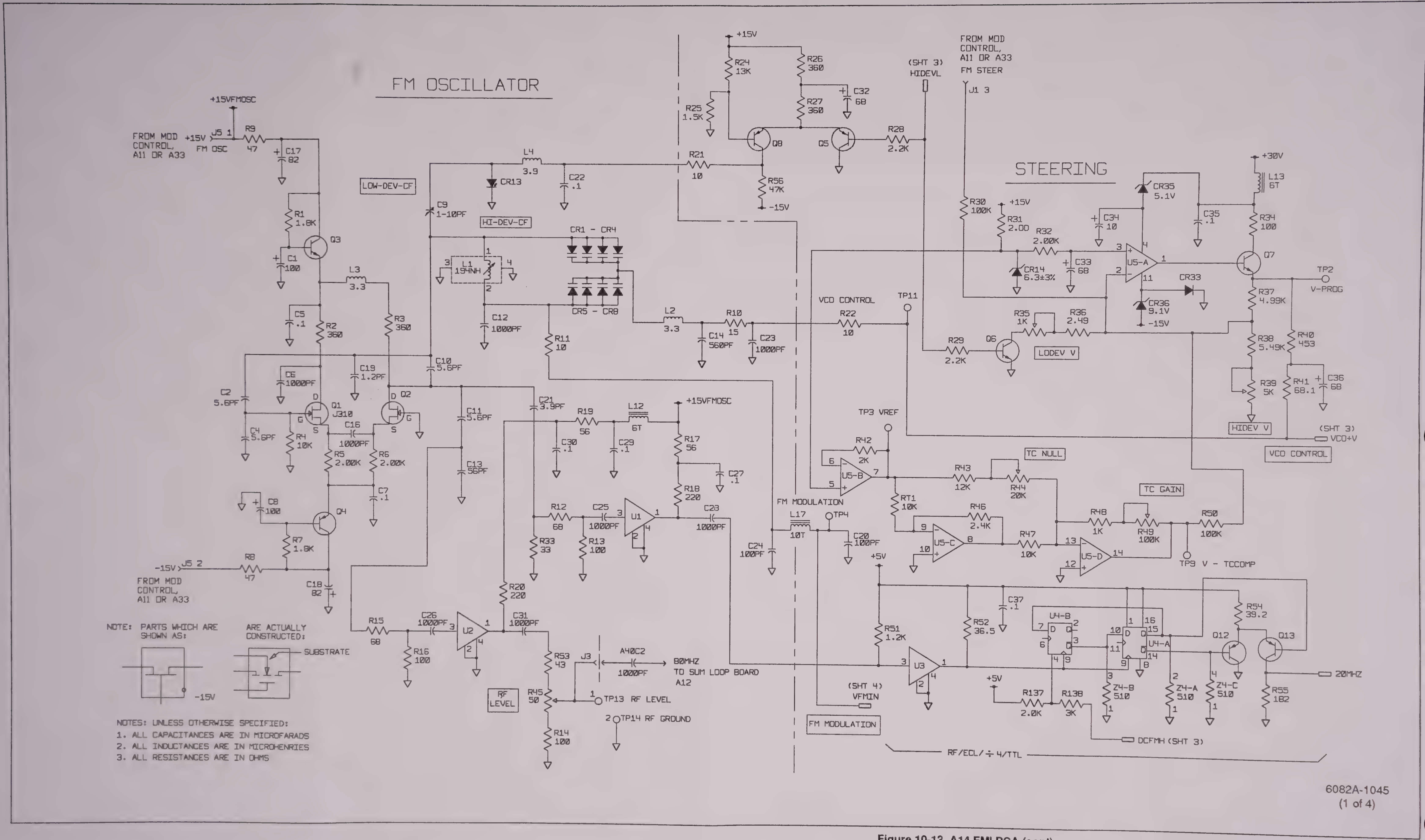

A14
J1
J3
J4
J5
J6
J7
J8
K1
K2
K4
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U20
U21
U22
U23
U24
U25
U27
U29
U30
U32
U33
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
CR1-8
CR12
CR14
CR15
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CR24
CR25
CR26
CR27
CR28
CR30
CR31
CR32
CR33
CR35
CR36
RT1
R45
R104
C100
C104
C107
6082A-1645

Figure 10-13. A14 FM PCA


FM OSCILLATOR
STEERING
+15VFMOSC
FROM MOD CONTROL, A11 OR A33
+15V J5 1 FM OSC
R9 47
C17 82
R1 1.8K
Q3
C1 100
L3 3.3
C5 .1
R2 360
R3 360
LOW-DEV-CF
HI-DEV-CF
L4 3.9
CR13
C22 .1
C9 1-10PF
L1 194NH
C12 1000PF
CR1 - CR4
CR5 - CR8
R11 10
L2 3.3
C14 560PF
R10 15
C23 1000PF
C10 5.6PF
C19 1.2PF
C6 1000PF
C2 5.6PF
Q1 J310
Q2
C16 1000PF
C4 5.6PF
R4 10K
R5 2.00K
R6 2.00K
C11 5.6PF
C13 56PF
C21 3.9PF
R19 56
L12 6T
+15VFMOSC
C30 .1
C29 .1
R17 56
C27 .1
R18 220
C7 .1
C8 100
Q4
R7 1.8K
-15V J5 2
R8 47
FROM MOD CONTROL, A11 OR A33
C18 82
R12 68
C25 1000PF
U1
R33 33
R13 100
C28 1000PF
R20 220
R15 68
C26 1000PF
U2
R16 100
C31 1000PF
R53 43
J3
A40C2 1000PF
80MHZ TO SUM LOOP BOARD A12
RF LEVEL
R45 50
TP13 RF LEVEL
TP14 RF GROUND
R14 100
NOTE: PARTS WHICH ARE SHOWN AS:
ARE ACTUALLY CONSTRUCTED:
SUBSTRATE
-15V
+15V
R24 13K
R26 360
R25 1.5K
R27 360
C32 68
Q8
Q5
R21 10
R56 47K
-15V
(SHT 3) HIDEVL
R28 2.2K
FROM MOD CONTROL, A11 OR A33
FM STEER
J1 3
R30 100K
+15V
R31 2.00
R32 2.00K
CR14 6.3±3%
C33 68
C34 10
CR35 5.1V
C35 .1
U5-A
CR33
CR36 9.1V
-15V
+30V
L13 6T
R34 100
Q7
TP2 V-PROG
R37 4.99K
R38 5.49K
R40 453
R39 5K
R41 68.1
C36 68
HIDEV V
(SHT 3) VCO+V
VCO CONTROL
VCO CONTROL
R22 10
TP11
R35 1K
R36 2.49
LODEV V
R29 2.2K
Q6
TP3 VREF
R42 2K
U5-B
TC NULL
R43 12K
R44 20K
RT1 10K
R46 2.4K
U5-C
R47 10K
TC GAIN
R48 1K
R49 100K
R50 100K
U5-D
TP9 V - TCCOMP
FM MODULATION
L17 10T
TP4
C20 100PF
C24 100PF
+5V
C37 .1
R51 1.2K
R52 36.5
U4-B
U4-A
R54 39.2
Q12
Q13
U3
(SHT 4) VFMIN
FM MODULATION
+5V
R137 2.0K
R138 3K
Z4-B 510
Z4-A 510
Z4-C 510
R55 182
20MHZ
DCFMH (SHT 3)
RF/ECL/÷4/TTL

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITANCES ARE IN MICROFARADS
2. ALL INDUCTANCES ARE IN MICROHENRIES
3. ALL RESISTANCES ARE IN OHMS

6082A-1045
(1 of 4)

Figure 10-13. A14 FMI PCA (cont)

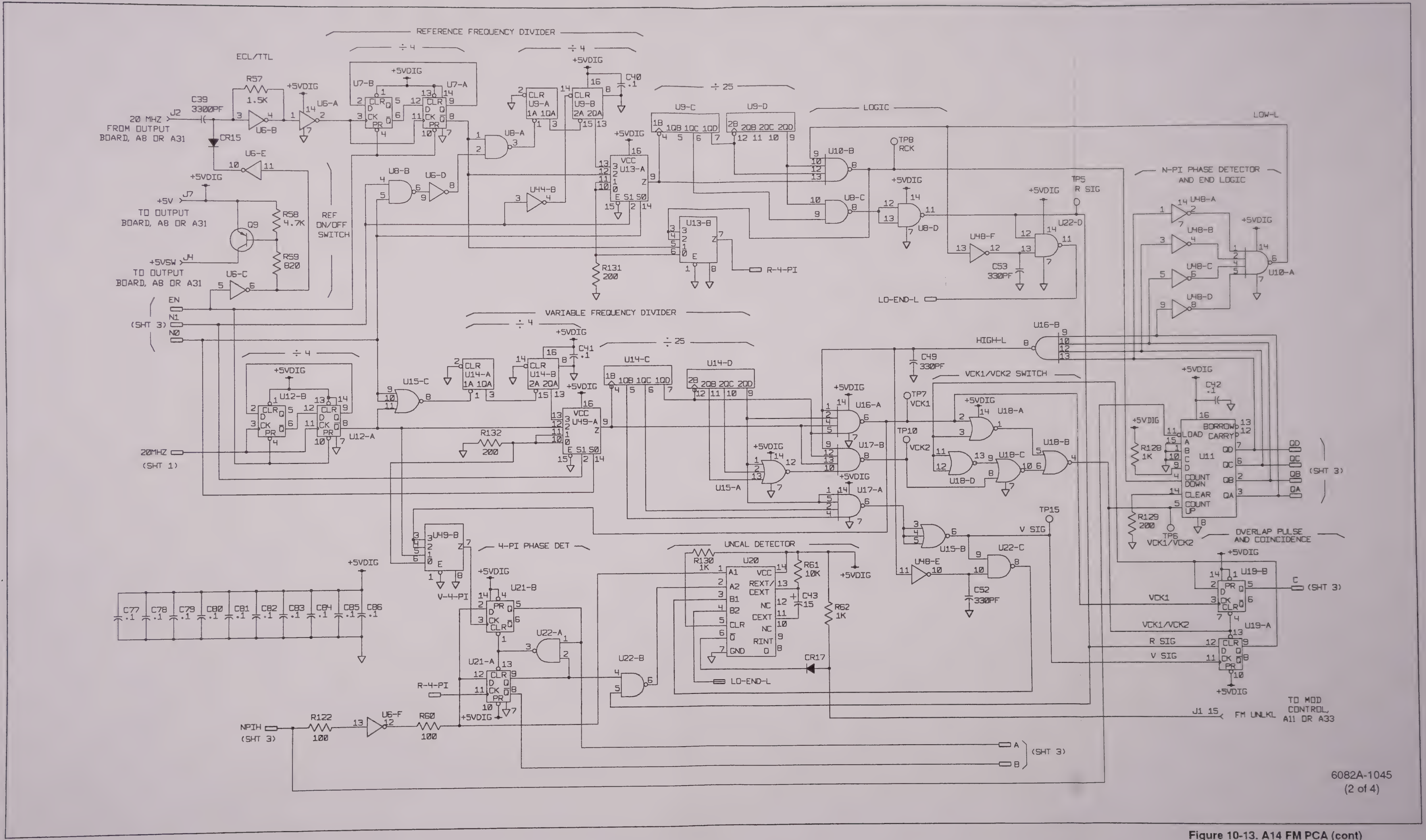

REFERENCE FREQUENCY DIVIDER
÷ 4
÷ 4
÷ 25
LOGIC
ECL/TTL
20 MHZ FROM OUTPUT BOARD, A8 OR A31
J2
C39 3300PF
R57 1.5K
CR15
U6-A
U6-B
U6-E
U7-B
U7-A
U9-A
U9-B
C40 .1
U9-C
U9-D
U8-A
U8-B
U6-D
U44-B
U13-A
U13-B
R-4-PI
U10-B
U8-C
U8-D
TP8 RCK
TP5 R SIG
U22-D
U48-F
C53 330PF
LO-END-L
LOW-L
N-PI PHASE DETECTOR AND END LOGIC
U48-A
U48-B
U48-C
U48-D
U10-A
+5V TO OUTPUT BOARD, A8 OR A31
J7
Q9
R58 4.7K
R59 820
+5VSW TO OUTPUT BOARD, A8 OR A31
J4
U6-C
REF ON/OFF SWITCH
R131 200
EN
N1
N0
(SHT 3)
+5VDIG
VARIABLE FREQUENCY DIVIDER
÷ 4
÷ 25
U14-A
U14-B
C41 .1
U14-C
U14-D
U12-B
U12-A
U15-C
U49-A
R132 200
20MHZ (SHT 1)
HIGH-L
U16-B
C49 330PF
VCK1/VCK2 SWITCH
TP7 VCK1
TP10 VCK2
U16-A
U17-B
U15-A
U17-A
U18-A
U18-B
U18-C
U18-D
C42 .1
U11
R128 1K
R129 200
TP6 VCK1/VCK2
QD
QC
QB
QA
(SHT 3)
OVERLAP PULSE AND COINCIDENCE
TP15
V SIG
U15-B
U22-C
U48-E
C52 330PF
U49-B
V-4-PI
4-PI PHASE DET
UNCAL DETECTOR
R130 1K
U20
R61 10K
C43 15
R62 1K
CR17
LO-END-L
U21-B
U22-A
U21-A
U22-B
R-4-PI
U19-B
U19-A
C (SHT 3)
VCK1
VCK1/VCK2
R SIG
V SIG
J1 15
FM UNLKL
TO MOD CONTROL, A11 OR A33
C77 .1
C78 .1
C79 .1
C80 .1
C81 .1
C82 .1
C83 .1
C84 .1
C85 .1
C86 .1
NPIH (SHT 3)
R122 100
U6-F
R60 100
A
B
(SHT 3)
6082A-1045
(2 of 4)

Figure 10-13. A14 FM PCA (cont)

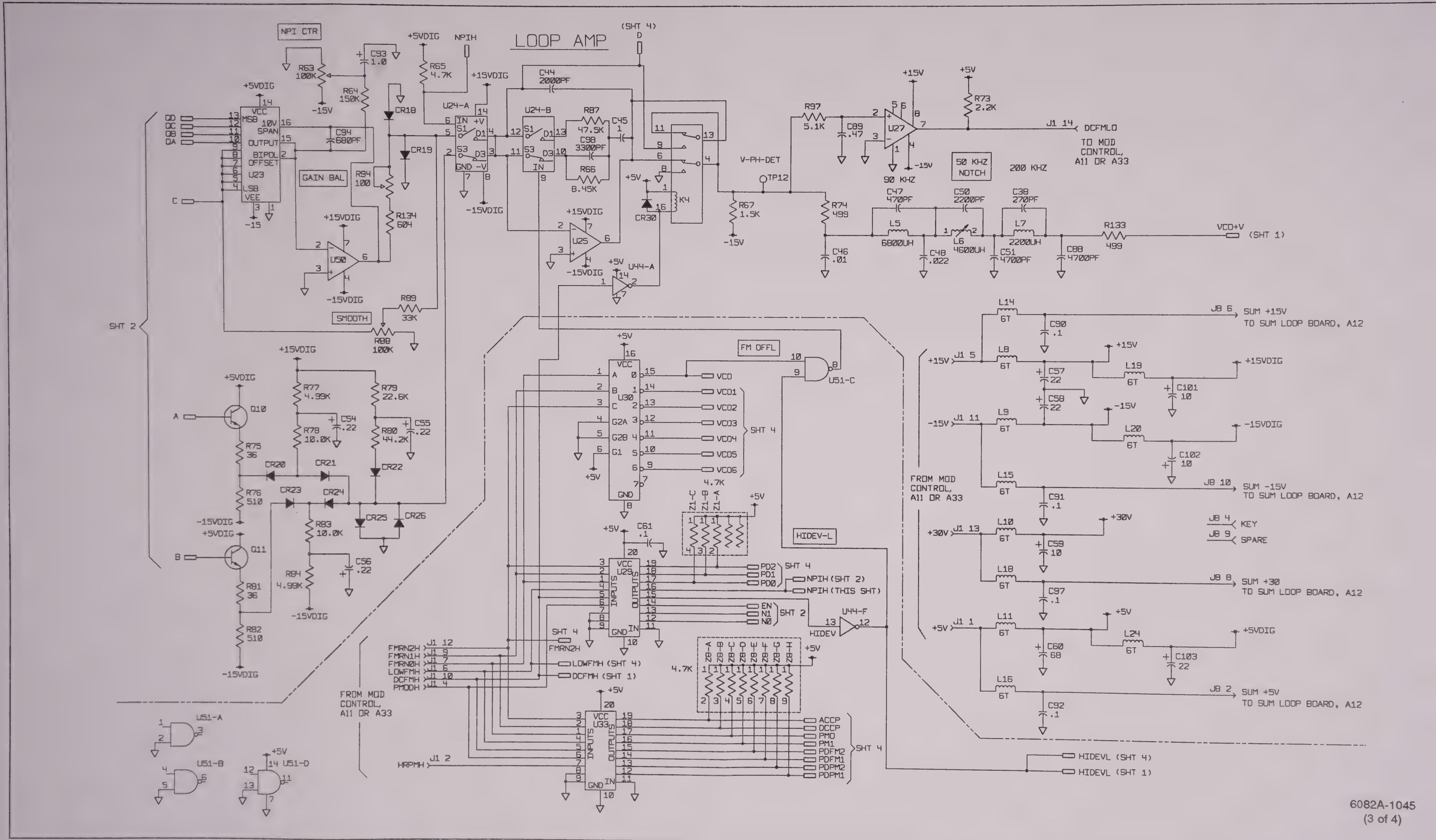

LOOP AMP
NPI CTR
GAIN BAL
SMOOTH
FM OFFL
HIDEV-L
(SHT 4)
D
+5VDIG
NPIH
+15VDIG
-15VDIG
R63 100K
C93 1.0
R64 150K
R65 4.7K
U23
VCC
MSB
10V SPAN
OUTPUT
BIPOL OFFSET
LSB
VEE
QD
QC
QB
QA
C
C94 680PF
CR18
CR19
R94 100
R134 604
U50
U24-A
U24-B
IN
S1
D1
S3
D3
GND
C44 2000PF
R87 47.5K
C45 1
C98 3300PF
R66 8.45K
K4
CR30
U25
U44-A
V-PH-DET
TP12
R67 1.5K
R97 5.1K
C89 .47
U27
R73 2.2K
J1 14
DCFMLO
TO MOD CONTROL, A11 OR A33
90 KHZ
50 KHZ NOTCH
200 KHZ
R74 499
C46 .01
C47 470PF
C50 2200PF
C38 270PF
L5 6800UH
L6 4600UH
L7 2200UH
C48 .022
C51 4700PF
C88 4700PF
R133 499
VCO+V
(SHT 1)
R89 33K
R88 100K
SHT 2
A
B
Q10
Q11
R75 36
R76 510
R77 4.99K
R78 10.0K
C54 .22
R79 22.6K
R80 44.2K
C55 .22
CR20
CR21
CR22
CR23
CR24
CR25
CR26
R83 10.0K
R84 4.99K
C56 .22
R81 36
R82 510
U30
G2A
G2B
G1
VCO
VCO1
VCO2
VCO3
VCO4
VCO5
VCO6
SHT 4
U51-C
4.7K
Z1-C
Z1-B
Z1-A
C61 .1
U29
INPUTS
OUTPUTS
PD2
PD1
PD0
NPIH (SHT 2)
NPIH (THIS SHT)
EN
N1
N0
U44-F
HIDEV
FMRN2H
FMRN1H
FMRN0H
LOWFMH
DCFMH
PMODH
J1 12
J1 9
J1 7
J1 6
J1 10
J1 4
LOWFMH (SHT 4)
DCFMH (SHT 1)
FROM MOD CONTROL, A11 OR A33
HRPMH
J1 2
U33
Z8-A
Z8-B
Z8-C
Z8-D
Z8-E
Z8-F
Z8-G
Z8-H
ACCP
DCCP
PM0
PM1
PDFM2
PDFM1
PDPM2
PDPM1
HIDEVL (SHT 4)
HIDEVL (SHT 1)
U51-A
U51-B
U51-D
+15V
J1 5
-15V
J1 11
+30V
J1 13
+5V
J1 1
L14 6T
L8 6T
L9 6T
L15 6T
L10 6T
L18 6T
L11 6T
L16 6T
L19 6T
L20 6T
L24 6T
C90 .1
C57 22
C58 22
C101 10
C102 10
C91 .1
C59 10
C97 .1
C60 68
C103 22
C92 .1
J8 6
SUM +15V TO SUM LOOP BOARD, A12
J8 10
SUM -15V TO SUM LOOP BOARD, A12
J8 4
KEY
J8 9
SPARE
J8 8
SUM +30 TO SUM LOOP BOARD, A12
J8 2
SUM +5V TO SUM LOOP BOARD, A12
+30V
6082A-1045
(3 of 4)

Figure 10-13. A14 FM PCA (cont)

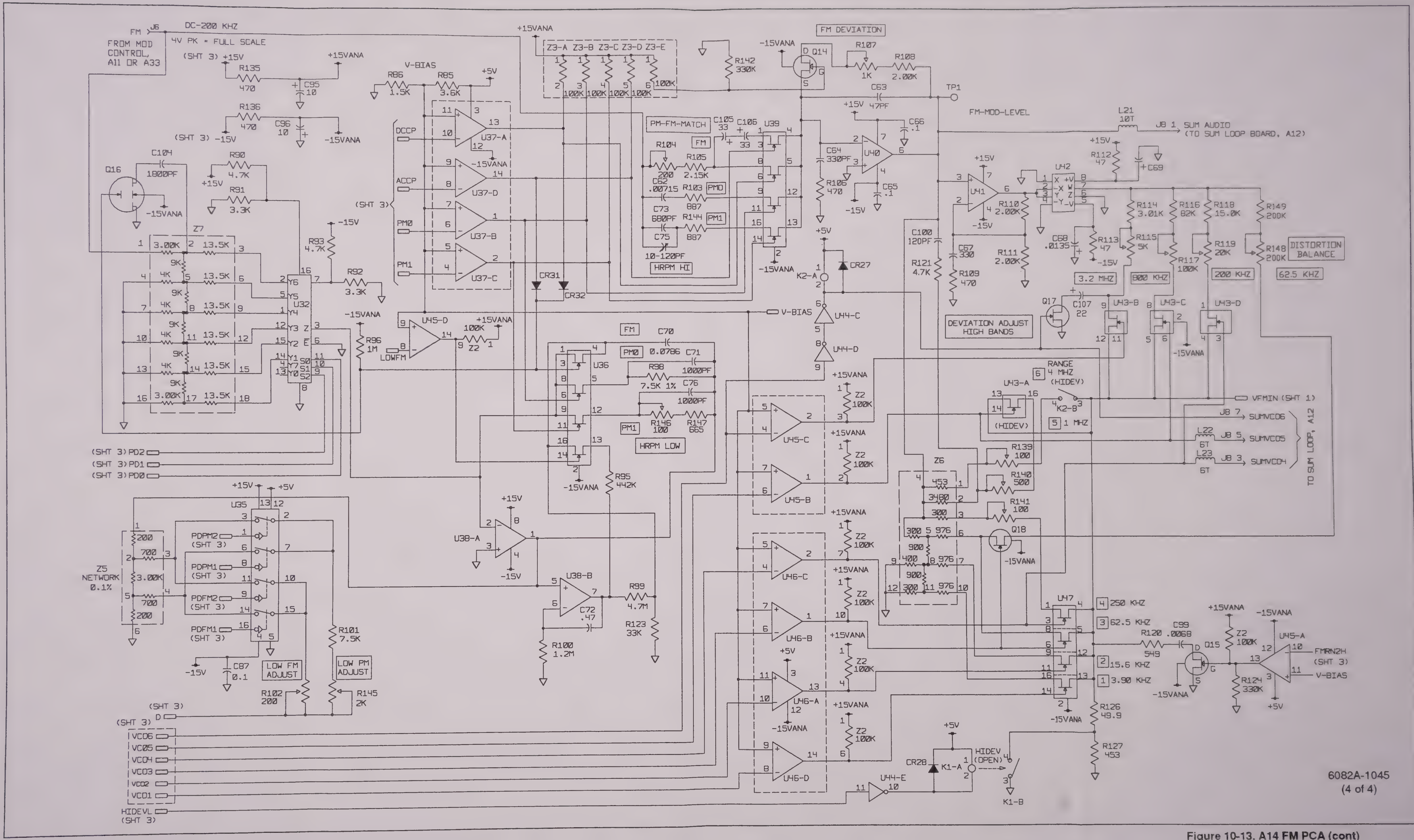
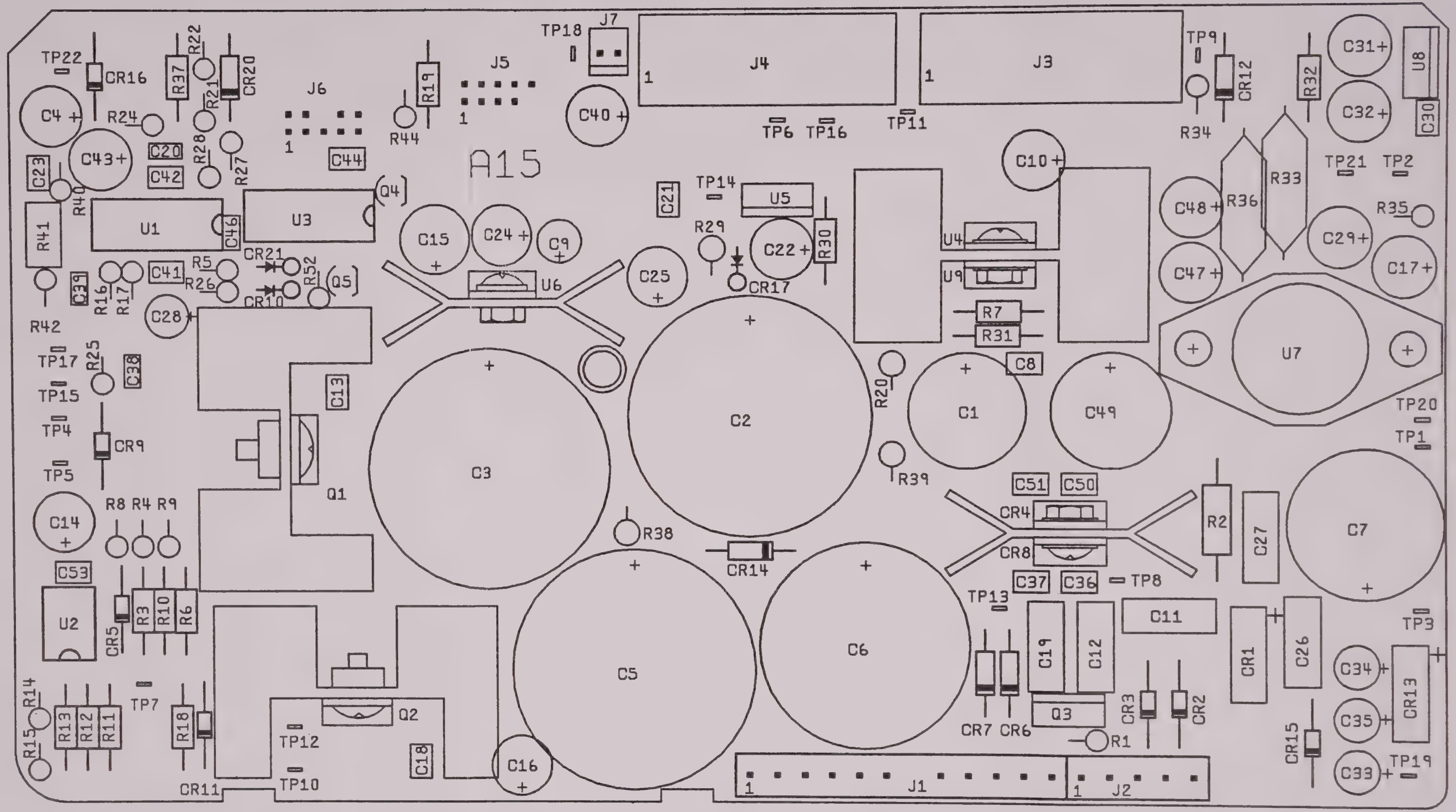
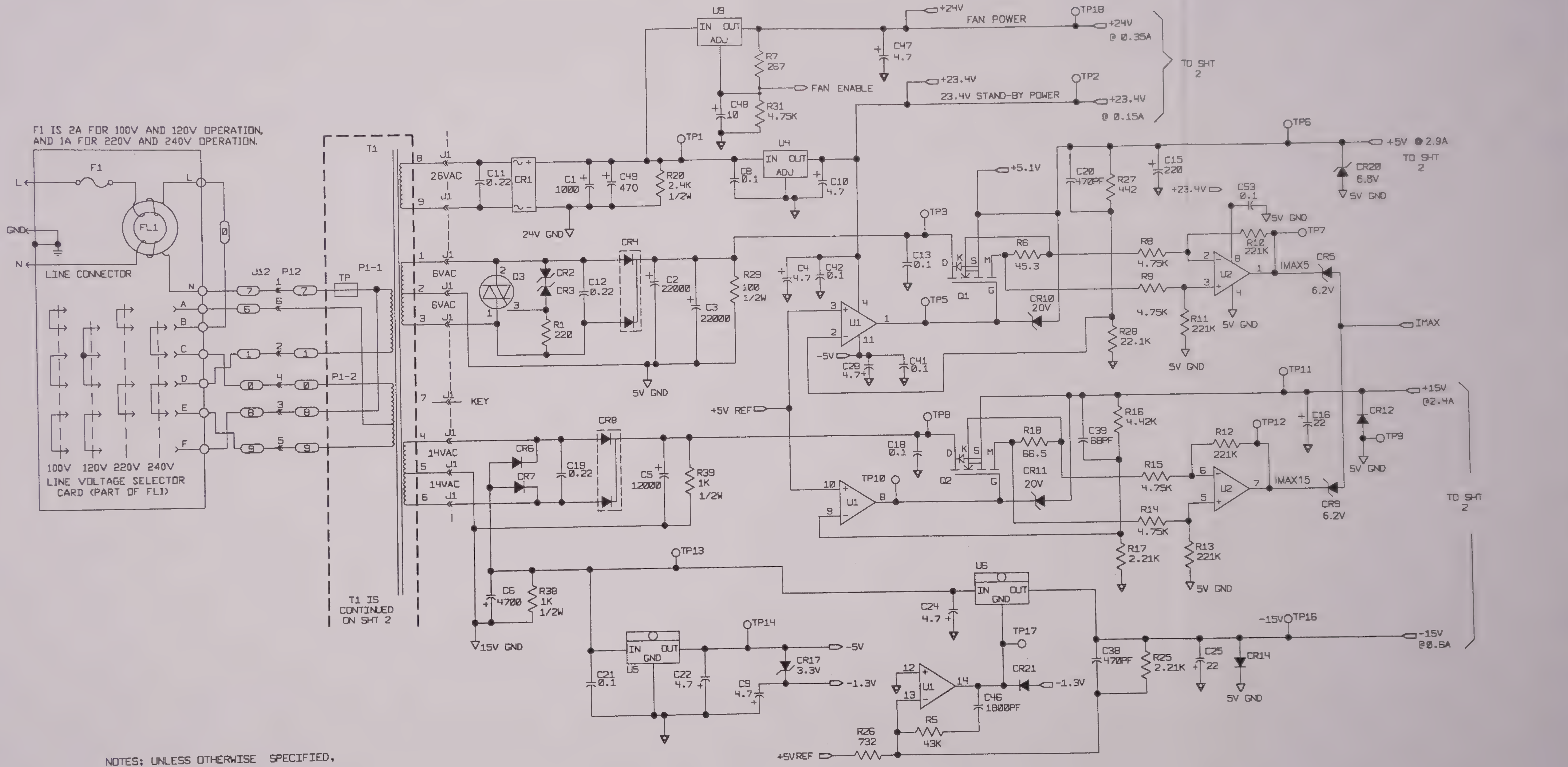

FM J6 DC-200 KHZ
4V PK = FULL SCALE
FROM MOD CONTROL, A11 OR A33
(SHT 3) +15V
R135 470
+15VANA
C95 10
R136 470
C96 10
(SHT 3) -15V
-15VANA
V-BIAS
R86 1.5K
R85 3.6K
+5V
DCCP
ACCP
PM0
PM1
(SHT 3)
U37-A
U37-D
U37-B
U37-C
Z3-A Z3-B Z3-C Z3-D Z3-E
100K
R142 330K
FM DEVIATION
-15VANA
Q14
R107 1K
R108 2.00K
C63 47PF
TP1
FM-MOD-LEVEL
L21 10T
J8 1, SUM AUDIO (TO SUM LOOP BOARD, A12)
PM-FM-MATCH
FM
PM0
PM1
R104 200
R105 2.15K
C62 .00715
R103 887
C73 680PF
R144 887
C75 10-120PF
HRPM HI
C105 33
C106 33
U39
C64 330PF
U40
R106 470
C65 .1
C66 .1
+15V
R112 47
C69
U42
U41
R110 2.00K
R111 2.00K
C68 .0135
R113 47
R114 3.01K
R115 5K
R116 82K
R117 100K
R118 15.0K
R119 20K
R149 200K
R148 200K
DISTORTION BALANCE
3.2 MHZ
800 KHZ
200 KHZ
62.5 KHZ
C100 120PF
C67 330
R109 470
R121 4.7K
DEVIATION ADJUST HIGH BANDS
Q17
C107 22
U43-B
U43-C
U43-D
C104 1800PF
Q16
R90 4.7K
R91 3.3K
Z7
3.00K
13.5K
9K
4K
U32
R93 4.7K
R92 3.3K
CR27
K2-A
U44-C
U44-D
CR31
CR32
U45-D
R96 1M
LOWFM
100K
Z2
U36
C70 0.0786
C71 1000PF
R98 7.5K 1%
C76 1000PF
R146 100
R147 665
HRPM LOW
R95 442K
RANGE
6 4 MHZ (HIDEV)
U43-A
K2-B
5 1 MHZ
VFMIN (SHT 1)
J8 7, SUMVCO6
L22 6T
J8 5, SUMVCO5
L23 6T
J8 3, SUMVCO4
TO SUM LOOP, A12
(SHT 3) PD2
(SHT 3) PD1
(SHT 3) PD0
U35
Z5 NETWORK 0.1%
200
700
3.00K
PDPM2 (SHT 3)
PDPM1 (SHT 3)
PDFM2 (SHT 3)
PDFM1 (SHT 3)
U38-A
U38-B
C72 .47
R99 4.7M
R123 33K
R100 1.2M
R101 7.5K
LOW FM ADJUST
LOW PM ADJUST
R102 200
R145 2K
C87 0.1
U45-C
U45-B
U46-C
U46-B
U46-A
U46-D
Z6
453
3480
300
976
900
400
R139 100
R140 500
R141 100
Q18
U47
4 250 KHZ
3 62.5 KHZ
2 15.6 KHZ
1 3.90 KHZ
R120 549
C99 .0068
Q15
R124 330K
U45-A
FMRN2H (SHT 3)
V-BIAS
R126 49.9
R127 453
CR28
K1-A
HIDEV (OPEN)
K1-B
U44-E
(SHT 3) D
VCO6
VCO5
VCO4
VCO3
VCO2
VCO1
HIDEVL (SHT 3)
6082A-1045 (4 of 4)

Figure 10-13. A14 FM PCA (cont)


A15
TP22
CR16
R37
R22
R21
CR20
R28
R27
J6
1
R19
R44
J5
1
TP18
J7
J4
1
J3
1
TP9
CR12
R34
R32
C31+
C32+
U8
C30
C4 +
R24
C43+
C20
C42
C23
R40
R41
U1
C46
U3
C44
Q4
C40 +
TP6
TP16
TP11
C10 +
TP21
TP2
R35
R36
R33
C48 +
C47 +
C29+
C17+
CR21
R5
R26
R52
Q5
CR10
C41
R16
R17
C39
R42
C28
C15
+
C24 +
C9
+
U6
C21
TP14
U5
R29
C22 +
R30
CR17
C25
+
U4
U9
R7
R31
C8
U7
+
+
TP17
R25
C38
TP15
TP4
CR9
TP5
C13
Q1
C3
+
C2
+
R20
C1
+
C49
+
TP20
TP1
R39
C51
C50
CR4
CR8
R2
C27
C7
+
C14
+
R8 R4 R9
R38
CR14
C5
+
C6
+
C37
C36
TP8
TP13
C53
U2
CR5
R3
R10
R6
C19
C12
C11
CR1
C26
TP3
C34
C35
CR13
C33
TP19
CR15
R14
R15
R13
R12
R11
TP7
R18
CR11
TP12
TP10
Q2
C18
C16
+
Q3
CR3
CR2
CR7 CR6
R1
1
J1
1
J2

6082A-1670

Figure 10-14. A15 Power Supply PCA


F1 IS 2A FOR 100V AND 120V OPERATION,
AND 1A FOR 220V AND 240V OPERATION.
F1
FL1
L
GND
N
LINE CONNECTOR
100V 120V 220V 240V
LINE VOLTAGE SELECTOR
CARD (PART OF FL1)
J12 P12
TP
P1-1
P1-2
T1
T1 IS
CONTINUED
ON SHT 2
26VAC
6VAC
14VAC
KEY
J1
CR1
C11 0.22
C1 1000
C49 470
R20 2.4K 1/2W
24V GND
U3
IN OUT ADJ
R7 267
R31 4.75K
C48 10
FAN ENABLE
C47 4.7
+24V
FAN POWER
TP18
+24V @ 0.35A
+23.4V
23.4V STAND-BY POWER
TP2
+23.4V @ 0.15A
TO SHT 2
TP1
U4
C8 0.1
C10 4.7
Q3
CR2
CR3
R1 220
C12 0.22
CR4
C2 22000
C3 22000
R29 100 1/2W
5V GND
+5.1V
TP3
C13 0.1
C4 4.7
C42 0.1
Q1
R6 45.3
TP5
U1
-5V
C28 4.7
C41 0.1
CR10 20V
C20 470PF
R27 442
C15 220
+23.4V
C53 0.1
TP6
+5V @ 2.9A
CR20 6.8V
R8 4.75K
R9 4.75K
R10 221K
TP7
U2
IMAX5
CR5 6.2V
R11 221K
R28 22.1K
IMAX
TP11
+15V @2.4A
+5V REF
TP8
C18 0.1
Q2
R18 66.5
CR11 20V
TP10
C39 68PF
R16 4.42K
C16 22
CR12
TP9
TP12
R12 221K
R15 4.75K
IMAX15
CR9 6.2V
R14 4.75K
R13 221K
R17 2.21K
CR6
CR7
C19 0.22
CR8
C5 12000
R39 1K 1/2W
C6 4700
R38 1K 1/2W
15V GND
TP13
U5
IN OUT GND
C21 0.1
C22 4.7
TP14
CR17 3.3V
C9 4.7
-5V
-1.3V
C24 4.7
TP17
CR21
-1.3V
C46 1800PF
R5 43K
R26 732
+5VREF
C38 470PF
R25 2.21K
C25 22
CR14
-15V TP16
-15V @0.6A
6082A-1070
(1 of 2)

NOTES; UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTANCES ARE IN OHMS.
3. ALL INDUCTANCES ARE IN MICROHENRIES.

Figure 10-14. A15 Power Supplyl PCA (cont)

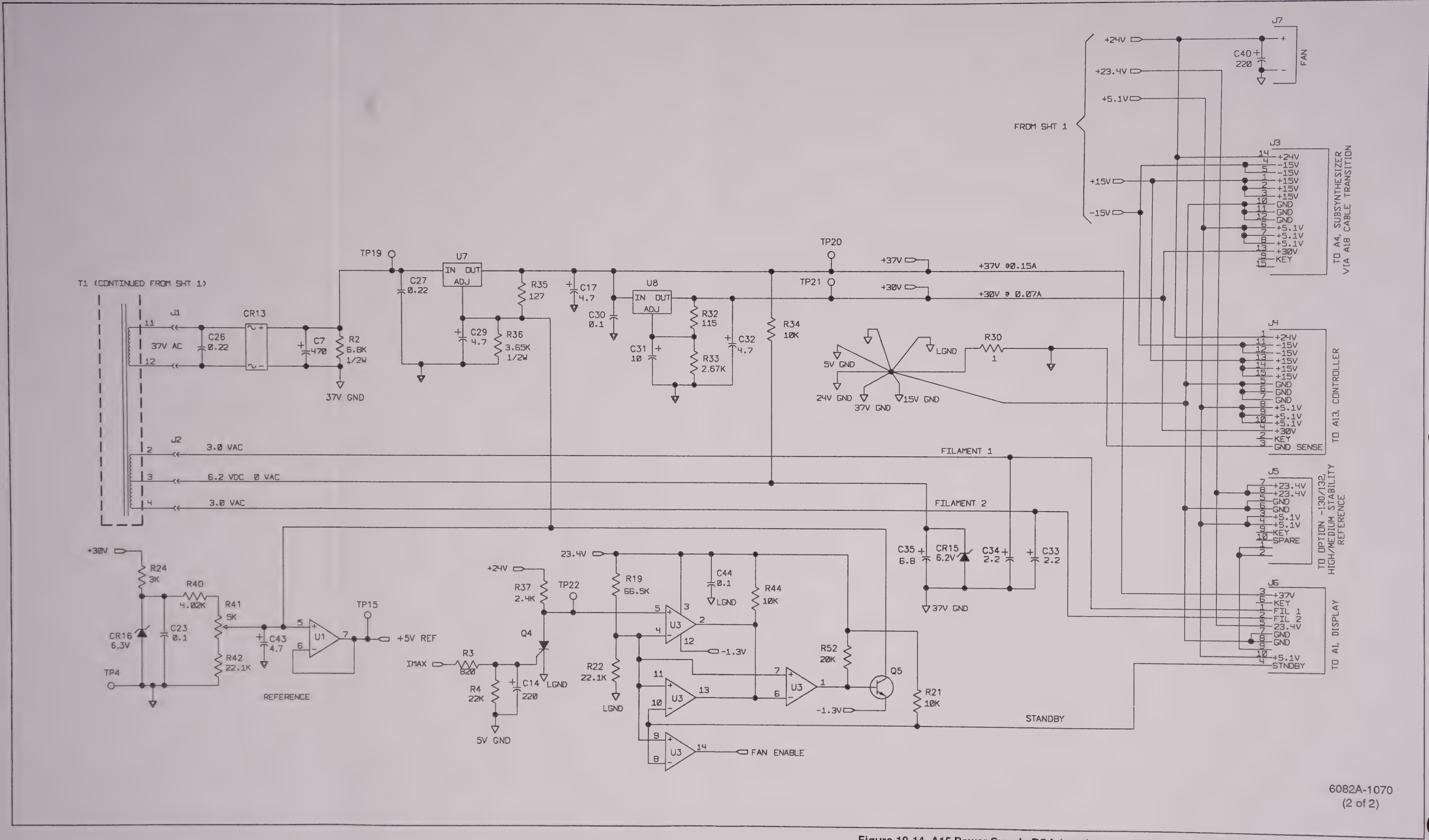

+24V
+23.4V
+5.1V
FROM SHT 1
+15V
-15V
J7
C40
220
FAN
J3
14 +24V
4 -15V
5 -15V
1 +15V
2 +15V
3 +15V
10 GND
11 GND
12 GND
6 +5.1V
7 +5.1V
8 +5.1V
13 +30V
9 KEY
15
TO A4, SUBSYNTHESIZER VIA A18 CABLE TRANSITION
TP19
U7
IN OUT
ADJ
C27
0.22
R35
127
C17
4.7
C29
4.7
R36
3.65K
1/2W
C30
0.1
U8
IN OUT
ADJ
R32
115
C31
10
R33
2.67K
C32
4.7
R34
10K
TP20
TP21
+37V
+30V
+37V @0.15A
+30V @ 0.07A
T1 (CONTINUED FROM SHT 1)
J1
11
37V AC
12
C26
0.22
CR13
C7
470
R2
6.8K
1/2W
37V GND
5V GND
LGND
24V GND
37V GND
15V GND
R30
1
J4
1 +24V
11 -15V
12 -15V
13 +15V
14 +15V
15 +15V
5 GND
6 GND
7 GND
8 +5.1V
9 +5.1V
10 +5.1V
4 +30V
2 KEY
3 GND SENSE
TO A13, CONTROLLER
J2
2 3.0 VAC
3 6.2 VDC 0 VAC
4 3.0 VAC
FILAMENT 1
FILAMENT 2
J5
7 +23.4V
8 +23.4V
5 GND
6 GND
3 +5.1V
4 +5.1V
9 KEY
10 SPARE
1
2
TO OPTION -130/132, HIGH/MEDIUM STABILITY REFERENCE
C35
6.8
CR15
6.2V
C34
2.2
C33
2.2
37V GND
J6
3 +37V
6 KEY
1 FIL 1
2 FIL 2
5 23.4V
7 GND
8 GND
9
10 +5.1V
4 STNDBY
TO A1, DISPLAY
+30V
R24
3K
R40
4.02K
R41
5K
CR16
6.3V
C23
0.1
R42
22.1K
TP4
C43
4.7
U1
5
6
7
TP15
+5V REF
REFERENCE
+24V
R37
2.4K
TP22
Q4
IMAX
R3
820
R4
22K
C14
220
LGND
5V GND
23.4V
R19
66.5K
R22
22.1K
LGND
C44
0.1
LGND
R44
10K
U3
5
4
3
2
12
-1.3V
11
10
13
7
6
1
9
8
14
FAN ENABLE
R52
20K
Q5
-1.3V
R21
10K
STANDBY
6082A-1070
(2 of 2)

Figure 10-14. A15 Power Supply PCA (cont)

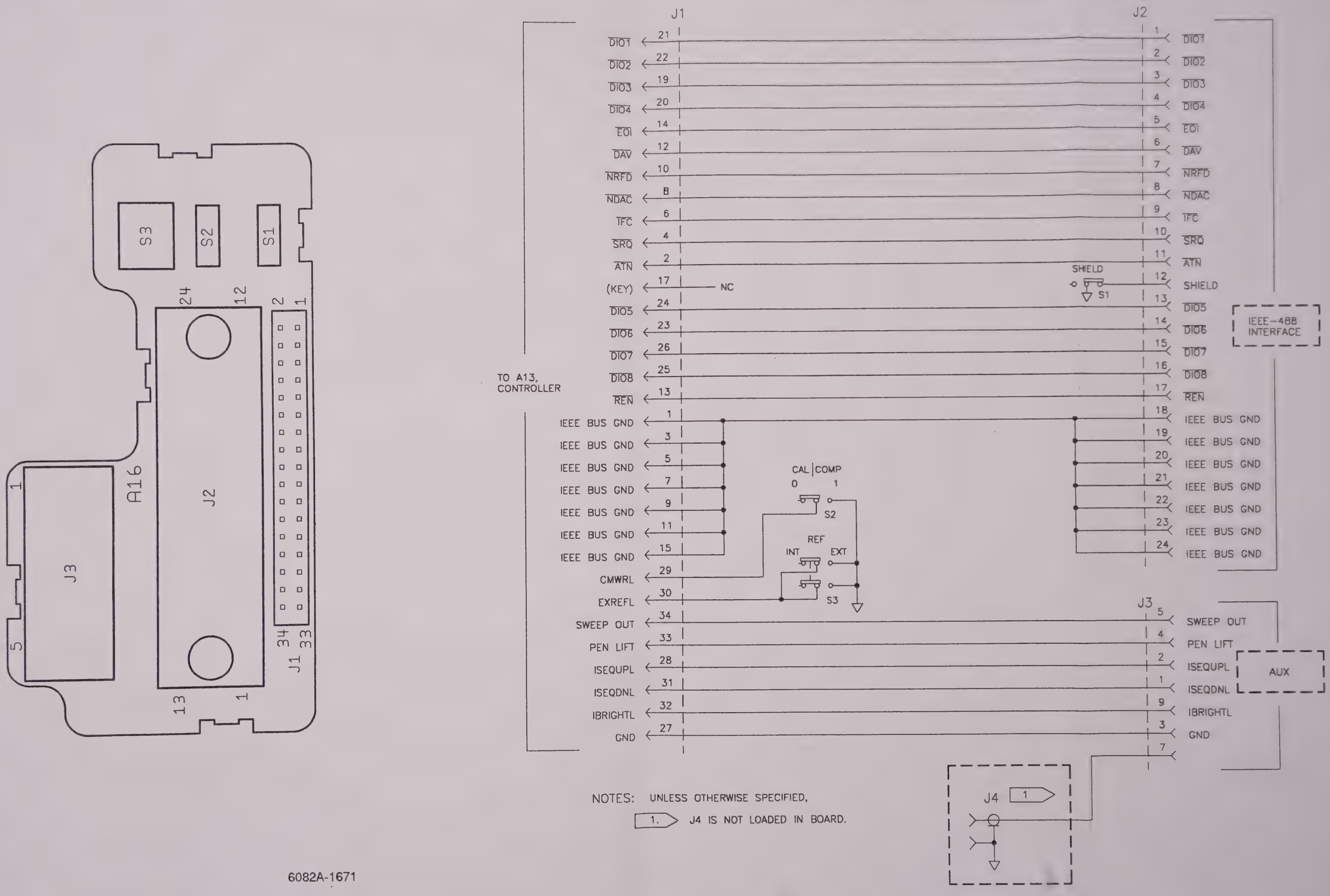
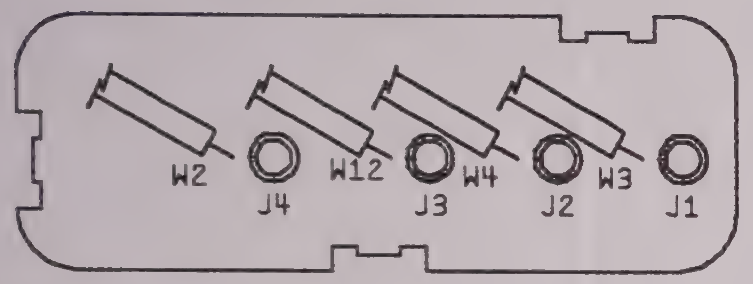
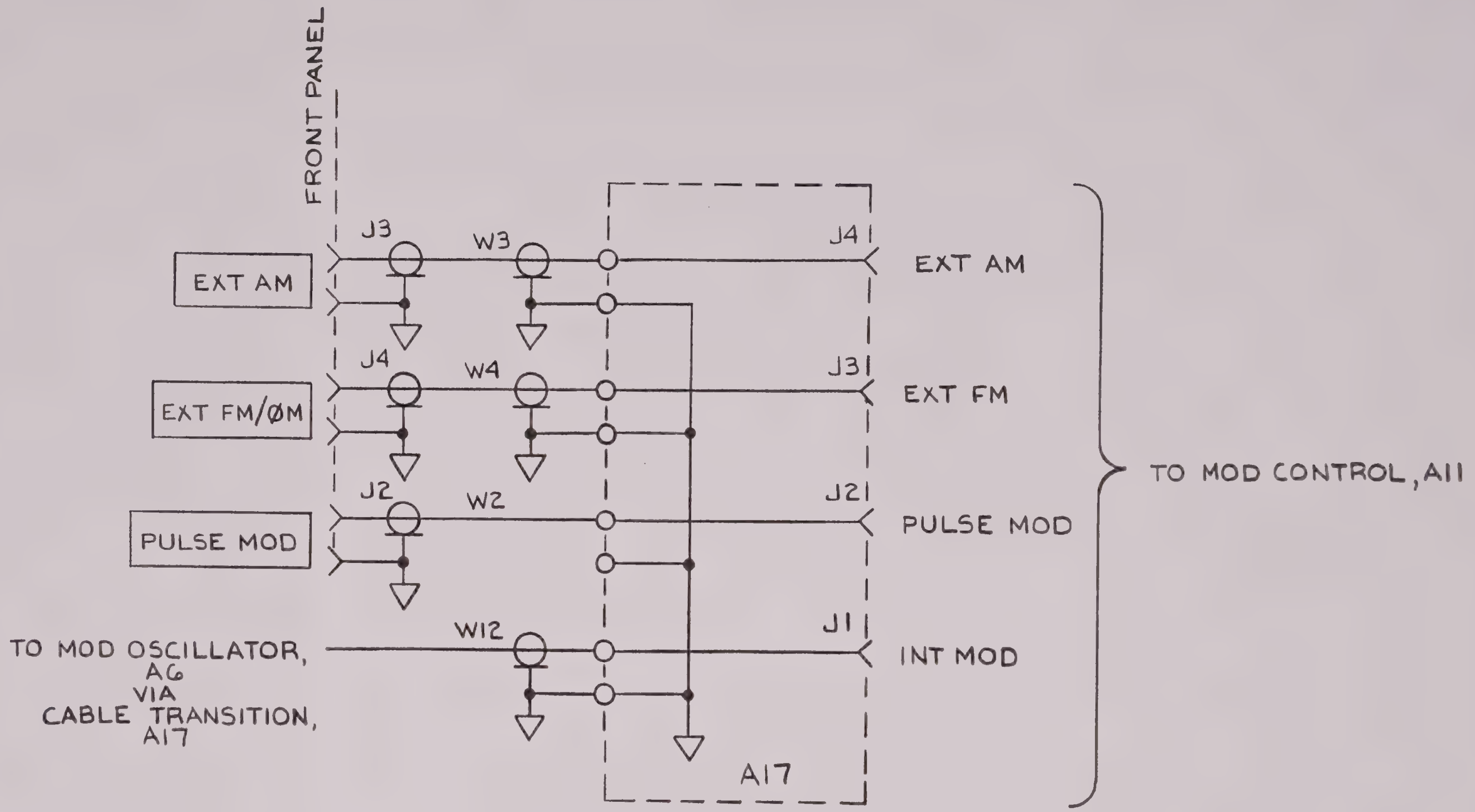

S3
S2
S1
24
12
2
1
A16
J2
J3
1
5
34
33
J1
13
1
6082A-1671
J1
J2
DIO1
DIO2
DIO3
DIO4
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
(KEY)
NC
DIO5
DIO6
DIO7
DIO8
REN
TO A13, CONTROLLER
IEEE BUS GND
CMWRL
EXREFL
SWEEP OUT
PEN LIFT
ISEQUPL
ISEQDNL
IBRIGHTL
GND
SHIELD
S1
CAL | COMP
0 1
S2
REF
INT EXT
S3
IEEE-488 INTERFACE
J3
AUX
J4
NOTES: UNLESS OTHERWISE SPECIFIED,
1. J4 IS NOT LOADED IN BOARD.
6082A-1071

Figure 10-15. A16 IEEE Connector PCA

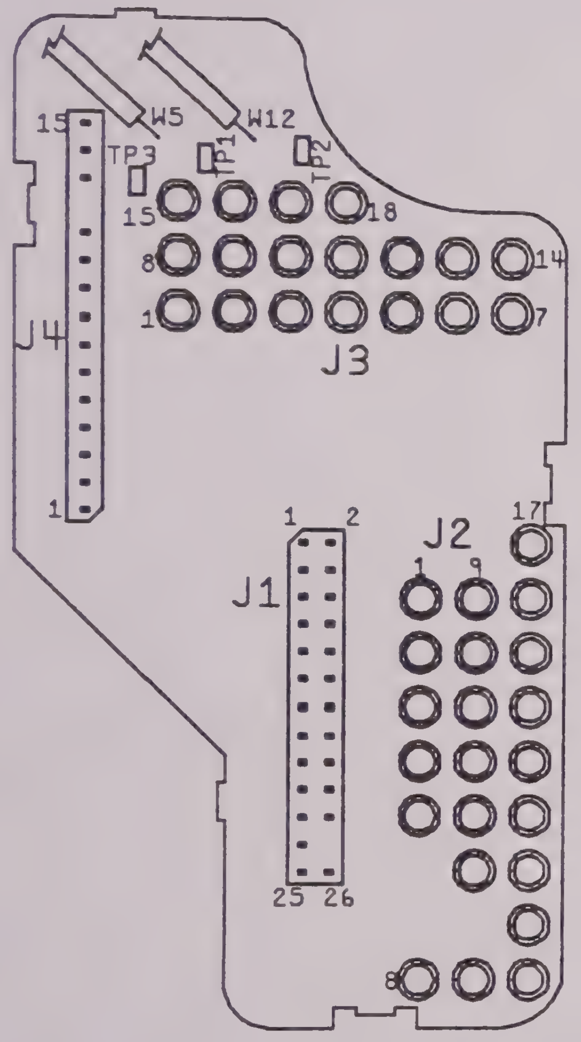

W2
J4
W12
J3
W4
J2
W3
J1

6082A-1610

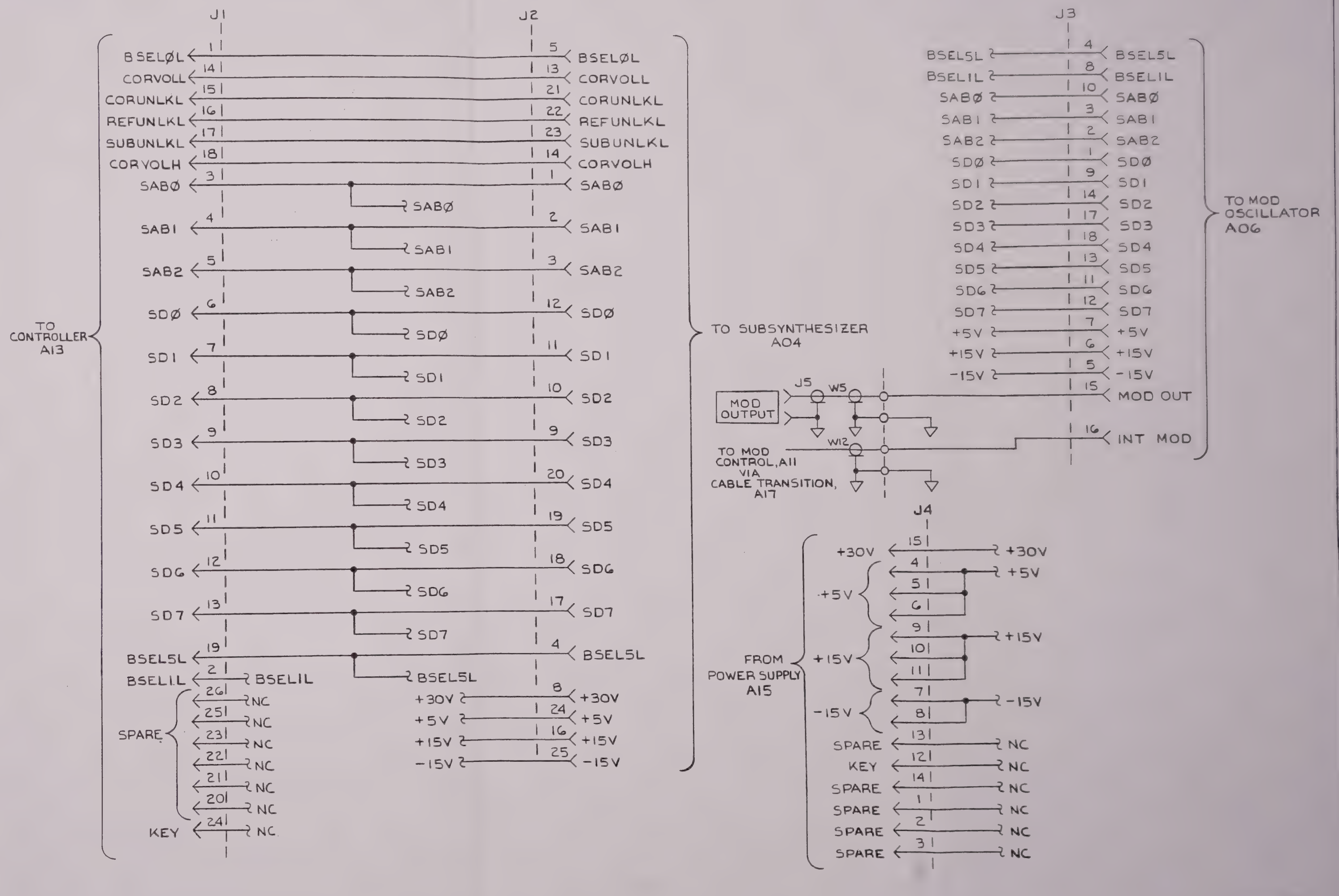

FRONT PANEL
EXT AM
EXT FM/ØM
PULSE MOD
TO MOD OSCILLATOR, A6 VIA CABLE TRANSITION, A17
J3
J4
J2
W3
W4
W2
W12
J4
J3
J2
J1
A17
EXT AM
EXT FM
PULSE MOD
INT MOD
TO MOD CONTROL, A11

6080A-1044

Figure 10-16. A17 Cable Transition PCA

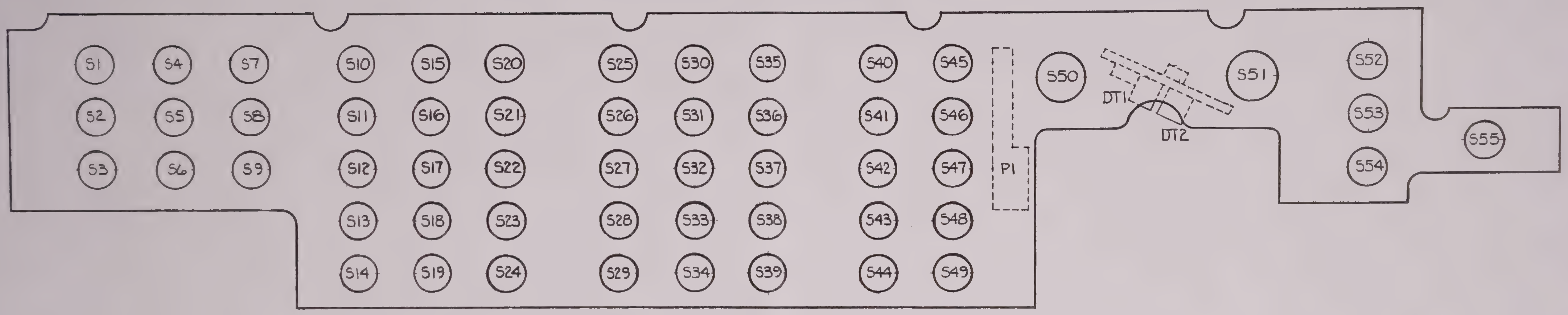

W5
W12
TP3
TP1
TP2
15
1
J4
15
18
8
14
1
7
J3
J1
1
2
25
26
J2
1
9
17
8

6080A-1610


J1
J2
J3
J4
TO CONTROLLER A13
TO SUBSYNTHESIZER A04
TO MOD OSCILLATOR A06
FROM POWER SUPPLY A15
BSELØL 1 5 BSELØL
CORVOLL 14 13 CORVOLL
CORUNLKL 15 21 CORUNLKL
REFUNLKL 16 22 REFUNLKL
SUBUNLKL 17 23 SUBUNLKL
CORVOLH 18 14 CORVOLH
SABØ 3 1 SABØ
SABØ
SAB1 4 2 SAB1
SAB1
SAB2 5 3 SAB2
SAB2
SDØ 6 12 SDØ
SDØ
SD1 7 11 SD1
SD1
SD2 8 10 SD2
SD2
SD3 9 9 SD3
SD3
SD4 10 20 SD4
SD4
SD5 11 19 SD5
SD5
SD6 12 18 SD6
SD6
SD7 13 17 SD7
SD7
BSEL5L 19 4 BSEL5L
BSEL5L
BSEL1L 2 BSEL1L
SPARE 26 25 23 22 21 20 NC
KEY 24 NC
+30V 8 +30V
+5V 24 +5V
+15V 16 +15V
−15V 25 −15V
BSEL5L 4 BSEL5L
BSEL1L 8 BSEL1L
SABØ 10 SABØ
SAB1 3 SAB1
SAB2 2 SAB2
SDØ 1 SDØ
SD1 9 SD1
SD2 14 SD2
SD3 17 SD3
SD4 18 SD4
SD5 13 SD5
SD6 11 SD6
SD7 12 SD7
+5V 7 +5V
+15V 6 +15V
−15V 5 −15V
15 MOD OUT
16 INT MOD
MOD OUTPUT
J5
W5
W12
TO MOD CONTROL, A11 VIA CABLE TRANSITION, A17
+30V 15 +30V
+5V 4 5 6 +5V
+15V 9 10 11 +15V
−15V 7 8 −15V
SPARE 13 NC
KEY 12 NC
SPARE 14 NC
SPARE 1 NC
SPARE 2 NC
SPARE 3 NC

6080A-1065

Figure 10-17. A18 Cable Transition PCA


S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
S36
S37
S38
S39
S40
S41
S42
S43
S44
S45
S46
S47
S48
S49
P1
S50
DT1
DT2
S51
S52
S53
S54
S55

6080A-1651

Figure 10-18. A19 Switch PCA

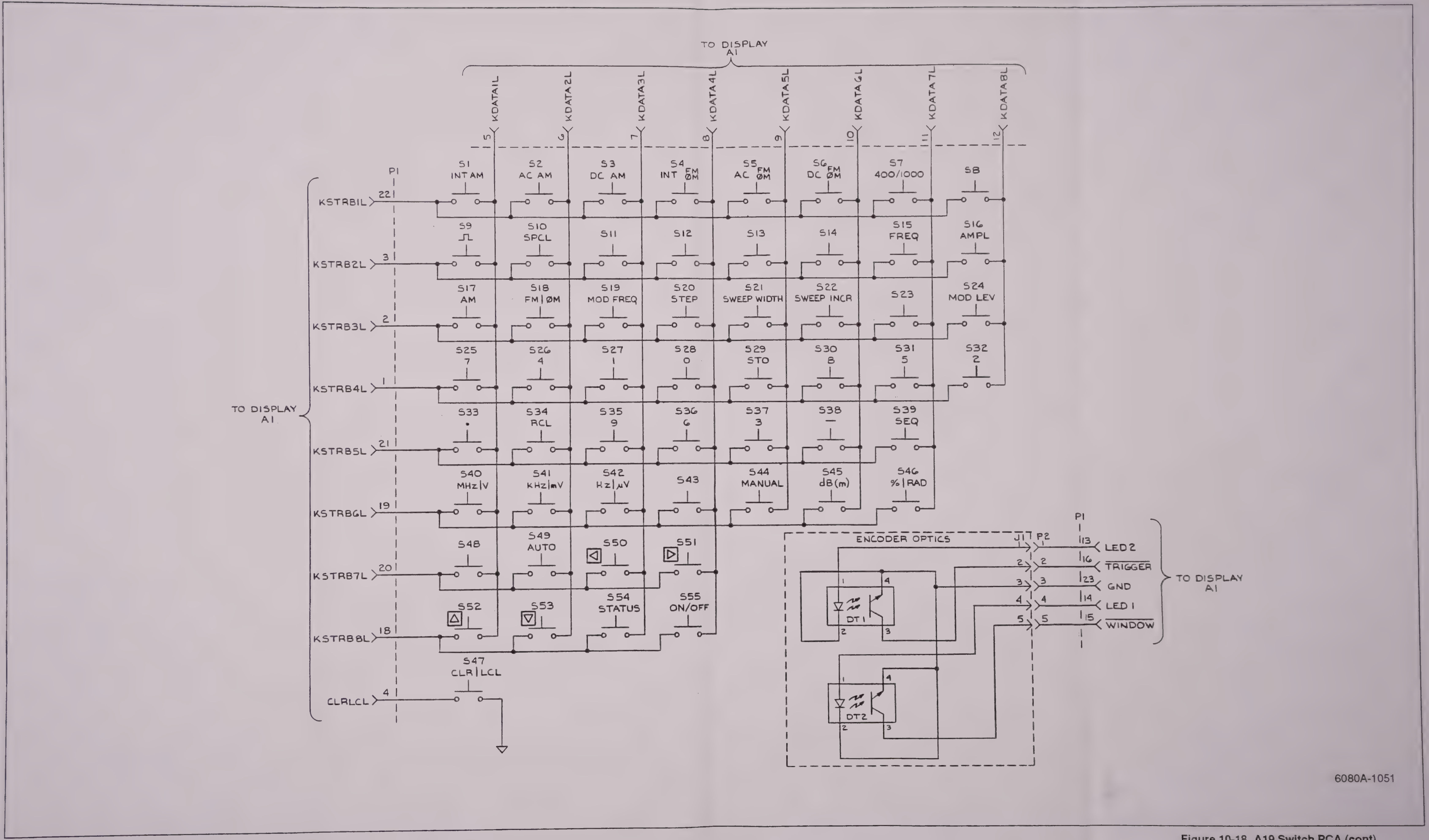
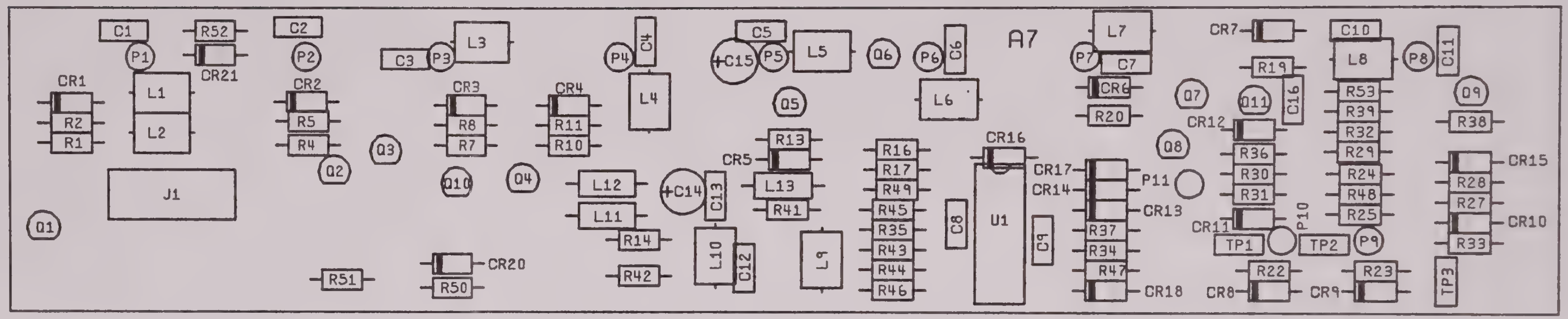
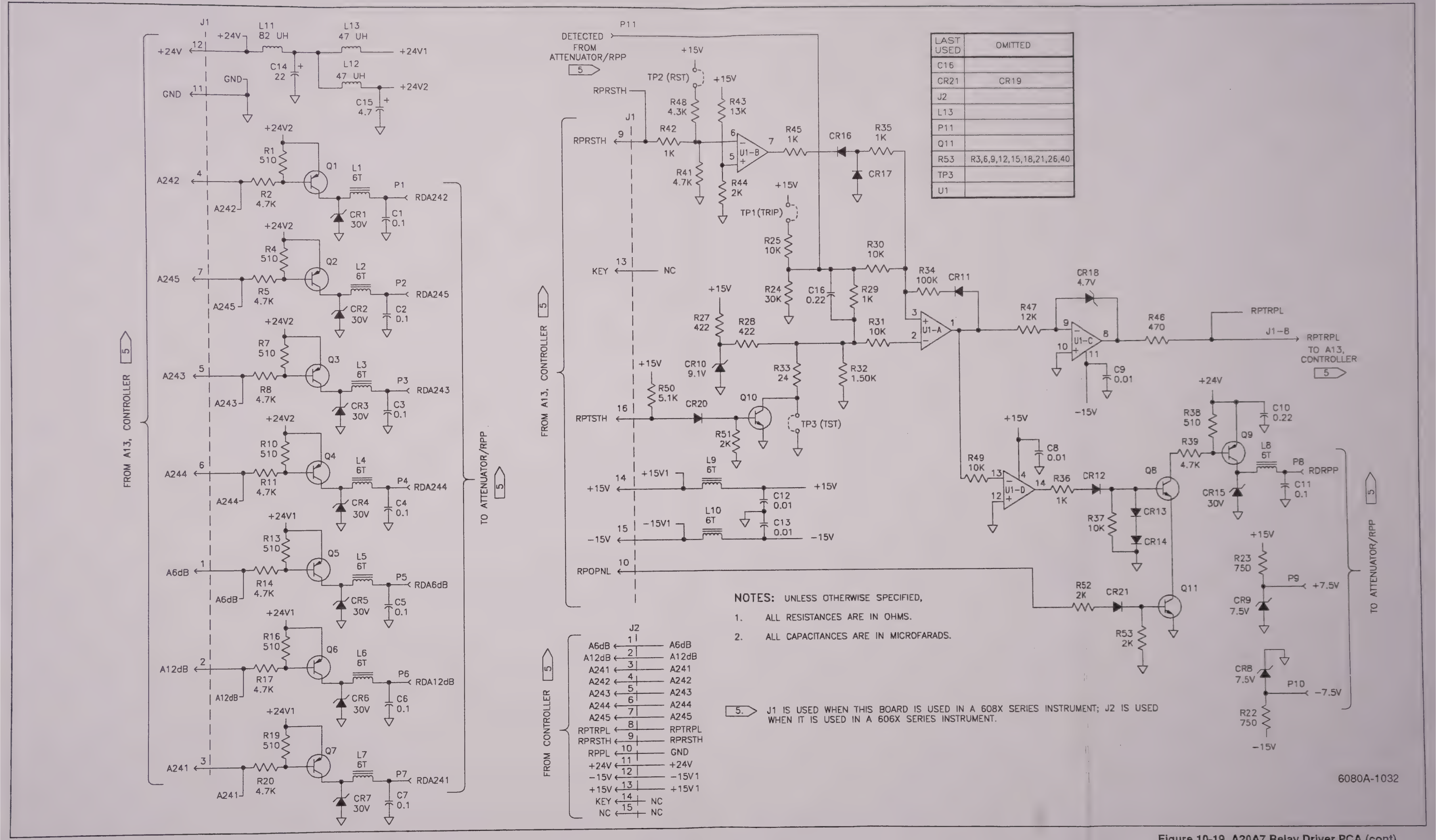

TO DISPLAY A1
KDATA1L
KDATA2L
KDATA3L
KDATA4L
KDATA5L
KDATA6L
KDATA7L
KDATA8L
5
6
7
8
9
10
11
12
P1
KSTRB1L
KSTRB2L
KSTRB3L
KSTRB4L
KSTRB5L
KSTRB6L
KSTRB7L
KSTRB8L
CLRLCL
22
3
2
1
21
19
20
18
4
TO DISPLAY A1
S1 INT AM
S2 AC AM
S3 DC AM
S4 INT FM ØM
S5 AC FM ØM
S6 DC FM ØM
S7 400/1000
S8
S9
S10 SPCL
S11
S12
S13
S14
S15 FREQ
S16 AMPL
S17 AM
S18 FM | ØM
S19 MOD FREQ
S20 STEP
S21 SWEEP WIDTH
S22 SWEEP INCR
S23
S24 MOD LEV
S25 7
S26 4
S27 1
S28 0
S29 STO
S30 8
S31 5
S32 2
S33 •
S34 RCL
S35 9
S36 6
S37 3
S38 —
S39 SEQ
S40 MHz | V
S41 kHz | mV
S42 Hz | μV
S43
S44 MANUAL
S45 dB(m)
S46 % | RAD
S48
S49 AUTO
S50
S51
S52
S53
S54 STATUS
S55 ON/OFF
S47 CLR | LCL
ENCODER OPTICS
J1
P2
P1
DT1
DT2
1
2
3
4
5
13
16
23
14
15
LED2
TRIGGER
GND
LED1
WINDOW
TO DISPLAY A1
6080A-1051

Figure 10-18. A19 Switch PCA (cont)


A7
C1
R52
CR21
C2
P1
P2
C3
P3
L3
CR1
L1
L2
R2
R1
CR2
R5
R4
Q2
Q3
CR3
R8
R7
Q10
Q4
CR4
R11
R10
P4
C4
L4
J1
Q1
R51
CR20
R50
L12
L11
R14
R42
C5
C15
P5
L5
Q5
R13
CR5
L13
R41
C14
C13
L10
C12
L9
Q6
P6
C6
L6
R16
R17
R49
R45
R35
R43
R44
R46
C8
CR16
U1
C9
L7
P7
C7
CR6
R20
CR17
CR14
P11
CR13
R37
R34
R47
CR18
Q7
Q8
CR7
R19
Q11
C16
CR12
R36
R30
R31
CR11
P10
TP1
TP2
R22
CR8
CR9
R23
C10
L8
P8
C11
R53
R39
R32
R29
R24
R48
R25
P9
Q9
R38
CR15
R28
R27
CR10
R33
TP3

6082A-1632

Figure 10-19. A20A7 Relay Driver PCA


J1
+24V
GND
L11 82 UH
L13 47 UH
L12 47 UH
C14 22
C15 4.7
+24V1
+24V2
A242
A245
A243
A244
A6dB
A12dB
A241
R1 510
R2 4.7K
R4 510
R5 4.7K
R7 510
R8 4.7K
R10 510
R11 4.7K
R13 510
R14 4.7K
R16 510
R17 4.7K
R19 510
R20 4.7K
Q1
Q2
Q3
Q4
Q5
Q6
Q7
L1 6T
L2 6T
L3 6T
L4 6T
L5 6T
L6 6T
L7 6T
CR1 30V
CR2 30V
CR3 30V
CR4 30V
CR5 30V
CR6 30V
CR7 30V
C1 0.1
C2 0.1
C3 0.1
C4 0.1
C5 0.1
C6 0.1
C7 0.1
P1 RDA242
P2 RDA245
P3 RDA243
P4 RDA244
P5 RDA6dB
P6 RDA12dB
P7 RDA241
FROM A13, CONTROLLER
TO ATTENUATOR/RPP
5
P11
DETECTED FROM ATTENUATOR/RPP
+15V
TP2 (RST)
RPRSTH
R48 4.3K
R43 13K
R42 1K
R41 4.7K
R44 2K
U1-B
R45 1K
CR16
R35 1K
CR17
TP1 (TRIP)
R25 10K
R30 10K
R24 30K
C16 0.22
R29 1K
R34 100K
CR11
CR18 4.7V
KEY
NC
R27 422
R28 422
R31 10K
U1-A
R47 12K
U1-C
R46 470
RPTRPL
J1-8
RPTRPL TO A13, CONTROLLER
C9 0.01
-15V
CR10 9.1V
R33 24
R32 1.50K
R50 5.1K
CR20
Q10
RPTSTH
R51 2K
TP3 (TST)
+15V1
L9 6T
C12 0.01
L10 6T
-15V1
C13 0.01
RPOPNL
R49 10K
C8 0.01
U1-D
R36 1K
CR12
R37 10K
CR13
CR14
Q8
+24V
R38 510
R39 4.7K
Q9
C10 0.22
L8 6T
P8 RDRPP
CR15 30V
C11 0.1
R23 750
P9 +7.5V
CR9 7.5V
CR8 7.5V
P10 -7.5V
R22 750
R52 2K
CR21
Q11
R53 2K
J2
FROM CONTROLLER
RPPL
6080A-1032

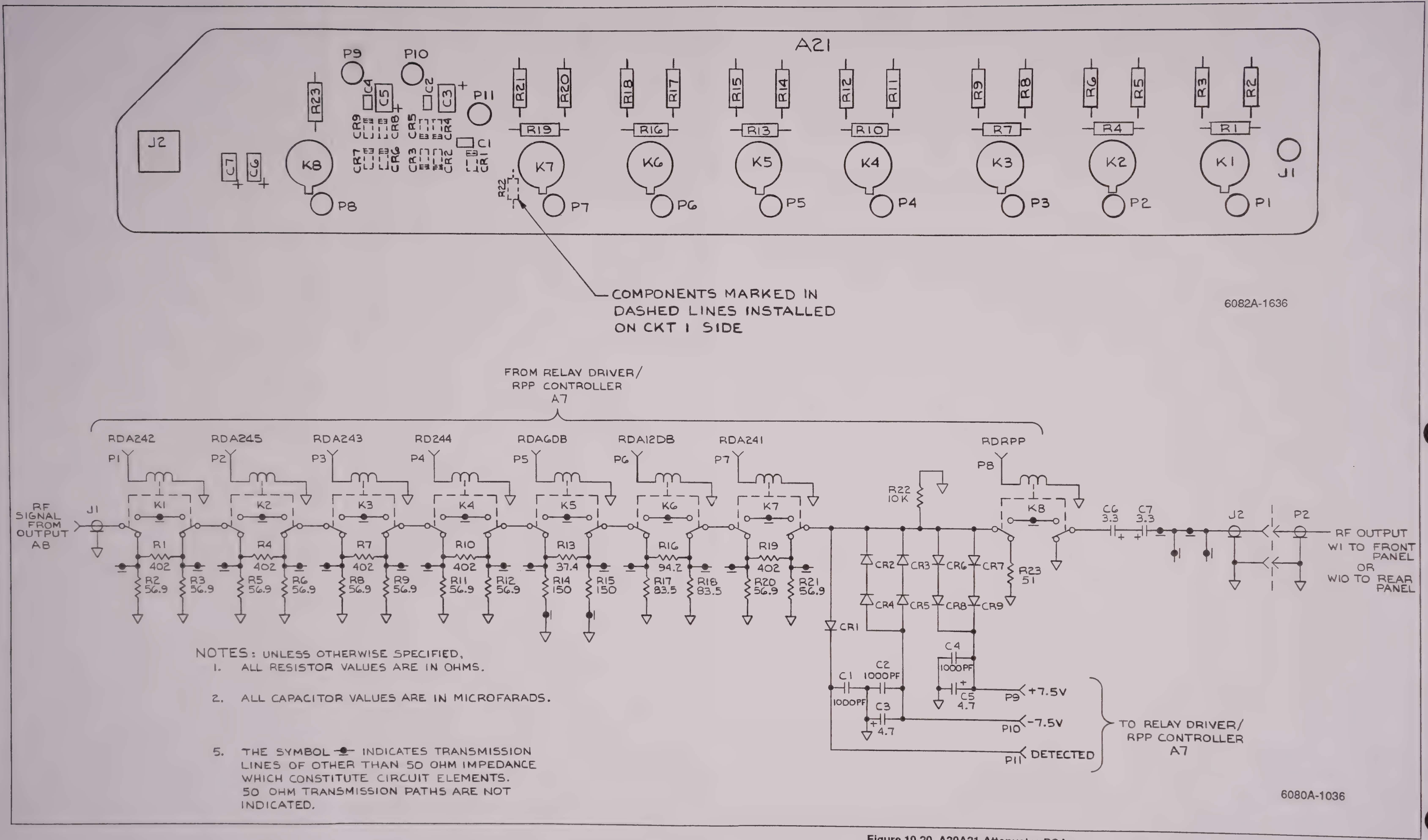
LAST USED	OMITTED
C16	
CR21	CR19
J2	
L13	
P11	
Q11	
R53	R3,6,9,12,15,18,21,26,40
TP3	
U1	

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES ARE IN OHMS.
2. ALL CAPACITANCES ARE IN MICROFARADS.

5. J1 IS USED WHEN THIS BOARD IS USED IN A 608X SERIES INSTRUMENT; J2 IS USED WHEN IT IS USED IN A 606X SERIES INSTRUMENT.

Figure 10-19. A20A7 Relay Driver PCA (cont)


A21
J2
C7
C6
R23
K8
P8
P9
P10
C4
C5
C2
C3
P11
CR9
CR8
CR5
CR4
CR7
CR6
CR3
CR2
C1
CR1
R22
R21
R20
R19
K7
P7
R18
R17
R16
K6
P6
R15
R14
R13
K5
P5
R12
R11
R10
K4
P4
R9
R8
R7
K3
P3
R6
R5
R4
K2
P2
R3
R2
R1
K1
P1
J1
COMPONENTS MARKED IN DASHED LINES INSTALLED ON CKT 1 SIDE
6082A-1636
FROM RELAY DRIVER/ RPP CONTROLLER A7
RDA242
RDA245
RDA243
RD244
RDA6DB
RDA12DB
RDA241
RDRPP
RF SIGNAL FROM OUTPUT A8
R1 402
R2 56.9
R3 56.9
R4 402
R5 56.9
R6 56.9
R7 402
R8 56.9
R9 56.9
R10 402
R11 56.9
R12 56.9
R13 37.4
R14 150
R15 150
R16 94.2
R17 83.5
R18 83.5
R19 402
R20 56.9
R21 56.9
R22 10K
R23 51
C6 3.3
C7 3.3
C1 1000PF
C2 1000PF
C3 4.7
C4 1000PF
C5 4.7
P9 +7.5V
P10 -7.5V
P11 DETECTED
TO RELAY DRIVER/ RPP CONTROLLER A7
RF OUTPUT W1 TO FRONT PANEL OR W10 TO REAR PANEL
6080A-1036

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
5. THE SYMBOL —●— INDICATES TRANSMISSION LINES OF OTHER THAN 50 OHM IMPEDANCE WHICH CONSTITUTE CIRCUIT ELEMENTS. 50 OHM TRANSMISSION PATHS ARE NOT INDICATED.

Figure 10-20. A20A21 Attenuator PCA

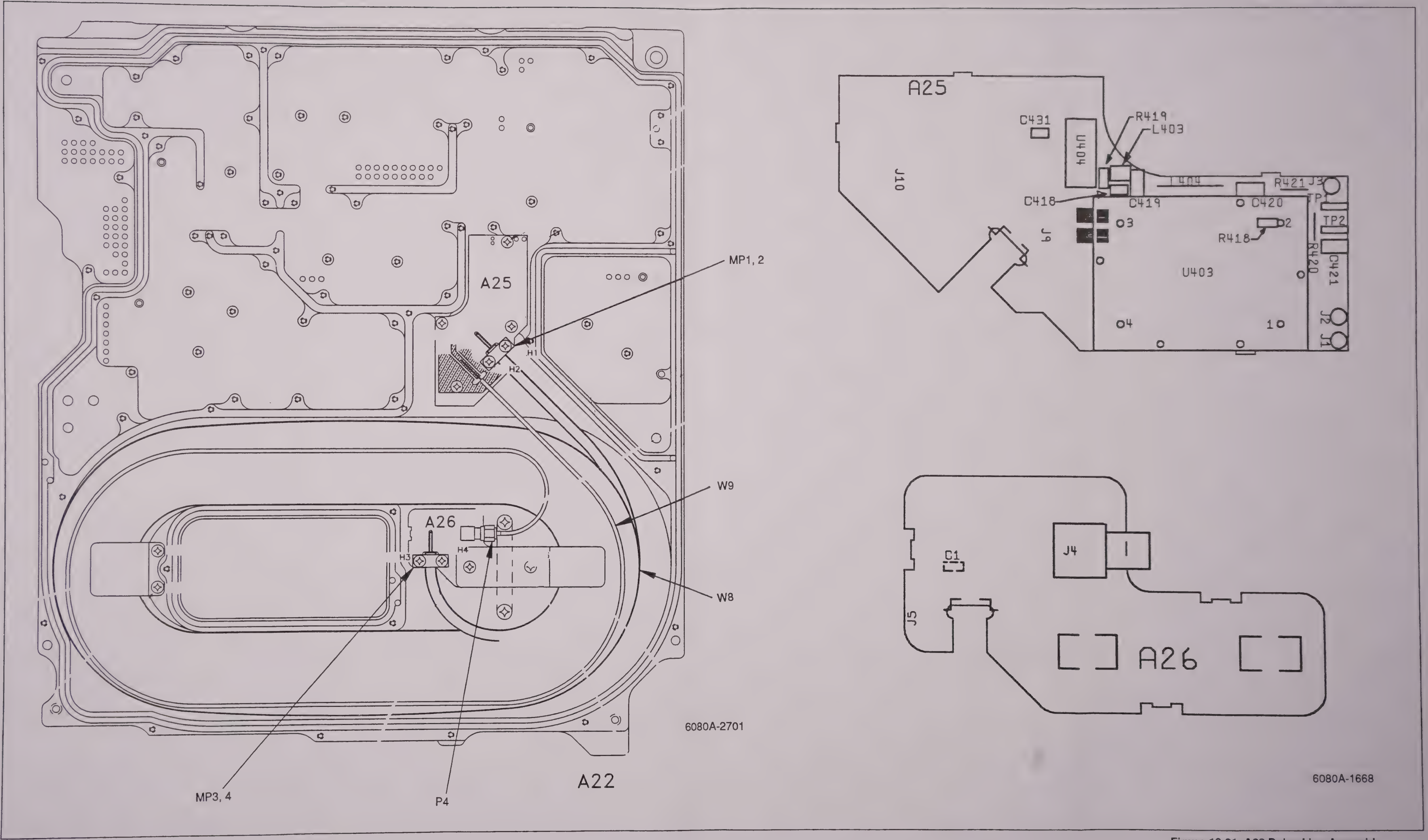
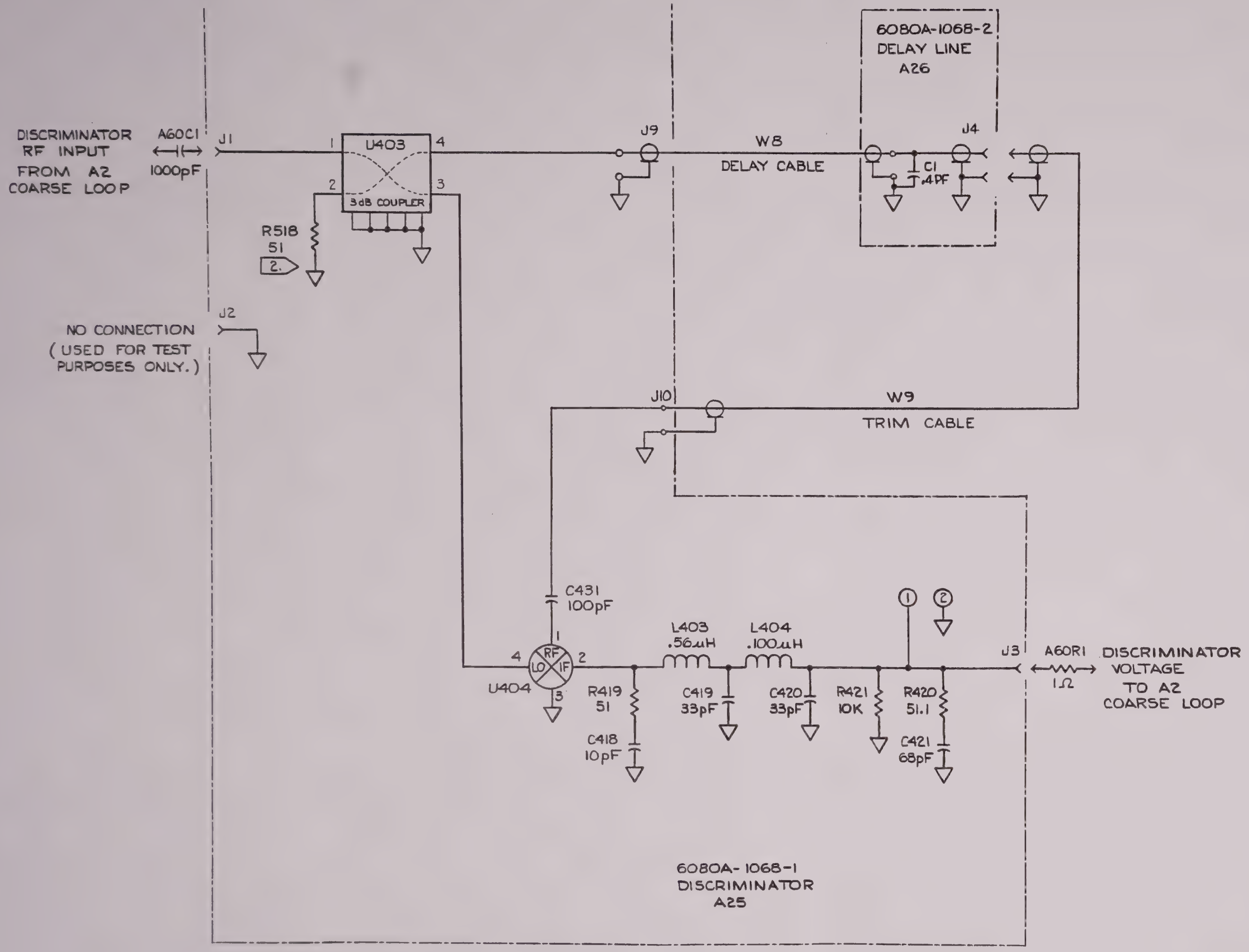

A25
MP1, 2
H1
H2
W9
A26
H4
H3
W8
6080A-2701
A22
MP3, 4
P4
A25
C431
U404
R419
L403
J10
C418
L404
R421
J3
TP1
C419
C420
TP2
J9
3
2
R418
R420
C421
U403
4
1
J2
J1
J4
C1
J5
A26
6080A-1668

Figure 10-21. A22 Delay Line Assembly


DISCRIMINATOR RF INPUT FROM A2 COARSE LOOP
A60C1
1000pF
J1
U403
1
2
3
4
3dB COUPLER
R518
51
2.
J9
W8
DELAY CABLE
6080A-1068-2
DELAY LINE
A26
J4
C1
.4PF
J2
NO CONNECTION
(USED FOR TEST PURPOSES ONLY.)
J10
W9
TRIM CABLE
C431
100pF
U404
RF
LO
IF
L403
.56uH
L404
.100uH
R419
51
C418
10pF
C419
33pF
C420
33pF
R421
10K
R420
51.1
C421
68pF
①
②
J3
A60R1
1Ω
DISCRIMINATOR VOLTAGE TO A2 COARSE LOOP
6080A-1068-1
DISCRIMINATOR
A25

NOTES: (UNLESS OTHERWISE SPECIFIED.)

1. ALL RESISTOR VALUES ARE IN OHMS.

2. PARTS INDICATED ARE MOUNTED ON TOP OF THE 3dB COUPLER.

3. "A22" REFERS TO THE ENTIRE DELAY CABLE ASSEMBLY. (BOTH BOARDS AND BOTH CABLES.)

6080A-1068

Figure 10-20. A22 Delay Line Assembly (cont)

Appendix A

Instrument Preset State

Appendix A. Instrument Preset State

FUNCTION	SET TO STATES		
	SPCL 00	RCL 97 [1]	SPCL 01 [2] (PRESET)
FREQUENCY			
Output frequency		1000 MHz	1000 MHz
Relative frequency mode (SPCL 20)	Off	Off	Off
AMPLITUDE			
Output amplitude		–140 dBm	–140 dBm
RF output state			On
Relative amplitude mode (SPCL 30)	Off	Off	Off
Fixed range amplitude (SPCL 50)	Normal	Normal	Normal
Amplitude display units (SPCL 840)	dBm	dBm	dBm
EMF-Volts amplitude display mode (SPCL 850)	Off	Off	Off
MODULATION			
AM depth		30 %	30 %
FM/ØM deviation		5 kHz	5 kHz
Modulation frequency		1 kHz	1 kHz
Modulation level		0 V	0 V
Pulse width		500 µs	500 µs
Internal AM		Off	Off
External AC AM		Off	Off
External DC AM		Off	Off
Internal FM/ØM		Off	Off
External AC FM/ØM		Off	Off
External DC FM/ØM		Off	Off
External pulse modulation		Off	Off
Modulation Oscillator output (SPCL 40)	On	On	On
Low-rate FM (SPCL 710)	Off	Off	Off
High-rate ØM (SPCL 720)	Off	Off	Off
Low-distortion/fixed range FM (SPCL 730)	Normal	Normal	Normal
Internal pulse modulation (SPCL 740)	Off	Off	Off
Modulation oscillator waveform (SPCL 750)	Sine	Sine	Sine
SWEEP			
Frequency sweep width		100 MHz	100 MHz
Frequency sweep increment		1 MHz	1 MHz
Amplitude sweep width		10 dB	10 dB
Amplitude sweep increment		.1 dB	.1 dB
Active sweep field		Freq.	Freq.
Sweep dwell time (SPCL 890)	0 s	0 s	0 s
Sweep symmetry (SPCL 880)	Sym.	Sym.	Sym.
Sweep mode			Off
EDIT			
Frequency bright-digit		10 MHz	10 MHz
Amplitude bright-digit		10 dBm	10 dBm
AM bright-digit		10 %	10 %
FM bright-digit		1 kHz	1 kHz

Appendix A. Instrument Preset State (cont)

FUNCTION	SET TO STATES		
	SPCL 00	RCL 98 [1]	SPCL 01 [2] (PRESET)
Modulation frequency bright-digit		1 kHz	1 kHz
Modulation level bright-digit		100 mV	100 mV
Modulation display field		FM	FM
Active bright-digit field		Freq.	Freq.
STEP			
Frequency step size		10 MHz	10 MHz
Amplitude step size		10 dB	10 dB
AM depth step size		10%	10%
FM/ØM deviation step size		1 kHz	1 kHz
Modulation frequency step size		1 kHz	1 kHz
Modulation level step size		.1 V	.1 V
Active step field		Freq.	Freq.
MISCELLANEOUS			
Display (SPCL 770)			On
Key repeat rate (SPCL 860)			Medium
Knob and step key operation (SPCL 870)			On, Step
Calibration/compensation procedures			Off
Amplitude compensation (SPCL 920)			All
REMOTE			
Service request enable (SPCL 13)			0
Event status enable			0
Instrument status change enable			0

NOTES:

1. *Store and recall operations include these parameters.*
2. *Power-on State.*

SPCL 00 and RCL 98 are not allowed while the 6080A/AN is sweeping.

The following instrument parameters are only set from the Fluke factory or with their associated commands:

External reference frequency (SPCL 760)	*Standard*
Memory dividers (SPCL 802)	*0,0,0,0*
Memory lock state (SPCL 810)	*Off*
Output compensation data (SPCL 930)	*Standard*
IEEE-488 address (SPCL 10)	*2*
IEEE-488 addressed/listen-only/talk-only (SPCL 11)	*Addressed*
IEEE-488 language (SPCL 12)	*6080 Language*
Secure mode (SPCL 820)	*Off*
RF Output Blanking (SPCL 780)	*Off*
Low noise external reference (SPCL 950)	*Off*
Nonvolatile memory erase repeat count (SPCL 828)	*12*

Appendix B

Special Function Table

Appendix B. Special Function Table

SPECIAL FUNCTION	DESCRIPTION
00	Clear special functions
01	Restore Instrument Preset State
02	Initiate power-on self tests
03	Display self test results
04	Display cal/comp memory checksum status
05	Display cal/comp memory data origins
06	Self tests with RF and pulse
08	Display option loading status
09	Display software revision level
10	Display/Set IEEE-488 address
11	Display/Set IEEE-488 address mode
12	Display/Set IEEE-488 language
13	Display/Enter service request mask
14	Set user request SRQ
15	Clear SRQ
20	Disable relative frequency mode
21	Enable relative frequency mode
30	Disable relative amplitude mode
31	Enable relative amplitude mode
40	Enable modulation oscillator output
41	Disable modulation oscillator output
42	Enter modulation frequency with 0.1 Hz resolution
50	Disable fixed range amplitude
51	Enable fixed range amplitude
701	Enable phase adjust mode
702	Zero phase adjust indicator
710	Disable low-rate FM
711	Enable low-rate FM
720	Disable high-rate ØM
721	Enable high-rate ØM
730	Select normal range FM
731	Select low-distortion range FM
732	Select fixed range FM
740	Disable internal pulse modulation
741	Enable internal pulse modulation
750	Select sine oscillator waveform
751	Select triangle oscillator waveform
752	Select square oscillator waveform

Appendix B. Special Function Table (cont)

SPECIAL FUNCTION	DESCRIPTION
758	Select pulse waveform
759	Enter pulse width
760	Use 10 MHz external reference input frequency
761	Use alternate external reference input frequency
770	Enable display
771	Disable display
780	Disable RF output blanking
781	Enable RF output blanking
801	Reset memory locations
802	Display/Set memory sequence dividers
808	Continuous memory sequence (860-862 select rate)
810	Unlock memory store operations
811	Lock memory store operations
820	Disable secure mode
821	Enable secure mode
828	Nonvolatile memory erase repeat count
829	Erase nonvolatile memory
840	Select dBm amplitude display units
841	Select dBmV amplitude display units
842	Select dBuV amplitude display units
843	Select dBf amplitude display units
850	Disable EMF-Volts amplitude display mode
851	Enable EMF-Volts amplitude display mode
860	Select medium key repeat rate
861	Select fast key repeat rate
862	Select slow key repeat rate
870	Normal knob and step key operation
871	Knob disabled, normal step key operation
872	Normal knob, step keys operate as EDIT up/down
873	Knob disabled, step keys operate as EDIT up/down
880	Select symmetrical sweep symmetry
881	Select asymmetrical sweep symmetry
882	Initiate single sweep
890	Select sweep dwell time of 0 ms
891	Select sweep dwell time of 20 ms
892	Select sweep dwell time of 50 ms
893	Select sweep dwell time of 100 ms
894	Select sweep dwell time of 200 ms
895	Select sweep dwell time of 500 ms
896	Select sweep dwell time of 1s

Appendix B. Special Function Table (cont)

SPECIAL FUNCTION	DESCRIPTION
897	Select sweep dwell time of 2s
898	Select sweep dwell time of 5s
899	Select sweep dwell time of 10s
901	Display test
902	Button test
903	Latch test
904	Initiate self tests with RF output enabled
905	Display operating time since manufacture in hours
907	Repair cal/comp memory checksum errors
909	Diagnostic preset state
910	Rear output option (-830) installed
920	Enable amplitude compensation
921	Disable all amplitude compensation
922	Disable attenuator amplitude compensation
923	Program alternate A24b attenuator
924	Program alternate A24c attenuator
925	Program alternate A24d attenuator
926	Program alternate A24e attenuator
930	Use normal output compensation data
931	Use alternate output compensation data
941	Set all internal DACs to zero
942	Set all internal DACs to half scale
943	Set all internal DACs to full scale
945	Display sum loop frequency
946	Display coarse loop frequency
947	Display subsynthesizer frequency
950	Disable low noise external reference mode
951	Enable low noise external reference mode
961	Transfer output MEC prom data
962	Transfer attenuator MEC prom data
963	Transfer subsynthesizer MEC prom data
971	Automatic coarse loop compensation procedure
972	Automatic sum loop compensation procedure
981	Front panel output compensation procedure
982	Front panel output compensation w/default attenuator procedure
983	Front panel attenuator compensation procedure
984	Front panel subsynthesizer compensation procedure
988	Front panel attenuator comp procedure (power meter)
989	Display Het offset adjustment following output comp procedure
991	Front panel AM calibration procedure
992	Front panel FM calibration procedure
993	Front panel level calibration procedure
994	Front panel reference oscillator calibration procedure

Appendix C

Rejected Entry Error Codes

Appendix C. Rejected Entry Error Codes

ERROR CODE	DESCRIPTION
FREQUENCY	
1	Frequency out of range
2	Frequency step size out of range
3	Frequency sweep width out of range
4	Frequency sweep increment out of range
AMPLITUDE	
10	Amplitude out of range
11	Amplitude units conversion out of range
12	Amplitude units conversion not allowed with voltage reference
13	Amplitude step size out of range
14	Amplitude step with mixed units not allowed
15	Amplitude step/sweep width/sweep increment units conversion not allowed
16	Amplitude sweep width out of range
17	Amplitude sweep increment out of range
AM	
20	AM depth out of range
21	AM step size out of range
FM/øM DEVIATION	
30	FM/øM deviation out of range
31	FM/øM step size out of range
32	FM/øM units conversion not allowed when external FM enabled
33	FM/øM units conversion out of range
34	FM/øM step with mixed units not allowed
35	FM/øM step units conversion not allowed
MOD FREQUENCY / MOD LEVEL	
40	Mod frequency out of range
41	Mod frequency step size out of range
42	Mod level out of range
43	Mod level step size out of range
44	Pulse width out of range
SWEEP	
50	Sweep field (Freq/Ampl) cannot be changed while sweeping
51	Sweep cannot be enabled with current sweep parameters
52	Entry conflicts with active sweep
53	Selected function not allowed while sweep is active
54	Amplitude sweep with mixed units not allowed
55	Selected function not allowed unless sweep is active

Appendix C. Rejected Entry Error Codes (cont)

ERROR CODE	DESCRIPTION
SPECIAL FUNCTION AND MEMORY	
60	Special function code invalid
61	Memory location number invalid
62	Memory location data invalid
63	Store operation not allowed when memory locked
64	Display ON not allowed when Secure ON
65	Nonvolatile memory erase failed
REMOTE	
70	IEEE address must be <= 30
71	IEEE invalid edit or step
72	IEEE invalid command
73	IEEE bad command syntax
74	IEEE bad argument value
75	IEEE bad argument type
76	IEEE bad argument count
77	IEEE invalid keyword
78	IEEE 488.2 unterminated command
79	IEEE 488.2 interrupted query
80	IEEE 488.2 I/O deadlock
81	IEEE error/status queue overflow
82	IEEE recursive trigger buffer not allowed
83	IEEE command not allowed in local mode or listen-only mode
84	IEEE query after indefinite response
CALIBRATION/COMPENSATION	
90	CAL|COMP switch not set to 1 (on)
91	Cal/comp adjustment out of range
92	Cal/comp procedure incomplete, data cannot be stored
93	Cal/comp data range error (too much correction)
94	Command not allowed during current cal/comp procedure
95	Command only allowed with appropriate cal/comp procedure
96	Internal cal/comp data transfer error
97	Stored cal/comp memory contains invalid data
98	MEC PROM ID code invalid, or MEC PROM checksum error
99	Sum loop compensation procedure failed
100	Coarse loop compensation procedure failed

Appendix D
Overrange/Uncal Status Codes

Appendix D. Overrange/Uncal Status Codes

STATUS CODE	DESCRIPTION
UNSPECIFIED OPERATION	
201	Level correction disabled
202	High-stability reference oven cold
HARDWARE LIMITED	
220*	Level DAC at 0(Amplitude fixed range)
221*	Level DAC at max(Amplitude fixed range)
222*	FM DAC at 0 (FM fixed range)
223*	FM DAC at max (FM fixed range)
224*	FM out of range for RF frequency band
225*	Mod frequency too low for pulse mode
226*	Pulse width >= 1/mod frequency
HARDWARE FAULT	
240*	RPP tripped
241*	ALC loop unleveled or AM overmodulation
242*	Sub synthesizer unlocked
243*	Coarse loop unlocked
244*	Sum loop unlocked
245*	Sum loop unleveled
246*	Reference unlocked
247*	FM loop unlocked or FM overmodulation
248*	DCFM DAC at 0
249*	DCFM DAC at max
250*	Multiple calibration/compensation memory errors

NOTE:

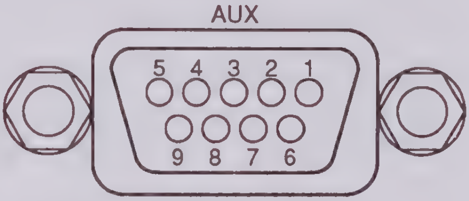
*Flashing codes (denoted by *) indicate abnormal operation or aberrated output. Non-flashing codes indicate operation outside specified range.*

Appendix E
Self-Test Status Codes

Appendix E. Self-Test Status Codes

STATUS CODE	DESCRIPTION
00	No self test errors
301	Self tests aborted
302	Calibration/compensation memory checksum test failed
303	Ram test failed
304	EPROM test failed
305	Non-volatile memory test failed
306	IEEE interface test failed
307-309	AM tests (See Service Manual)
310-317	FM tests (See Service Manual)
318-319	DCFM tests (See Service Manual)
320-323	Coarse loop tests (See Service Manual)
324-326	Subsynthesizer tests (See Service Manual)
327-333	Sum loop tests (See Service Manual)
334-336	RF output tests (See Service Manual)
337-338	Pulse modulator tests (See Service Manual)
339-356	Filter tests (See Service Manual)

Appendix F
Using Rear Panel AUX Connector Pinout



REAR PANEL VIEW

PIN	DIRECTION	FUNCTION
1	Input	Sequence down memory location
2	Input	Sequence up memory location
3	--	Ground
4	Output	Pen Lift/Blanking, TTL
5	Output	Sweep DAC, 0-10V
6	--	--
7	--	--
8	--	--
9	Input	Toggle bright digit between frequency and amplitude fields.

NOTE: This connector is for foot-pedal or other external switch control. The input lines are active when taken to ground (pin 3). The inputs lines do not repeat if held at ground. The pin 5 output, Sweep DAC, is a 0-10v dc analog signal for driving a plotter. See Section 4E in the Operator manual for more information.

Appendix G
Example Calibration Controller Programs

Appendix G consists of eight figures. Each figure is a listing of a calibration program that will run on the Fluke 1722A Controller. These figures are listed below:

- Figure G-1. Example AM Calibration Control Program
- Figure G-2. Example FM Calibration Control Program
- Figure G-3. Example Level Calibration Control Program
- Figure G-4. Example Reference Calibration Control Program
- Figure G-5. Example Output/Attenuator Compensation and Level Cal Program
- Figure G-6. Example Sub-Synthesizer Compensation
- Figure G-7. Example Coarse Loop Compensation
- Figure G-8. Example Sum Loop Compensation

Figure G-1. Example AM Calibration Control Program

```
5    ! Fluke 6080A Signal Generator AM calibration control program.
6    !    Runs on a Fluke 1722A controller.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS".  No indemnity or warranties
14   !    are provided, whether expressed or implied.  FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use.  In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
70   INIT PORT 0%
80   A% = 2%                      ! IEEE-488 address of Signal Generator
90   AM% = 14%                    ! IEEE-488 address of Modulation Analyzer
100  PRINT @ A%,"*rst;*cls"       ! initialize Signal Generator
110  GOSUB 3000                   ! initialize Modulation Analyzer
120  !
130  PRINT @A%,"cal_am"          ! enter AM calibration procedure
140  PRINT @A%,"error? explain" \ INPUT @ A%,ST%,EM$
150  IF (ST% = 0) THEN GOTO 1000
160      PRINT "There is an error with the 6080A."
170      PRINT ST%,EM$
180      STOP
1000 !
1010 ! Main loop
1020 !
1030     ! get frequency, exit main loop on last frequency
1040     PRINT @ A%,"cc_freq?" \ INPUT @ A%,F,UN$
1050     IF (F = 9E9) GOTO 2000
1060     !
1140     ! get modulation analyzer reading
1150     GOSUB 4000               ! reading -> RD
1160     !
1170     ! send modulation analyzer reading to 6080A
1180     PRINT @ A%,"cc_rdam";RD;"pct"
1190 GOTO 1000
2000 !
2010 ! Store results
2020 !
2030 PRINT @ A%,"cc_save"         ! save data in compensation memory
2040 WAIT 5000                    ! wait 5 seconds for store to complete
2050 PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
2060 IF (ST% = 0) THEN GOTO 2100
2070     PRINT "The store operation failed."
2080     PRINT EM$
2090     STOP
2100 LOCAL
```

```
2110 END
3000 !
3010 ! Subroutine to initialize HP 8901 Modulation Analyzer
3020 !
3030     PRINT @ AM%,"AUM1T0"     ! Automatic operation, AM, Free Run
3040     PRINT @ AM%,"H1L1D1"     ! 50 Hz HP Filter on, 3 kHz LP on, Peak+
3050 RETURN
4000  !
4010  ! Subroutine to get readings from HP 8901 Modulation Analyzer
4020  ! Give the modulation analyzer 700 msec to settle.  Then get
4030  ! readings until two are within 0.1%.  Get one more reading
4035  ! and return the average of all three.
4040  !
4050  INPUT @ AM%,R1
4060  !
4070  WAIT 700
4100  INPUT @ AM%,RD
4110  IF ABS(RD-R1) <= 0.1 THEN GOTO 4200
4120  R1 = RD
4130  GOTO 4100
4200  R1 = RD + R1
4210  INPUT @ AM%,RD
4220  RD = (RD + R1)/3
4230  RETURN
```

Figure G-2. Example FM Calibration Control Program

```
5    ! Fluke 6080A Signal Generator FM calibration control program.
6    !    Runs on a Fluke 1722A controller.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS".  No indemnity or warranties
14   !    are provided, whether expressed or implied.  FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use.  In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
50   ! Initialization
60   !
70   INIT PORT 0%
80   A% = 2%                      ! IEEE-488 address of Signal Generator
90   AM% = 14%                    ! IEEE-488 address of Modulation Analyzer
100  PRINT @ A%,"*rst;*cls"       ! initialize Signal Generator
110  GOSUB 3000                   ! initialize Modulation Analyzer
120  !
130  PRINT @ A%,"cal_fm"          ! enter FM calibration procedure
140  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
150  IF (ST% = 0) THEN GOTO 1000
160      PRINT "There is an error with the 6080A."
170      PRINT ST%,EM$
180      STOP
1000 !
1010 ! Main loop
1020 !
1030     ! get frequency, exit main loop on last frequency
1040     PRINT @ A%,"cc_freq?" \ INPUT @ A%,F,UN$
1050     IF (F = 9E9) GOTO 2000
1060     !
1140     ! get modulation analyzer reading
1150     GOSUB 4000               ! reading -> RD
1160     !
1170     ! send modulation analyzer reading to 6080A
1180     PRINT @ A%,"cc_rdfm";RD;"hz"
1190 GOTO 1000
2000 !
2010 ! Store results
2020 !
2030 PRINT @ A%,"cc_save"         ! save data in compensation memory
2040 WAIT 5000                    ! wait 5 seconds for store to complete
2050 PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EX$
2060 IF (ST% = 0) THEN GOTO 2100
2070     PRINT "The store operation failed."
2080     PRINT ST%,EX$
```

```
2090     STOP
2100 LOCAL
2110 END

3000 !
3010 ! Subroutine to initialize HP 8901 Modulation Analyzer
3020 !
3030     PRINT @ AM%,"AUM2TO"     ! Automatic operation, FM, Free Run
3040     PRINT @ AM%,"H1L1D1"     ! 50 Hz HP Filter on, 3 kHz LP on, Peak+
3050 RETURN

4000  !
4010  ! Subroutine to get readings from HP 8901 Modulation Analyzer
4020  ! Give the modulation analyzer 700 msec to settle.  Then get
4030  ! readings until two are within 100 hz.  Get one more reading
4035  ! and return the average of all three.
4040  !
4050  INPUT @ AM%,R1
4060  !
4070  WAIT 700
4100    INPUT @ AM%,RD
4110    IF ABS(RD-R1) <= 100 THEN GOTO 4200
4120    R1 = RD
4130    GOTO 4100
4200  R1 = RD + R1
4210  INPUT @ AM%,RD
4220  RD = (RD + R1)/3
4230  RETURN
```

Figure G-3. Example Level Calibration Control Program

```
1    ! Fluke 6080A Signal Generator Level calibration control program.
2    !    Runs on a Fluke 1722A controller.
3    !
4    ! NOTE: enter the power meter calibration factors for your power
5    !    meter into the table in the subroutine beginning at line
6    !    7000.  Remember to specify the number of entries in the table.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS".  No indemnity or warranties
14   !    are provided, whether expressed or implied.  FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use.  In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
50   INIT PORT 0
60   A% = 2%                      ! IEEE-488 address of Signal Generator
70   AP% = 13%                    ! IEEE-488 address of Power Meter
80   PRINT @ A%,"*rst;*cls"       ! initialize Signal Generator
90   GOSUB 3000                   ! initialize Power Meter
100  GOSUB 7000                   ! set up CAL factor tables
640  PRINT @ A%,"cal_level"
650  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
660  IF (ST% = 0 ) THEN GOTO 800
670      PRINT "There is an error with the 6080A."
680      PRINT ST%,EM$
690      STOP
800  !
810  GOSUB 5000                   ! zero power meter
1000 !
1010 ! Main loop
1020 !
1030     ! get frequency, exit main loop on last frequency
1040     PRINT @ A%,"cc_freq?" \ INPUT @ A%,F,UN$
1050     IF (F = 9E9) GOTO 2000
1060     !
1130     ! get power meter reading
1140     GOSUB 4000               ! reading -> RD
1150     !
1160     ! send power meter reading to 6080A
1170     PRINT @ A%,"cc_rdpower";RD;"dbm"
1180 GOTO 1000
2000 !
2010 ! Store results
2020 !
2030 PRINT @ A%,"cc_save"         ! save data in compensation memory
2040 !
```

```
2050 PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
2060 IF (ST% = 0) THEN GOTO 2900
2080     PRINT "The store operation failed."
2090     PRINT ST%,EM$
2100     STOP
2110 !
2900 LOCAL
2910 END
3000 !
3010 ! Subroutine to initialize HP 436A Power Meter
3020 ! P$ is used when zeroing the power meter too
3030 !
3040     P$ = "D+9H"          ! dBm mode, no CAL factor, auto range, Hold
3050     PRINT @ AP%,P$
3060     PRINT @ AP%,"I"      ! get first reading
3070     INPUT LINE @ AP%,RD$ ! throw it away
3080 RETURN
4000 !
4010 ! Subroutine to get readings from HP 436A Power Meter
4020 !
4030 ! Get two readings within .01 dB, then read eight
4040 !   more and return the average of all ten.
4050 !
4060     ! set delay to 200 ms or 400 ms if 24 dB pad
4070     WT% = 200%
4090     !
4100     ! wait 2 seconds
4110     WAIT 2000 \ PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4120     !
4130     R1 = VAL(RIGHT(RD$,4))
4480     !
4490     ! get settled reading
4500     !
4510         WAIT WT% \ PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4520         RD = VAL(RIGHT(RD$,4))
4530         IF ABS(RD-R1) <= .01 THEN GOTO 4600
4540         R1 = RD
4550     GOTO 4500
4580     !
4590     ! The reading is in the settled range, now average more.
4600     R1 = R1 + RD    ! sum includes last 2 readings
4605     AV = 10.0
4610     FOR I% = 1% TO (AV-2)
4620        PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4630        RD = VAL(RIGHT(RD$,4))
4640        R1 = R1 + RD
4650     NEXT I%
4660     RD = R1 / AV
4670     !
4800     GOSUB 6000               ! power meter CAL factor -> CF
4810     RD = RD + CF
4840 RETURN
5000 !
5010 ! Subroutine to zero HP 436A Power Meter
5020 ! P$ is set up in the power meter initialization routine
```

```
5030 !
5040     PRINT @ A%,"rfout off" \ WAIT 3000
5050     PRINT @ AP%,"Z1T" \ WAIT 30
5060     PRINT @ AP%,P$ \ WAIT 5000
5070     PRINT @ A%,"rfout on" \ WAIT 30
5080 RETURN
6000 !
6010 ! Subroutine to compute power meter CAL factor
6020 !
6030     ! use first data point if frequency is low
6040     CF = 10 * LOG(1/CA(1%))
6050     IF (F/1.0E6 <= FR(1%)) THEN RETURN
6060     !
6070     ! use last data point if frequency is high
6080     CF = 10 * LOG(1/CA(30%))
6090     IF (F/1.0E6) >= FR(30%) THEN RETURN
6100     !
6110     ! search table for closest frequency points
6120     I% = 1%
6130     IF (F/1.0E6 < FR(I%)) THEN GOTO 6500
6140     I% = I% + 1%
6150     GOTO 6130
6500     !
6510     ! interpolate between frequency points
6520     D = (F/1.0E6 - FR(I%-1%)) / (FR(I%)-FR(I%-1%))
6530     C = ( D * (CA(I%)-CA(I%-1%)) ) + CA(I%-1%)
6540     !
6550     ! convert ratio to dB
6560     CF = 10 * LOG(1/C)
6570 RETURN
7000 !
7010 ! Subroutine to set up CAL factor tables
7020 !
7030 ! Number of frequencies used - Maximum of 30
7040 DATA 11
7050 !
7060 ! Table of Frequencies in MHz, and CAL factors
7065 !    as multiplicative scale factors.
7066 !    (Nominally multiply by 1.00).
7070 DATA   .1, 1.00
7080 DATA   .3, 1.00
7090 DATA    1, 1.00
7100 DATA    3, 1.00
7110 DATA   10, 1.00
7120 DATA   30, 1.00
7130 DATA  100, 1.00
7140 DATA  300, 1.00
7150 DATA 1000, 1.00
7160 DATA 1700, 1.00
7170 DATA 2100, 1.00
7300 !
7310 DIM FR(30%), CA(30%)
7320 !
7330 READ N% \ IF (N% > 30%) THEN N% = 30%
7340 FOR I% = 1% TO N%
```

```
7350     READ FR(I%) ! load frequency table
7360     READ CA(I%) ! load CAL factor table
7370 NEXT I%
7380 !
7390 !
7400 FOR I% = N%+1% TO 30%
7410     FR(I%) = FR(N%) ! fill in rest of tables
7420     CA(I%) = CA(N%)
7430 NEXT I%
7440 RETURN
```

Figure G-4. Example Reference Calibration Control Program

```
5    ! Fluke 6080A Signal Generator Reference calibration control program.
6    !    Runs on a Fluke 1722A controller.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS".  No indemnity or warranties
14   !    are provided, whether expressed or implied.  FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use.  In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
70   INIT PORT 0%
80   A%  =  2%                    ! IEEE-488 address of Signal Generator
90   FC% = 20%                    ! IEEE-488 address of Frequency Counter
100  PRINT @ A%,"*rst;*cls"       ! initialize Signal Generator
110  GOSUB 3000                   ! initialize counter
112  !
120  !
130  PRINT @A%,"cal_refosc"       ! enter Reference Osc. Cal procedure
140  PRINT @A%,"error? explain" \ INPUT @ A%,ST%,EM$
150  IF (ST% = 0) THEN GOTO 1000
160      PRINT "There is an error with the 6080A."
170      PRINT ST%,EM$
180      STOP
1000 !
1010 ! Main loop
1020 !
1030     ! get frequency, exit main loop on last frequency
1040     PRINT @ A%,"cc_freq?" \ INPUT @ A%,F,UN$
1050     IF (F = 9E9) GOTO 2000
1060     !
1140     ! get counter reading
1150     GOSUB 4000               ! reading -> RD
1160     !
1170     ! send modulation analyzer reading to 6080A
1180     PRINT @ A%, USING "##########", "cc_rdfreq";RD;"hz"
1190 GOTO 1000
2000 !
2010 ! Store results
2020 !
2030 PRINT @ A%,"cc_save"         ! save data in compensation memory
2040 WAIT 5000                    ! wait 5 seconds for store to complete
2050 PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
2060 IF (ST% = 0) THEN GOTO 2900
2070     PRINT "The store operation failed."
2080     PRINT EM$
2090     STOP
```

```
2900 LOCAL
2910 END

3000 !
3010 ! Subroutine to initialize Fluke 1953A Counter
3020 !   reset counter (input port A, trigger level 0 Volts
3030 !       positive slope AC coupled).
3040 !   select 1 second range and triggered mode
3050 !
3060     PRINT @ FC%,"C R4 H1"
3070 RETURN

4000  !
4010  ! Subroutine to get readings from Fluke 1953A Counter
4020  ! Give the counter 2 seconds to settle.  Then get
4030  ! readings until two are within 5 hz.  Get one more reading
4035  ! and return the average of all three.
4040  !
4050  PRINT @FC%,"T" \ WAIT 1000 \ INPUT @ FC%,R1
4060  !
4070  WAIT 2000
4100  PRINT @FC%,"T" \ WAIT 1000 \ INPUT @ FC%,RD
4110  IF ABS(RD-R1) <= 5 THEN GOTO 4200
4120  R1 = RD
4130  GOTO 4100
4200  R1 = RD + R1
4210  PRINT @FC%,"T" \ WAIT 1000 \ INPUT @ FC%,RD
4220  RD = (RD + R1)/3
4230  RETURN
```

Figure G-5. Example Output/Attenuator Compensation and Level Cal Program

```
2       ! Fluke 6080A/82A Signal Generator Output/Attenuator compensation
4       !    and Level calibration control program. Runs on a Fluke 1722A
6       !    controller using an HP8902 Measuring Receiver as the level
8       !    test set.
10      !
12      ! This program allows the following procedures to be performed:
14      !     * Output compensation
16      !     * Attenuator compensation
18      !     * Output compensation with default attenuator data
20      !     * Level Calibration
22      !     * Verification of level performance
24      !         The verification frequencies are specified in a table
26      !         in the subroutine beginning at line 12000.
28      !
30      ! The rear panel CAL|COMP switch must be set to 1 (on) before
32      !    running this program.
34      !
36      ! Disclaimer:
38      !
40      !    This program is provided "AS IS".  No indemnity or warranties
42      !    are provided, whether expressed or implied.  FLUKE specifically
44      !    disclaims the implied warranties or merchantability and fitness
46      !    for the purpose or use.  In no event shall FLUKE be liable for
48      !    any loss of data, use, profits or goodwill, or for special,
50      !    incidental, consequential or other similar damages.
52      !
54      !
56      !
58      !
90      ! Initialization
100     TIMEOUT 30000
110     ON CTRL/C GOTO 30000
115     ON ERROR  GOTO 29000
120     !
130     GOSUB 25000                           ! Select procedure
140     !
150     INIT PORT 0
160     A% =   2% \ REMOTE @A%  \ CLEAR @A%   ! IEEE-488 addr of Sig Gen
170     LT% = 14% \ REMOTE @LT% \ CLEAR @LT%  ! IEEE-488 addr of Level Test Set
180     LO% = 19% \ REMOTE @LO% \ CLEAR @LO%  ! IEEE-488 addr of Local Osc
190     !
200     PRINT @ A%,"*rst;rfout on;*cls"       ! Initialize Signal Generator
210     GOSUB 3000                            ! Initialize Level Test Set
220     PRINT @LO%,"*rst;rfout on;*cls"       ! Initialize Local Oscillator
230     !
240     IF(MD$ = "verify") THEN GOSUB 10000 ELSE GOSUB 500
250     !
260     GOTO 30000                            ! cleanup and exit
500     !
510     !-------------------------------------------------------------
520     ! Main test subroutine
530     !
```

```
540   ! Performs the following actions:
550   !
560   !    * Initiates the comp procedure
570   !    * Main Loop
580   !        * Get frequency and exit if "end-code"
590   !        * Get Reading from Level Test Set
600   !        * Send Reading to Signal Generator
610   !        * End Loop
620   !    * Store results
630   !
640   !
720   TS$ = TIME$                    ! Save start time for later
730   GOSUB 3000
770   !
780   PRINT @ A%,MD$                 ! Initiate compensation procedure
790   PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,ST$
800   IF (ST% = 0 ) THEN GOTO 850
810       PRINT ST%, ST$
820       STOP
830   !
840   ! Get power-meter/level test set "break frequency"
850   PRINT @ A%, "CC_BRKFREQ?"
860   INPUT @ A%, BF, SF$
870   !
880   TP = -9999                     ! Initialize "TP" to invalid value
890   F = 0
1000  !
1010  ! Main loop
1020  !
1030      ! get frequency, exit main loop on last frequency
1040      FL = F
1050      PRINT @ A%,"CC_FREQ?" \ INPUT @ A%,F,UN$
1060      IF (F = 9E9) GOTO 2000                  ! Quit if "end-code"
1070      IF (F <> FL) THEN GOSUB 6000            ! Tune if new freq
1080      !
1090      PRINT @ A%,"CC_TARGET?" \ INPUT @A%,T,UN$  ! Read target value
1100      !
1110      ! Zero power-meter or switch to tuned RF mode if necessary
1120      GOSUB 5000
1130      TP = T
1140      !
1150      ! get reading
1160      AP = T                     ! "AP" approximates expected reading
1170      GOSUB 4000                 ! reading -> RD
1180      !
1190      PRINT F/1E6,
1200      PRINT USING "S####.###",RD,RD-T
1210      !
1220      ! send reading to Signal Generator
1230      PRINT @ A%,"CC_RDPOWER ";RD;" DBM"
1240  GOTO 1000
2000  !
2010  ! Store results
2020  !
2030  PRINT @ A%,"CC_SAVE"           ! save data in compensation memory
```

```
2040  WAIT 30000                   ! wait 30 seconds for store to complete
2050  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,ST$
2060  IF (ST% = 0 ) THEN GOTO 2090
2070      PRINT ST%, ST$
2080      STOP
2090  PRINT "started at :";TS$,"ended at :";TIME$
2100  RETURN
3000  !
3010  !-------------------------------------------------------------
3020  ! Subroutine to initialize HP 8902A
3030  !
3040  !
3050  IL = 120.53E6                    ! Intermediate Freq of LO
3060  LF = 2.5E6                       ! Lowest freq in tuned RF mode
3070  PRINT @ A%,  "freq 100 khz; ampl 10 dbm" \ WAIT 500
3080  PRINT @ LT%, "AU 100kz 22.32SP"  ! Enable RECAL/UNCAL serial poll bit
3090  PRINT @ LT%, "27.0sp 32.0sp"     ! 0.01 dB res, disable offset mode
3100  PRINT @ LT%, "M4 LG" \ WAIT 500  ! Power-meter mode in dBm
3110  AP=0 \ F=0 \ GOSUB 16000         ! zero power-meter
3120  RETURN
4000  !
4010  !-------------------------------------------------------------
4020  ! Subroutine to get readings from HP 8902A
4030  !
4040  ! Get two readings within specified tolerance, then read
4050  !   (AV-2) more and returns the average of all.
4060  !
4070  ! The delay between readings, and the "window" of valid readings
4080  !   is dependent on the expected level.  At lower levels, We must
4090  !   wait longer between readings and expect more rattle.
4100  !   Note: -14 dBm is near the lower end of the power-meter range
4110  !         so it is slower and has more rattle.
4120  !
4130  !   Inputs:  AP = approximates expected reading
4140  !   Outputs: RD = settled and averaged reading
4150  !
4160  !   Local:   AV  = number of readings averaged
4170  !            WN  = Settled reading window
4180  !            WS% = Wait between readings during settling period
4190  !            WI% = Wait between readings during average period
4200  !
4210  AV  = 15.0
4220  WI% = 50
4230  !
4240  GOSUB 8200                ! short delay
4250                                 WS% =  100 \ WN = 0.01   ! default
4260  IF (AP =  -14 AND F < LF) THEN WS% = 2000 \ WN = 0.01
4270  IF (AP <  -40) THEN WAIT 500 \ WS% =  100 \ WN = 0.01
4280  IF (AP <  -80) THEN WAIT 750 \ WS% =  500 \ WN = 0.01
4290  IF (AP < -110) THEN WAIT 750 \ WS% = 1000 \ WN = 0.02
4300  !
4310  INPUT @LT%,R1
4480  !
4490  ! get settled reading
4500  !
```

```
4510      WAIT WS%
4520      INPUT @LT%,RD
4530      IF( ABS(RD-R1) <= WN ) THEN GOTO 4600
4540      R1 = RD
4550  GOTO 4500
4580  !
4590  ! The reading is in the settled range, now average more.
4600  R1 = R1 + RD     ! sum includes last 2 readings
4610  FOR I% = 1% TO (AV-2)
4620      WAIT WI% \ INPUT @LT%,RD
4640      R1 = R1 + RD
4650  NEXT I%
4660  RD = R1 / AV
4670  !
4680  RETURN
5000  !
5010  !--------------------------------------------------------------
5020  ! Zero power-meter mode or switch to tuned RF mode
5030  !
5040  ! This routine is called after each settled reading has
5050  ! been sent to the SigGen or when the frequency or amplitude
5060  ! changes during verification.  It performs the following actions:
5200  !
5210  ! * If below 8902's tuned RF range and measuring first 24 dB pad,
5220  !        zero power-meter.
5230  ! * If in 8902's tuned RF range and measuring first 24 dB pad,
5240  !        switch to tuned RF mode. (different level for verification).
5600  !
5610  ! When below tuned RF range: Zero power meter at first 24 dB pad
5620  IF (F < LF) AND (T<=-14) AND (TP >-14) THEN GOSUB 16000 \ RETURN
5630  !
5640  ! When in tuned RF range: Switch to tuned RF mode at first 24 dB pad
5650  IF (F < LF) THEN RETURN
5660    IF(MD$<>"verify") AND(T<=-14.0) AND(TP >-14.0) THEN GOSUB 9000\RETURN
5670    IF(MD$= "verify") AND(T<=-11.1) AND(TP >-11.1) THEN GOSUB 9000\RETURN
5680  RETURN
6000  !
6010  !--------------------------------------------------------------
6020  !
6030  ! Tune new frequency for Attenuator Compensation procedures.
6040  !     Performs all 8902 Calibration transfers for this frequency.
6050  !
6060  ! Note: When running the procedure with a 6082, the 8902 system must
6070  !    contain a microwave converter and an additional 6082 as a local
6080  !    oscillator.
6200  !
6210  IF( MD$ = "comp_att" OR MD$ = "verify") THEN GOTO 6300
6220    ! new frequency, tune 8902 and short delay
6230    PRINT @ LT%, F/1E6; " MZ M4" \ GOSUB 8200
6240    RETURN
6300  !
6310  ! Attenuator procedure only:
6320  !    Skip to 6082 code if above 1300 MHz
6330  !
6340  IF(F > 1300E6) THEN GOTO 6500
```

```
6350    !
6360    !  6080 Code: Program new frequency
6370    PRINT @ LT%, F/1E6; " MZ M4" \ GOSUB 8200
6380    !
6390    !  If freq is above the break-freq, Cal tuned RF mode then resume.
6400    !      (except during verification)
6410    IF (F>=BF AND MD$<>"verify") THEN GOSUB 7000 \PRINT @A%,"cc_resume"
6420    RETURN
6500  !
6510  ! 6082 Code: Program LO, and 8902 frequency and frequency offset.
6520  !
6530  IF( F >= 1900E6 ) THEN FO = F - IL    ! determine 8902 freq offset
6540  IF( F <  1900E6 ) THEN FO = F + IL
6550  !
6560  ! Program Local Oscillator and 8902 freq offset mode
6570  PRINT @ LO%, "freq ";  FO/1E6; " mhz; ampl 1 dbm"
6580  PRINT @ LT%, "27.0SP M4 27.3SP"; FO/1E6; "MZ" \ GOSUB 8200
6590  !
6600  ! Program 8902 to 6082 output frequency (in addition to offset)
6610  PRINT @ LT%, "FR"; F/1E6 ; "MZ"
6620                                        ! calibrate 8902 at new frequency
6630   IF (F>=BF AND MD$<>"verify") THEN GOSUB 7000 \PRINT @A%,"cc_resume"
6640  RETURN
7000  !
7010  !-----------------------------------------------------------------
7020  ! Subroutine to cal the 8902A in the tuned RF mode
7030  !
7040  ! Starts at -11.1 dBm so that first 24 dB pad is in for VSWR.
7050  ! Steps down in 3 dB increments making the cal transfers
7060  ! as it goes.  All transfers are made before measuring
7070  ! the attenuators so we don't have to be concerned about
7080  ! the measurement levels coinciding with the re-cal levels.
7090  !
7100  PRINT "Calibrating 8902 at ";F/1E6;" MHz ";
7110  AC = -11.1
7120  PRINT @ A%, "ampl "; AC; "dbm"      ! program Siggen amplitude
7130  PRINT ".";
7140  GOSUB 16000                         ! zero power-meter
7150  GOSUB 9000                          ! tuned RF mode and 1st transfer
7160  !
7170  FOR AC = -11.1 TO -70 STEP -3.0
7180    PRINT @ A%, "ampl "; AC; "dbm"
7190    PRINT ".";
7200    GOSUB 8200                        ! short delay
7210    S% = SPL(LT%)                     ! Check recal bit
7220    IF ((S% AND 32%) = 0) GOTO 7500   !   Skip cal if bit isn't set
7230      PRINT @ LT%, "C1"               ! calibrate 8902
7240      GOSUB 8000                      ! long delay
7250      S% = SPL(LT%)                   ! clear serial poll status
7260      S% = SPL(LT%)                   ! recal/uncal bit should be cleared
7270      IF ((S% AND 32%) = 0) GOTO 7500
7280        PRINT "8902A Calibration failed at: ";F;" Hz, and ";AC" dBm"
7290        STOP
7500  NEXT AC
7590  !
```

```
7600  PRINT @ LT%, "M4 LG"                ! switch back to power-meter mode
7610  GOSUB 8200 \ PRINT " done"          ! short delay
7620  RETURN
8000  !
8010  !-------------------------------------------------------------
8020  ! Wait 15 seconds then throw one reading away
8030  !
8040  WAIT 15000%
8050  INPUT @ LT%, RD
8060  RETURN
8200  !
8210  !-------------------------------------------------------------
8220  ! Wait 200 ms then throw one reading away
8230  !
8240  WAIT 200%
8250  INPUT @ LT%, RD
8260  RETURN
9000  !
9010  !-------------------------------------------------------------
9020  ! switch to tuned RF mode
9030  !
9040  IF(MD$ = "verify") THEN PRINT "switching to tuned RF mode ... ";
9050  WAIT 5000 \ GOSUB 4000           ! medium delay
9060  GOSUB 16000                      ! zero power-meter
9070  PRINT @ LT%, "S4"                ! change to tuned RF mode
9080  GOSUB 8000                       ! long delay
9090  PRINT @LT%,"C1" \ GOSUB 8000     ! always cal at first point
9100  S% = SPL(LT%)                    !   clear serial poll status
9110  IF(MD$ = "verify") THEN PRINT "done"
9120  RETURN
10000 !
10010 !-------------------------------------------------------------
10020 ! Level Verification
10030 !
10040 ! Steps through the specified frequencies and amplitudes and
10050 ! compares the measured level to the expected level.  The
10060 ! results are printed to display and to the file "lc8902.vfy".
10070 ! Calibrates the 8902 as needed as it steps the level down.
10080 !
10090 ! Performs the following actions:
10100 !
10110 !    Loads verification frequency list (subroutine 12000)
10120 !    Foreach frequency in list
10130 !    {
10140 !        Program SigGen frequency
10150 !        Foreach amplitude from +13 dBm to -125 dBm step -6 dB
10160 !        {
10170 !            Program 8902
10180 !            Program SigGen level
10190 !            Re-cal 8902 if needed
10200 !            Get reading from 8902 and print results
10210 !                (Take a second reading if out-of-spec)
10220 !            Step down 3 dB in small steps
10230 !            Re-cal 8902 if needed
10240 !            Step down 3 dB again in small steps
```

```
10250 !         }
10260 !     }
10270 !
10280 !
10290 OPEN "lc8902.vfy" AS NEW FILE 1
10300 !
10310 BF =    0.0   ! All freqs verified to low levels
10320 SA =   13.0   ! Starting amplitude
10330 EL = -114.0   ! Ending amplitude for 6080
10340 EG = -100.0   ! Ending amplitude for 6082 When (F > 1300 MHz)
10350 AI =   -6.026 ! Amplitude increment
10360 MX =    1.0   ! Spec limit
10370 WE =    0.0   ! Worst error of verification run
10380 !
10390 TS$ = TIME$
10400 !
10410 GOSUB 12000                         ! load freq list into array "FR()"
10420                                     !   and number of freqs into N%
10430 FL = 0                              ! "FL" = previous frequency
10440 !
10450 FOR FI% = 1% TO N%
10460 !{
10470    F = FR(FI%)                       ! "F"  = current frequency
10480    PRINT @A%, "freq ";F;"hz"
10490    !
10500    IF( F <= 1300E6 ) THEN EN = EL ! "EN" is lowest amplitude
10510    IF( F >  1300E6 ) THEN EN = EG !     tested (depends on freq)
10520    TP = -9999                     ! "TP" = previous target
10530    EF$ = "good"                   ! "EF" = error flag for retry
10540    NS = 1                         ! "NS" = # of small ampl steps
10550    SD = 100                       ! "SD" = normal step-down delay
10560    !
10590    FOR AP = SA TO EN STEP AI
10600    !{
10610       IF( AP < -100 ) THEN NS = 6 \ SD = 500  ! step down slowly
10620       T = AP
10630       PRINT @A%, "ampl ";AP;"dbm"  ! Program siggen level
10640       IF(F <> FL) THEN GOSUB 6000  ! If new freq, Tune 8902
10650       !
10660       GOSUB 5000                   ! Zero Pmeter, or tuned RF
10670       FL = F
10680       GOSUB 11000                  ! Calibrate 8902 if needed
10690       GOSUB 4000                   ! Get reading
10700       !
10710       ! Print results, flag out-of-spec errors with asterisks
10720       ER = RD-AP
10730       IF( ABS(ER) > ABS(WE) ) THEN WE = ER
10740       IF( ABS(ER) > MX ) THEN FL$ = " ****" ELSE FL$ = "     "
10750       PRINT     USING "S#####.###", F/1E6, AP, RD, ER; FL$
10760       PRINT #1, USING "S#####.###", F/1E6, AP, RD, ER; FL$
10770       !
10780       ! Try again if out-of-spec (** JUMP TO TOP OF LOOP **)
10790       IF(ABS(ER) > MX AND EF$ = "good") THEN EF$="bad" \ GOTO 10600
10800       !
10810       ! Step smoothly in small steps to next amplitude
```

```
10820       FOR SI = 1 TO NS/2
10830         PRINT @A%,"ampl ";AP + (SI*AI/NS);" dbm" \ WAIT SD
10840       NEXT SI
10850       GOSUB 11000                   ! Calibrate 8902 if needed
10860       FOR SI = NS/2 TO NS
10870         PRINT @A%,"ampl ";AP + (SI*AI/NS);" dbm" \ WAIT SD
10880       NEXT SI
10890       TP = T \ EF$ = "good"
10900     !}
10910   NEXT AP
10920 !}
10930 NEXT FI%
10940 !
10950 PRINT "started at :";TS$,"ended at :";TIME$
10960 PRINT "Worst Error = ";WE
10970 RETURN
11000 !-------------------------------------------------------------
11010 ! Calibrate 8902 during verification (if needed)
11020 !
11030 ! If serial poll status bit 32 is set, the 8902 is requesting
11040 ! recalibration.  Do the calibration and check the bit again.
11050 ! If it is still set, the calibration failed and we quit
11060 ! immediately.
11070 !
11080 GOSUB 8200
11090 S% = SPL(LT%)
11100 !
11110 ! Calibrate only if level below -11.1 and recal bit is set
11120 IF ((AP > -11.1) OR (S% AND 32%) = 0) GOTO 11200
11130   PRINT @ LT%, "C1"                  ! calibrate 8902
11140   GOSUB 8000                         ! long delay
11150   !
11160   S% = SPL(LT%)                      ! check recal bit again
11170   IF ((S% AND 32%) = 0) GOTO 11200
11180     PRINT "8902A Calibration failed at: ";F;" Hz, and ";AC" dBm"
11190     STOP
11200 RETURN
12000 !-------------------------------------------------------------
12010 !
12020 ! Load verification frequencies into table
12030 !
12040 ! The frequency list and number of frequencies used are
12050 ! specified by the data statements below.  The number
12060 ! of frequencies must match the number of table entries.
12070 !
12080 ! NOTE: All frequencies are verified in the tuned RF mode so the
12090 !       list cannot contain any frequencies less than 2.5 MHz.
12100 !
12110 DIM FR(30%)
12120 !
12130 ! Number of frequencies in table below
12140 DATA 14
12150 !
12160 ! Table of Frequencies in Hz
12170 DATA     10000000
```

```
12180 DATA     50000000
12190 DATA    100000000
12200 DATA    200000000
12210 DATA    400000000
12220 DATA    600000000
12230 DATA    800000000
12240 DATA   1000000000
12250 DATA   1200000000
12260 DATA   1400000000
12270 DATA   1600000000
12280 DATA   1800000000
12290 DATA   2000000000
12300 DATA   2112000000
12310 !
12700 READ N%
12710 IF (N% > 30%) THEN N% = 30%
12720 FOR FI% = 1% TO N%
12730     READ FR(FI%)   ! load frequency table
12740 NEXT FI%
12750 RETURN
16000 !
16010 !-------------------------------------------------------------
16020 ! Subroutine to zero power-meter in HP 8902A
16030 !
16040 PRINT @ LT%,"M4"    \ GOSUB 4000
16050 PRINT @ LT%,"ZR"    \ GOSUB 8000   ! long  delay
16060 PRINT @ LT%,"M4 LG" \ GOSUB 8200   ! short delay
16070 RETURN
24990 !-------------------------------------------------------------
25000 !
25010 ! Ask operator which procedure to use
25020 !
25030 MD% = 0%                     ! default is output
25040 PRINT "Select compensation procedure:"
25050 PRINT "    0 output"
25060 PRINT "    1 attenuator"
25070 PRINT "    2 output with default attenuator"
25080 PRINT "    3 level calibration"
25090 PRINT "    4 attenuator verification only"
25110 !
25120 INPUT MD%
25130 IF(MD% < 0% OR MD% > 4%) GOTO 25000
25140 IF(MD%=0%) THEN MD$="comp_out"
25150 IF(MD%=1%) THEN MD$="comp_att"
25160 IF(MD%=2%) THEN MD$="comp_outdef"
25170 IF(MD%=3%) THEN MD$="cal_level"
25190 IF(MD%=4%) THEN MD$="verify"
25200 RETURN
29000 !
29005 PRINT "Hung at ";F,AP \ PRINT CHR$(7) \ WAIT 10000
29010 PRINT @A%, "ampl_step 12 db"
29020 PRINT @A%, "step_ampl up; step_ampl down"
29025 PRINT #1,"Hung at ";F,AP
29030 RESUME
30000 !
```

```
30010 !-----------------------------------------------
30020 ! Finished, close up files and exit
30030 !
30040 CLOSE 1
30050 LOCAL
30060 END
```

Figure G-6. Example Sub-Synthesizer Compensation Program

```
1    ! Fluke 6080A Signal Generator Output/Attenuator compensation and
2    !    Level cal control program. Runs on a Fluke 1722A controller.
3    !
4    ! NOTE: enter the power meter calibration factors for your power
5    !    meter into the table in the subroutine beginning at line
6    !    7000.  Remember to specify the number of entries in the table.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS".  No indemnity or warranties
14   !    are provided, whether expressed or implied.  FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use.  In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
20   !
30   TIMEOUT 10000
50   INIT PORT 0
60   A% = 2%                      ! IEEE-488 address of Signal Generator
70   AP% = 13%                    ! IEEE-488 address of Power Meter
80   PRINT @ A%,"*rst;*cls"       ! initialize Signal Generator
90   GOSUB 3000                   ! initialize Power Meter
100  GOSUB 7000                   ! set up CAL factor tables
500  !
510  ! Ask operator which cal/comp procedure
520  !
530  MD% = 0%                     ! default level calibration
540  PRINT "Select calibration/compensation procedure:"
545  PRINT "    0 for level calibration"
550  PRINT "    1 for output compensation"
560  PRINT "    2 for attenuator compensation"
570  PRINT "    3 for output with default attenuator compensation"
580  INPUT MD%
590  IF (MD% < 0 OR MD% > 3%) GOTO 500
595  IF (MD% = 0%) THEN CM$ = "cal_level"
600  IF (MD% = 1%) THEN CM$ = "comp_out"
610  IF (MD% = 2%) THEN CM$ = "comp_att"
620  IF (MD% = 3%) THEN CM$ = "comp_outdef"
630  !
640  PRINT @A%,CM$
650  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EM$
660  IF (ST% = 0 ) THEN GOTO 800
670      PRINT "There is an error with the 6080A."
680      PRINT ST%,EM$
690      STOP
800  !
810  GOSUB 5000                   ! zero power meter
820  TL = 10                      ! flag used to determine when to zero meter
1000 !
```

```
1010 ! Main loop
1020 !
1030     ! get frequency, exit main loop on last frequency
1040     PRINT @ A%,"cc_freq?" \ INPUT @ A%,F,UN$
1050     IF (F = 9E9) GOTO 2000
1060     !
1070     ! zero power meter before measuring first 24 dB attenuator
1080     !  (target level changes from -2 dBm to -14 dBm).
1090     PRINT @ A%,"cc_target?" \ INPUT @A%,T,UN$
1100     IF ((T = -14) AND (TL = -2)) THEN GOSUB 5000  ! zero power meter
1110     TL = T
1120     !
1130     ! get power meter reading
1140     GOSUB 4000               ! reading -> RD
1150     !
1160     ! send power meter reading to 6080A
1170     PRINT @ A%,"cc_rdpower ";RD;" dbm"
1180 GOTO 1000
2000 !
2010 ! Store results
2020 !
2030 PRINT @ A%,"cc_save"         ! save data in compensation memory
2040 IF( CM$ <> "comp_att" ) THEN GOTO 2050
2045     WAIT 45000               ! wait 45 seconds for atten store
2050 PRINT @ A%,"error?" \ INPUT @ A%,ST%
2060 IF (ST% = 0 OR ST% = 79%) THEN GOTO 2900
2080     PRINT ST%
2100     STOP
2900 END
3000 !
3010 ! Subroutine to initialize HP 436A Power Meter
3020 ! P$ is used when zeroing the power meter too
3030 !
3040     P$ = "D+9H"          ! dBm mode, no CAL factor, auto range, Hold
3050     PRINT @ AP%,P$
3060     PRINT @ AP%,"I"      ! get first reading
3070     INPUT LINE @ AP%,RD$ ! throw it away
3080 RETURN
4000 !
4010 ! Subroutine to get readings from HP 436A Power Meter
4020 !
4030 ! Get two readings within .01 dB, then read eight
4040 !   more and return the average of all ten.
4050 !
4060     ! set delay to 200 ms or 400 ms if 24 dB pad
4070     WT% = 200%
4080     IF( T = -14 ) THEN WT% = 400%
4090     !
4100     ! wait 2 seconds
4110     WAIT 2000 \ PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4120     !
4130     R1 = VAL(RIGHT(RD$,4))
4480     !
4490     ! get settled reading
4500     !
```

```
4510         WAIT WT% \ PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4520         RD = VAL(RIGHT(RD$,4))
4530         IF ABS(RD-R1) <= .01 THEN GOTO 4600
4540         R1 = RD
4550     GOTO 4500
4580     !
4590     ! The reading is in the settled range, now average more.
4600     R1 = R1 + RD    ! sum includes last 2 readings
4605     AV = 4.0
4610     FOR I% = 1% TO (AV-2)
4620        PRINT @ AP%,"I" \ INPUT LINE @ AP%,RD$
4630        RD = VAL(RIGHT(RD$,4))
4640        R1 = R1 + RD
4650     NEXT I%
4660     RD = R1 / AV
4670     !
4800     GOSUB 6000               ! power meter CAL factor -> CF
4810     RD = RD + CF
4840 RETURN
5000 !
5010 ! Subroutine to zero HP 436A Power Meter
5020 ! P$ is set up in the power meter initialization routine
5030 !
5040     PRINT @ A%,"rfout off" \ WAIT 100
5050     PRINT @ AP%,"Z1T" \ WAIT 1000
5060     PRINT @ AP%,P$ \ WAIT 5000
5070     PRINT @ A%,"rfout on" \ WAIT 30
5080 RETURN
6000 !
6010 ! Subroutine to compute power meter CAL factor
6020 !
6030     ! use first data point if frequency is low
6040     CF = 10 * LOG(1/CA(1%))
6050     IF (F/1.0E6 <= FR(1%)) THEN RETURN
6060     !
6070     ! use last data point if frequency is high
6080     CF = 10 * LOG(1/CA(30%))
6090     IF (F/1.0E6) >= FR(30%) THEN RETURN
6100     !
6110     ! search table for closest frequency points
6120     I% = 1%
6130     IF (F/1.0E6 < FR(I%)) THEN GOTO 6500
6140     I% = I% + 1%
6150     GOTO 6130
6500     !
6510     ! interpolate between frequency points
6520     D = (F/1.0E6 - FR(I%-1%)) / (FR(I%)-FR(I%-1%))
6530     C = ( D * (CA(I%)-CA(I%-1%)) ) + CA(I%-1%)
6540     !
6550     ! convert ratio to dB
6560     CF = 10 * LOG(1/C)
6570 RETURN
7000 !
7010 ! Subroutine to set up CAL factor tables
7020 !
```

```
7030 ! Number of frequencies used - Maximum of 30
7040 DATA 11
7050 !
7060 ! Table of Frequencies in MHz, and CAL factors
7065 !    as multiplicative scale factors.
7066 !    (Nominally multiply by 1.00).
7070 DATA   .1, 1.00
7080 DATA   .3, 1.00
7090 DATA    1, 1.00
7100 DATA    3, 1.00
7110 DATA   10, 1.00
7120 DATA   30, 1.00
7130 DATA  100, 1.00
7140 DATA  300, 1.00
7150 DATA 1000, 1.00
7160 DATA 1700, 1.00
7170 DATA 2100, 1.00
7300 !
7310 DIM FR(30%), CA(30%)
7320 !
7330 READ N% \ IF (N% > 30%) THEN N% = 30%
7340 FOR I% = 1% TO N%
7350     READ FR(I%) ! load frequency table
7360     READ CA(I%) ! load CAL factor table
7370 NEXT I%
7380 !
7390 !
7400 FOR I% = N%+1% TO 30%
7410     FR(I%) = FR(N%) ! fill in rest of tables
7420     CA(I%) = CA(N%)
7430 NEXT I%
7440 RETURN
```

Figure G-7. Example Coarse Loop Compensation Program

```
5    ! Fluke 6080A Signal Generator Coarse Loop Compensation control program.
6    !    Runs on a Fluke 1722A controller.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS". No indemnity or warranties
14   !    are provided, whether expressed or implied. FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use. In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
50   INIT PORT 0
60   A% = 2%                  ! IEEE-488 address of Signal Generator
70   TIMEOUT 0                ! Infinite timeout
80   CLEAR @ A%               ! device clear
90   PRINT @ A%,"*rst;*cls"   ! initialize Signal Generator
100  PRINT @ A%,"comp_coarse" ! start coarse comp procedure
110  PRINT @ A%,"*opc?"       ! wait for operation complete
120  INPUT @ A%, R$
130  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EX$
140  IF (ST% = 0 ) THEN GOTO 200
150      PRINT ST%,EX$
160      STOP
200  END
```

Figure G-8. Example Sum Loop Compensation Program

```
5    ! Fluke 6080A Signal Generator Sum Loop Compensation control program.
6    !    Runs on a Fluke 1722A controller.
7    !
8    ! The rear panel CAL|COMP switch must be set to 1 (on) before
9    !    running this program.
10   !
11   ! Disclaimer:
12   !
13   !    This program is provided "AS IS". No indemnity or warranties
14   !    are provided, whether expressed or implied. FLUKE specifically
15   !    disclaims the implied warranties or merchantability and fitness
16   !    for the purpose or use. In no event shall FLUKE be liable for
17   !    any loss of data, use, profits or goodwill, or for special,
18   !    incidental, consequential or other similar damages.
19   !
40   !
50   INIT PORT 0
60   A% = 2%                  ! IEEE-488 address of Signal Generator
70   TIMEOUT 0                ! Infinite timeout
80   CLEAR @ A%               ! device clear
90   PRINT @ A%,"*rst;*cls"   ! initialize Signal Generator
100  PRINT @ A%,"comp_sum"    ! start sum comp procedure
110  PRINT @ A%,"*opc?"       ! wait for operation complete
120  INPUT @ A%, R$
130  PRINT @ A%,"error? explain" \ INPUT @ A%,ST%,EX$
140  IF (ST% = 0 ) THEN GOTO 200
150      PRINT ST%,EX$
160      STOP
200  END
```

Index

A1 Display PCA (see Display PCA)
A2 Coarse Loop PCA (see Coarse Loop PCA)
A3 Subsynthesizer VCO PCA (see Subsynthesizer VCO PCA)
A4 Subsynthesizer PCA (see Subsynthesizer PCA)
A5 Coarse Loop VCO PCA (see Coarse Loop VCO PCA)
A6 Mod Oscillator PCA (see Mod Oscillator PCA)
A8 Output PCA (see Output PCA)
A9 Sum Loop VCO PCA (see Sum Loop VCO PCA)
A10 Premodulator PCA (see Premodulator PCA)
A11 Modulation Control PCA (see Mod Control PCA)
A12 Sum Loop PCA (see Sum Loop PCA)
A13 Controller PCA (see Controller PCA)
A14 FM PCA (see FM PCA)
A15 Power Supply PCA (see Power Supply PCA)
A16 IEEE-488 Connector PCA (see IEEE-488 Connector PCA)
A19 Switch PCA (see Switch PCA)
A20A7 Relay Driver PCA (see Relay Driver PCA)
A20A21 Attenuator PCA (see Attenuator PCA)
Access procedures, 5-1 (also see replacing modules)
  A2 Coarse Loop PCA, **5-4**
  A3 Subsynthesizer VCO PCA, **5-5**
  A4 Subsynthesizer PCA, **5-5**
  A5 Coarse Loop VCO PCA, **5-5**
  A6 Mod Oscillator PCA, **5-6**
  A8 Output PCA, **5-6**
  A9 Sum Loop VCO PCA, **5-7**
  A10 Premodulator PCA, **5-7**
  A11 Modulation Control PCA, **5-7**
  A12 Sum Loop PCA, **5-8**
  A13 Controller PCA, **5-8**
  A14 FM PCA, **5-9**
  A20 Attenuator/RPP Assembly, **5-9**
  A22 Delay Cable Assembly, **5-10**
  Front panel section, **5-2**
  Rear panel section, **5-3**
Acquisition circuits, **6C-39**
Address decoding, **6B-7**
Alignment, introduction, **6-1**
Alternate reference frequency, setting SW502 for, **6C-33**
Amplitude modulation, **2-7**
Attenuator PCA (A20, A21)
  Access procedure, **5-9**
  Attenuator control interface, **6B-3**
  Attenuator/reverse-power protection (RPP)
  Circuit, **6D-21**
  Parts list, **8-72**
  Schematic, **10-60**
  Troubleshooting, **6D-22**
AUX connector, using, **F-1**
Calibration
  AM, **4-3**
  AM, front panel procedure, **4-4**
  AM, remote procedure, **4-4**
  Closed-case, **4-1**
  Data, **4-3**
  FM, **4-7**
  FM, front panel procedure, **4-7**
  FM, remote procedure, **4-8**
  Front panel, **4-1**
  Remote, **4-1**
  Setup, **4-3**
Calibration/compensation memory, **6B-8**
  Memory origin status, **6B-9**
  Memory status, **6B-8**
  Repairing checksum errors, **6B-9**
Circuit description, introduction, **6-1**
Coarse Loop (also see Coarse Loop PCA and Coarse Loop VCO PCA)
  RF Levels **6C-25**
  Tests **6-15**
  VCO Binary Band Control Signals **6C-34**

- Coarse Loop PCA (A2)
  - Access procedure, **5-4**
  - Adjustments
    - 2-MHz notch adjustment, L205, **6C-33**
    - 40-MHz oscillator adjustment, L601, **6C-31**
    - 80-MHz filter tuning, L612 and L613, **6C-32**
    - 80-MHz level adjustment, R617, **6C-32**
    - Acquisition oscillator level adjustment, R227, **6C-31**
    - Alternate reference frequency selection, **6C-33**
    - Discriminator video amplifier offset adjustment, R102, **6C-30**
    - Steering gain adjustment, R221, **6C-30**
  - Circuit description, **6C-17**
    - Coarse loop, **6C-20**
    - Reference section, **6C-17**
  - Compensation procedure, front panel, **7-29**
  - Compensation procedure, remote, **7-31**
  - Parts list, **8-23**
  - Schematic, **10-6**
  - Test points, **6C-29**
  - Troubleshooting, **6C-23**
    - Main loop, **6C-25**
    - Reference section, **6C-23**
- Coarse Loop VCO PCA (A5)
  - Access procedure, **5-5**
  - Block diagram, **6C-21**
  - Circuit description, **6C-34**
  - Parts list, **8-34**
  - Schematic, **10-17**
  - Troubleshooting, **6C-35**
- Controller PCA (A13)
  - Access procedure, **5-8**
  - Block diagram, **6B-2**
  - Circuit description **6B-1**
  - Parts list, **8-57**
  - Schematic, **10-40**
  - Software description, **2-8**
    - Calibration/compensation memory, **2-9**
    - Self test, **2-9**
    - Status signals, **2-9**
    - User interface, **2-8**
  - Troubleshooting, **6B-4**
    - Address decoder, **6B-6**
    - Bus error, **6B-5**
    - Clock, **6B-5**
    - Interrupts, **6B-5**
    - I/O diagnostic tests, **6B-7**
    - Microprocessor bus, **6B-6**
    - Microprocessor kernel, **6B-5**
    - Power-on reset, **6B-5**
    - RF control, **6B-4**
    - Unused microprocessor inputs, **6B-5**
- Compensation procedures, **7-1**
- Diagnostic functions, **6-13**
  - Digital control latch test, **6-13**
  - Display synthesizer loop frequencies, **6-13**
  - Instrument diagnostic state, **6-13**
  - Set internal DACs, **6-13**
- Display PCA (A1)
  - Access procedure, **5-2**
  - Parts list, **8-21**
  - Schematic **10-3**
- Equipment verification, **3-35**
- Factory service, obtaining, **1-2**
- Fault tree, frequency synthesis, **6C-2**
- Flatness test, **3-13**
- Fluke Sales and Service Centers, **G-1**
- FM PCA (A11)
  - Access procedure, **5-9**
  - Adjustments, **6E-14**
  - Alignment, **6E-16**
  - Parts list, **8-60**
  - Schematic, **10-45**
  - Troubleshooting, **6E-12**
    - Frequency check, **6E-12**
    - Input signals and control input signals checks, **6E-14**
    - Modulation check, **6E-13**
- FM/ϕM block diagram, **6E-1**
- FM/ϕM circuit description, **6E-1**
  - Divider section, **6E-5**
  - Modulation section, **6E-9**
  - Oscillator section, **6E-4**
  - Phase detectors, loop circuits, and logic section, **6E-6**
  - Fault tree, **6E-1**
- Frequency, **2-2**
  - Accuracy test, **3-5**
  - And phase modulation circuit description, troubleshooting, and alignment **6E-1**
  - Band logic states **6D-9**
  - Coverage bands **2-3**
  - Fault tree, **6C-1**
  - Modulation, **2-4**
  - Synthesis circuit description, troubleshooting, and alignment, **6C-1**
- Front panel
  - Access procedure, **5-2**
  - Circuit description, **6B-9**
  - Bright-digit effect, **6B-10**
  - Data communications, **6B-10**
  - Display blanking, **6B-11**
  - Display filament voltage, **6B-10**
  - Display PCA, **6B-10**
  - Edit knob interface, **6B-10**
  - Interface, **6B-3**
  - Operate/standby selection, **6B-11**
  - Remote footswitch (AUX connector), **6B-10**
  - Switchboard interface, **6B-10**
  - Troubleshooting, **6B-11**
- Functional description, **2-2**
- Harmonic and line-related spurious test, **3-15**
- High-Stability Reference, Option 6080A-130, **9-1**
  - Adjusting the reference frequency, **9-1**
  - Parts list, **9-2**
- IEEE-488 Connector PCA (A16)

- Parts list, **8-67**
- Interface, **6B-3**
- Schematic, **10-53**

Instrument preset state, **A-1**

Intermodulation
- Distortion test, **3-36**
- Intermodulation test, **3-35**

Internal mod oscillator, see Mod Oscillator PCA (A6)

Level accuracy test
- Alternate, **3-11**
- High-level, **3-6**
- Low-level, **3-10**
- Mid-level, **3-9**

Level flatness compensation, **7-1**
- Accuracy notes, **7-3**
- Compensating level flatness errors in an external system, **7-9**
- Front panel attenuator flatness compensation procedure, **7-10**
- Front panel attenuator flatness compensation procedure using power meter, **7-15**
- Front panel output compensation with default attenuator data, **7-9**
- Front panel output flatness compensation procedure, **7-5**
- Het band level adjustment, **7-8**
- Level compensation data mixing, **7-4**
- Limits **7-3**
- Procedures
  - Remote, **7-18**
  - Remote attenuator compensation procedure, **7-20**
  - Remote output compensation procedures, **7-18**

Location of major assemblies, **5-2**

Loop amplifier, **6C-39**

Manual status information, **8-5**

Medium-Stability Reference (6080A-132), **9-2**
- Adjusting the reference frequency, **9-2**
- Parts list, **9-3**

Memory, **6B-1**

Memory control, **6B-3**

Microprocessor, **6B-1**

Mod Control PCA (A11)
- Access procedure, **5-7**
- Circuit description, **6E-11**
- FM control signals generation, **6E-12**
- FM input voltage processing, **6E-11**
- FM steer voltage generation, **6E-12**
- Parts list, **8-49**
- Schematic, **10-32**
- Test points, **6D-11**

Mod Oscillator PCA (A6)
- Access procedure, **5-6**
- Block diagram, **6F-1**
- Circuit description, **6F-1**
- Direct digital synthesized wave generator, **6F-1**
- Parts list, **8-36**
- Pulse generator, **6F-3**
- Schematic, **10-19**
- Signal routing, **6F-3**
- Troubleshooting and adjustments, **6F-4**
  - Direct digital synthesizer, **6F-4**
  - Pulse generator, **6F-5**

Modulation tests, **3-22**
- Amplitude modulation tests, **3-23**
- Frequency modulation tests, **3-26**
- Internal modulation oscillator tests, **3-30**
- Phase modulation tests, **3-28**

Module I/O interface, **6B-3**

N-Divider Logic States **6C-27**

Non-harmonic spurious.signals test using RF spectrum analyzer, **3-16**

Options, **9-1**

Output leakage test, **3-14**

Output/level control, **2-7**

Output PCA (A8) (also see RF level)
- Access procedure, **5-6**
- Parts list, **8-38**
- Schematic, **10-22**

Overrange/uncal status codes, **D-1**

Parts lists
- A1 Display PCA, **8-21**
- A2 Coarse Loop PCA, **8-23**
- A3 Subsynthesizer VCO PCA, **8-28**
- A4 Subsynthesizer PCA , **8-30**
- A5 Coarse Loop VCO PCA, **8-34**
- A6 Mod Oscillator PCA, **8-36**
- A7 Relay Driver PCA, **8-70**
- A8 Output PCA, **8-38**
- A9 Sum Loop VCO PCA, **8-43**
- A10 Premodulator PCA, **8-45**
- A11 Modulation Control PCA, **8-49**
- A12 Sum Loop PCA, **8-53**
- A13 Controller PCA, **8-57**
- A14 FM PCA, **8-60**
- A15 Power Supply PCA, **8-65**
- A16 IEEE-488 Connector PCA, **8-67**
- A19 Switch PCA, **8-68**
- A20 Attenuator/RPP Assembly, **8-69**
- A21 Attenuator PCA, **8-72**
- A22 Delay Line PCA, **8-74**
- Final Assembly, **8-6**
- How to obtain parts, **8-3**

Performance tests, **3-1**

Phase modulation, **2-6**

Phase noise, residual FM, and spurious signals test, **3-16**

Pivoting synthesizer module warning, **5-2**

Power Supply PCA (A15), **2-8**
- Adjustment procedure, **6A-5**
- Block diagram, **6A-2**
- Circuit description, **6A-1**
- Parts list, **8-65**
- Schematic, **10-50**
- Troubleshooting, **6A-4**

Power-on test, **3-4**

Premodulator PCA (A10)

  - Access procedure, **5-7**
  - Block diagram, **6D-3**
  - Parts list, **8-45**
  - Schematic, **10-28**
- Pulse modulation, **2-7**
- Pulse tests, **3-33**
- Raising and lowering the synthesizer module, **5-3**
- Rear Output/Modulation Input (Option 6080A-830), **9-3**
  - Theory of operation, **9-3**
  - Parts list, **9-4**
- Reference oscillator calibration, **4-12**
  - Front panel procedure, **4-12**
  - Remote procedure, **4-13**
- Rejected entry codes, **C-1**
- Relay Driver PCA
  - Parts list, **8-70**
  - Schematic, **10-58**
- Removing PCAs, see access procedures and replacing modules
- Replacing modules, **6-5**
  - A1 Display PCA, **6-5**
  - A2 Coarse Loop PCA, **6-5**
  - A3 Subsynthesizer VCO PCA, **6-5**
  - A4 Subsynthesizer PCA, **6-7**
  - A5 Coarse Loop VCO PCA, **6-7**
  - A6 Mod Oscillator PCA, **6-8**
  - A7 Relay Driver PCA, **6-8**
  - A8 Output PCA, **6-8**
  - A9 Sum Loop VCO PCA, **6-8**
  - A10 Premodulator PCA, **6-8**
  - A11 Modulation Control PCA, **6-8**
  - A12 Sum Loop PCA, **6-9**
  - A13 Controller PCA, **6-9**
  - A14 FM board PCA, **6-9**
  - A15 Power Supply PCA, **6-9**
  - A19 Switch PCA, **6-9**
  - A20 Attenuator/RPP Assembly (A7, A21, A30), **6-9**
  - A22 Delay Line Assembly (A25, A26, Delay Cable, Trim Cable), **6-9**
    - Self test description, **6-11**
    - Updating compensation memory with module exchange data, **6-10**
- Residual AM noise test, **3-20**
- RF level adjustments, **6D-10**
  - FM gain adjustment, R82, on Mod Control PCA, **6D-21**
  - FM inv balance, R102 on Mod Control PCA, **6D-21**
  - FM steer gain, R101 on Mod Control PCA, **6D-21**
  - Mod Control PCA AM DAC offset adjustment, R8, **6D-12**
  - Mod Control PCA AM depth adjustment, R10, **6D-14**
  - Mod Control PCA detector offset adjustment, R28, **6D-13**
  - Mod Control PCA external modulation level indicator adjustment, R71, **6D-16**
  - Mod Control PCA level DAC offset adjustment, R23, **6D-12**
  - Mod Control PCA RF level adjustment, R20, **6D-15**
  - Mod Control PCA sum steer gain adjustment, R99, **6D-16**
  - Output PCA gain flatness adjustment, C201, **6D-20**
  - Output PCA het level adjustment, R10, **6D-18**
  - Output PCA het mixer level adjustment, R72, **6D-17**
  - Output PCA Q16 bias adjustment, R96, **6D-19**
  - Output PCA Q9 bias adjustment, R1, **6D-20**
  - Premodulator PCA bandwidth adjustment, R51 and C7, **6D-19**
- RF level block diagram, **6D-1**
- RF level calibration, **4-9**
  - Front panel procedure, **4-10**
  - Remote procedure, **4-10**
- RF level circuit description, **6D-4**
  - Level control, **6D-7**
  - Leveling loop, **6D-6**
  - RF path, **6D-4**
- RF level troubleshooting, **6D-8**
  - Fault tree, **6D-1**
  - Output assembly test point signal information, **6D-10**
  - Unleveled condition, **6D-8**
  - Troubleshooting, **6D-8**
- Safety, following Title Page, **5-1**
- Schematic diagrams
  - A1 Display PCA, **10-3**
  - A2 Coarse Loop PCA, **10-6**
  - A3 Subsynthesizer VCO PCA, **10-11**
  - A4 Subsynthesizer PCA, **10-13**
  - A5 Coarse Loop VCO PCA, **10-17**
  - A6 Mod Oscillator PCA, **10-19**
  - A8 Output PCA, **10-22**
  - A9 Sum Loop VCO PCA, **10-26**
  - A10 Premodulator PCA, **10-28**
  - A11 Modulation Control PCA, **10-32**
  - A12 Sum Loop PCA, **10-36**
  - A13 Controller PCA, **10-40**
  - A14 FM PCA, **10-45**
  - A15 Power Supply PCA, **10-50**
  - A16 IEEE Connector PCA, **10-53**
  - A17 Cable Transition PCA, **10-54**
  - A18 Cable Transition PCA, **10-55**
  - A19 Switch PCA, **10-56**
  - A20A7 Relay Driver PCA, **10-58**
  - A20A21 Attenuator PCA, **10-60**
  - A22 Delay Line Assembly, **10-61**
- Self test status codes, **E-1**
- Service centers, **8-4**
- Special function table, **B-1**
- Specifications, **1-2**
- Status
  - And control latches, **6B-4**
  - Signals and status codes, **6-13**
- Subsynthesizer PCA (A4)
  - 10-kHz notch adjustment, L56, **6C-15**
  - Access procedure, **5-5**
  - Adjustments, **6C-13**
    - Lower clamp adjustment, R99, **6C-13**

    - SSB mixer LO drive adjustment, R106, **6C-14**
    - Steering DAC full-scale adjustment, **6C-13**
    - Upper clamp adjustment, R98, **6C-14**
  - Block diagram, **6C-3**
  - Circuit description, **6C-1**
    - DACs and latches, **6C-9**
    - Loop amplifier, **6C-9**
    - Low-order digits generator, **6C-9**
    - N-divider, **6C-4**
    - Phase detector, **6C-8**
    - Single-sideband mixer, **6C-1**
  - Compensation procedures, **7-25**
    - Front panel, **7-26**
    - Remote, **7-28**
  - Parts list, **8-30**
  - Schematic, **10-13**
  - Troubleshooting, **6C-9**
- Subsynthesizer VCO PCA (A3)
  - Access procedure, **5-5**
  - Circuit description, **6C-16**
  - Parts list, **8-28**
  - Schematic, **10-11**
  - Troubleshooting, **6C-16**
- Sum Loop PCA (A12)
  - Access procedure, **5-8**
  - Adjustments, **6C-45**
    - Acquisition oscillator level adjustment, R132, **6C-47**
    - Buffer gain match adjustment, R121, **6C-45**
    - FM null adjustment, R116, **6C-46**
    - Loop gain adjustment, R167, **6C-47**
    - Steering level adjustment, R112, **6C-45**
  - Block diagram, **6C-35**
  - Circuit description, **6C-37**
    - Audio section, **6C-39**
    - RF section, **6C-37**
  - Compensation procedures, **7-31**
    - Front panel, **7-32**
    - Remote, **7-33**
  - Parts list, **8-53**
  - RF circuitry test information **6C-43**
  - RF section dc bias voltages **6C-43**
  - Schematic, **10-36**
  - Test points **6C-44**
  - Troubleshooting, **6C-41**
- Sum Loop VCO PCA (A9)
  - Access procedure, **7**
  - Adjustment, **6C-50**
  - Circuit description, **6C-48**
  - Parts list, **8-43**
  - Schematic, **10-26**
  - Steering circuit, **6C-40**
  - Troubleshooting, **6C-49**
- Switch PCA (A19)
  - Parts list, **8-68**
  - Schematic, **10-56**
- Synthesis test, **3-5**
- Test equipment, **3-1**
- Tests
  - AM, **6-11**
  - Coarse loop, **6-12**
  - DC FM, **6-12**
  - Digital, **6-11**
  - Filter, **6-13**
  - FM, **6-11**
  - ϕM, **6-12**
  - Pulse modulator, **6-12**
  - RF output, **6-12**
  - Subsynthesizer, **6-12**
  - Sum loop, **6-12**
- Theory of operation, **2-1**
- Troubleshooting, introduction, **6-2**
- Voltage standing-wave ratio (VSWR) tests, **3-31**